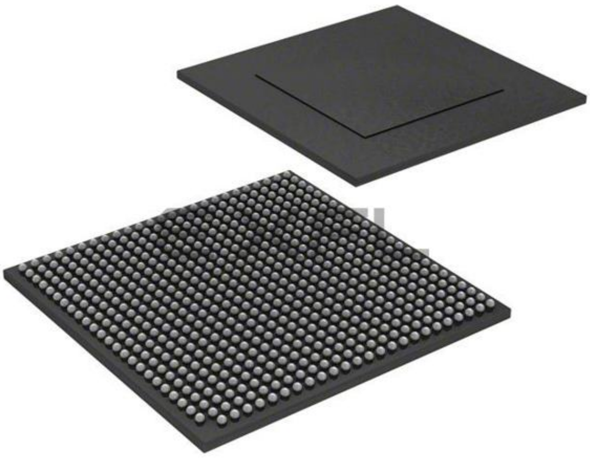

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Not For New Designs
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	4 Core, 32-Bit
Speed	852MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (1)
SATA	SATA 3Gbps (1)
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-40°C ~ 125°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	624-FBGA, FCBGA
Supplier Device Package	624-FCBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6q4avt08ac

— Gigabit Ethernet Controller (IEEE1588 compliant), 10/100/1000[1] Mbps
— Four Pulse Width Modulators (PWM)
— System JTAG Controller (SJC)
— GPIO with interrupt capabilities
— 8x8 Key Pad Port (KPP)
— Sony Philips Digital Interconnect Format (SPDIF), Rx and Tx
— Two Controller Area Network (FlexCAN), 1 Mbps each
— Two Watchdog timers (WDOG)
— Audio MUX (AUDMUX)
— MLB (MediaLB) provides interface to MOST Networks (150 Mbps) with the option of DTCP cipher accelerator

The i.MX 6Dual/6Quad processors integrate advanced power management unit and controllers:

- Provide PMU, including LDO supplies, for on-chip resources
- Use Temperature Sensor for monitoring the die temperature
- Support DVFS techniques for low power modes
- Use Software State Retention and Power Gating for ARM and MPE
- Support various levels of system power modes
- Use flexible clock gating control scheme

The i.MX 6Dual/6Quad processors use dedicated hardware accelerators to meet the targeted multimedia performance. The use of hardware accelerators is a key factor in obtaining high performance at low power consumption numbers, while having the CPU core relatively free for performing other tasks.

The i.MX 6Dual/6Quad processors incorporate the following hardware accelerators:

- VPU—Video Processing Unit
- IPUv3H—Image Processing Unit version 3H (2 IPUs)
- GPU3Dv4—3D Graphics Processing Unit (OpenGL ES 2.0) version 4
- GPU2Dv2—2D Graphics Processing Unit (BitBlt)
- GPUVG—OpenVG 1.1 Graphics Processing Unit
- ASRC—Asynchronous Sample Rate Converter

Security functions are enabled and accelerated by the following hardware:

- ARM TrustZone including the TZ architecture (separation of interrupts, memory mapping, etc.)
- SJC—System JTAG Controller. Protecting JTAG from debug port attacks by regulating or blocking the access to the system debug features.
- CAAM—Cryptographic Acceleration and Assurance Module, containing 16 KB secure RAM and True and Pseudo Random Number Generator (NIST certified)
- SNVS—Secure Non-Volatile Storage, including Secure Real Time Clock

1. The theoretical maximum performance of 1 Gbps ENET is limited to 470 Mbps (total for Tx and Rx) due to internal bus throughput limitations. The actual measured performance in optimized environment is up to 400 Mbps. For details, see the ERR004512 erratum in the i.MX 6Dual/6Quad errata document (IMX6DQCE).

voltage. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded, to take the necessary steps. This regulator has a built in power-mux that allows the user to select to run the regulator from either VBUS supply, when both are present. If only one of the VBUS voltages is present, then the regulator automatically selects this supply. Current limit is also included to help the system meet in-rush current targets. If no VBUS voltage is present, then the VBUSVALID threshold setting will prevent the regulator from being enabled.

For information on external capacitor requirements for this regulator, see the Hardware Development Guide for i.MX 6Quad, 6Dual, 6DualLite, 6Solo Families of Applications Processors (IMX6DQ6SDLHDG).

For additional information, see the i.MX 6Dual/6Quad reference manual (IMX6DQRM).

4.4 PLL Electrical Characteristics

4.4.1 Audio/Video PLL Electrical Parameters

Table 14. Audio/Video PLL Electrical Parameters

Parameter	Value
Clock output range	650 MHz ~1.3 GHz
Reference clock	24 MHz
Lock time	<11250 reference cycles

4.4.2 528 MHz PLL

Table 15. 528 MHz PLL Electrical Parameters

Parameter	Value
Clock output range	528 MHz PLL output
Reference clock	24 MHz
Lock time	<11250 reference cycles

4.4.3 Ethernet PLL

Table 16. Ethernet PLL Electrical Parameters

Parameter	Value
Clock output range	500 MHz
Reference clock	24 MHz
Lock time	<11250 reference cycles

4.7.2 DDR I/O AC Parameters

The LPDDR2 interface mode fully complies with JESD209-2B LPDDR2 JEDEC standard release June, 2009. The DDR3/DDR3L interface mode fully complies with JESD79-3D DDR3 JEDEC standard release April, 2008.

Table 29 shows the AC parameters for DDR I/O operating in LPDDR2 mode.

Table 29. DDR I/O LPDDR2 Mode AC Parameters[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AC input logic high	Vih(ac)	—	Vref + 0.22	—	OVDD	V
AC input logic low	Vil(ac)	—	0	—	Vref – 0.22	V
AC differential input high voltage[2]	Vidh(ac)	—	0.44	—	—	V
AC differential input low voltage	Vidl(ac)	—	—	—	0.44	V
Input AC differential cross point voltage[3]	Vix(ac)	Relative to Vref	-0.12	—	0.12	V
Over/undershoot peak	Vpeak	—	—	—	0.35	V
Over/undershoot area (above OVDD or below OVSS)	Varea	533 MHz	—	—	0.3	V-ns
Single output slew rate, measured between Vol(ac) and Voh(ac)	tsr	50 Ω to Vref. 5 pF load. Drive impedance = 4 0 Ω ±30%	1.5	—	3.5	V/ns
		50 Ω to Vref. 5pF load. Drive impedance = 60 Ω ±30%	1	—	2.5	
Skew between pad rise/fall asymmetry + skew caused by SSN	t_{SKD}	clk = 533 MHz	—	—	0.1	ns

1 Note that the JEDEC LPDDR2 specification (JESD209_2B) supersedes any specification in this document.

2 Vid(ac) specifies the input differential voltage |Vtr – Vcp| required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac) – Vil(ac).

3 The typical value of Vix(ac) is expected to be about 0.5 × OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

Table 30 shows the AC parameters for DDR I/O operating in DDR3/DDR3L mode.

Table 30. DDR I/O DDR3/DDR3L Mode AC Parameters[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AC input logic high	Vih(ac)	—	Vref + 0.175	—	OVDD	V
AC input logic low	Vil(ac)	—	0	—	Vref – 0.175	V
AC differential input voltage[2]	Vid(ac)	—	0.35	—	—	V
Input AC differential cross point voltage[3]	Vix(ac)	Relative to Vref	Vref – 0.15	—	Vref + 0.15	V
Over/undershoot peak	Vpeak	—	—	—	0.4	V
Over/undershoot area (above OVDD or below OVSS)	Varea	533 MHz	—	—	0.5	V-ns

Table 40. EIM Bus Timing Parameters (continued)

ID	Parameter	Min[1]	Max[1]	Unit
WE4	Clock rise to address valid	-0.5 × t × (k+1) - 1.25	-0.5 × t × (k+1) + 2.25	ns
WE5	Clock rise to address invalid	0.5 × t × (k+1) - 1.25	0.5 × t × (k+1) + 2.25	ns
WE6	Clock rise to EIM_CSx_B valid	-0.5 × t × (k+1) - 1.25	-0.5 × t × (k+1) + 2.25	ns
WE7	Clock rise to EIM_CSx_B invalid	0.5 × t × (k+1) - 1.25	0.5 × t × (k+1) + 2.25	ns
WE8	Clock rise to EIM_WE_B valid	-0.5 × t × (k+1) - 1.25	-0.5 × t × (k+1) + 2.25	ns
WE9	Clock rise to EIM_WE_B invalid	0.5 × t × (k+1) - 1.25	0.5 × t × (k+1) + 2.25	ns
WE10	Clock rise to EIM_OE_B valid	-0.5 × t × (k+1) - 1.25	-0.5 × t × (k+1) + 2.25	ns
WE11	Clock rise to EIM_OE_B invalid	0.5 × t × (k+1) - 1.25	0.5 × t × (k+1) + 2.25	ns
WE12	Clock rise to EIM_EBx_B valid	-0.5 × t × (k+1) - 1.25	-0.5 × t × (k+1) + 2.25	ns
WE13	Clock rise to EIM_EBx_B invalid	0.5 × t × (k+1) - 1.25	0.5 × t × (k+1) + 2.25	ns
WE14	Clock rise to EIM_LBA_B valid	-0.5 × t × (k+1) - 1.25	-0.5 × t × (k+1) + 2.25	ns
WE15	Clock rise to EIM_LBA_B invalid	0.5 × t × (k+1) - 1.25	0.5 × t × (k+1) + 2.25	ns
WE16	Clock rise to output data valid	-0.5 × t × (k+1) - 1.25	-0.5 × t × (k+1) + 2.25	ns
WE17	Clock rise to output data invalid	0.5 × t × (k+1) - 1.25	0.5 × t × (k+1) + 2.25	ns
WE18	Input data setup time to clock rise	2.3	—	ns
WE19	Input data hold time from clock rise	2	—	ns
WE20	EIM_WAIT_B setup time to clock rise	2	—	ns
WE21	EIM_WAIT_B hold time from clock rise	2	—	ns

[1] k represents register setting BCD value.

[2] t is clock period (1/Freq). For 104 MHz, t = 9.165 ns.

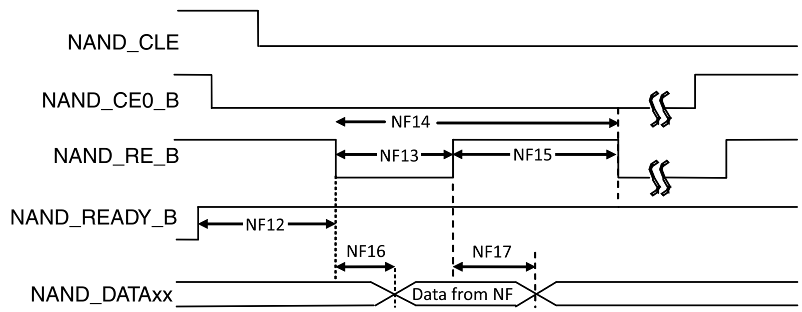

Figure 33. Read Data Latch Cycle Timing Diagram (Non-EDO Mode)

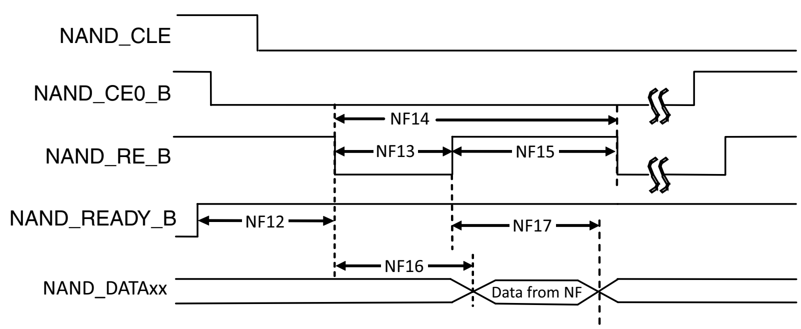

Figure 34. Read Data Latch Cycle Timing Diagram (EDO Mode)

Table 48. Asynchronous Mode Timing Parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min	Max	
NF1	NAND_CLE setup time	tCLS	(AS + DS) × T - 0.12 [see [2,3]]		ns
NF2	NAND_CLE hold time	tCLH	DH × T - 0.72 [see [2]]		ns
NF3	NAND_CEx_B setup time	tCS	(AS + DS + 1) × T [see [3,2]]		ns
NF4	NAND_CEx_B hold time	tCH	(DH+1) × T - 1 [see [2]]		ns
NF5	NAND_WE_B pulse width	tWP	DS × T [see [2]]		ns
NF6	NAND_ALE setup time	tALS	(AS + DS) × T - 0.49 [see [3,2]]		ns
NF7	NAND_ALE hold time	tALH	(DH × T - 0.42 [see [2]]		ns
NF8	Data setup time	tDS	DS × T - 0.26 [see [2]]		ns
NF9	Data hold time	tDH	DH × T - 1.37 [see [2]]		ns
NF10	Write cycle time	tWC	(DS + DH) × T [see [2]]		ns
NF11	NAND_WE_B hold time	tWH	DH × T [see [2]]		ns
NF12	Ready to NAND_RE_B low	tRR[4]	(AS + 2) × T [see [3,2]]	—	ns
NF13	NAND_RE_B pulse width	tRP	DS × T [see [2]]		ns
NF14	READ cycle time	tRC	(DS + DH) × T [see [2]]		ns
NF15	NAND_RE_B high hold time	tREH	DH × T [see [2]]		ns

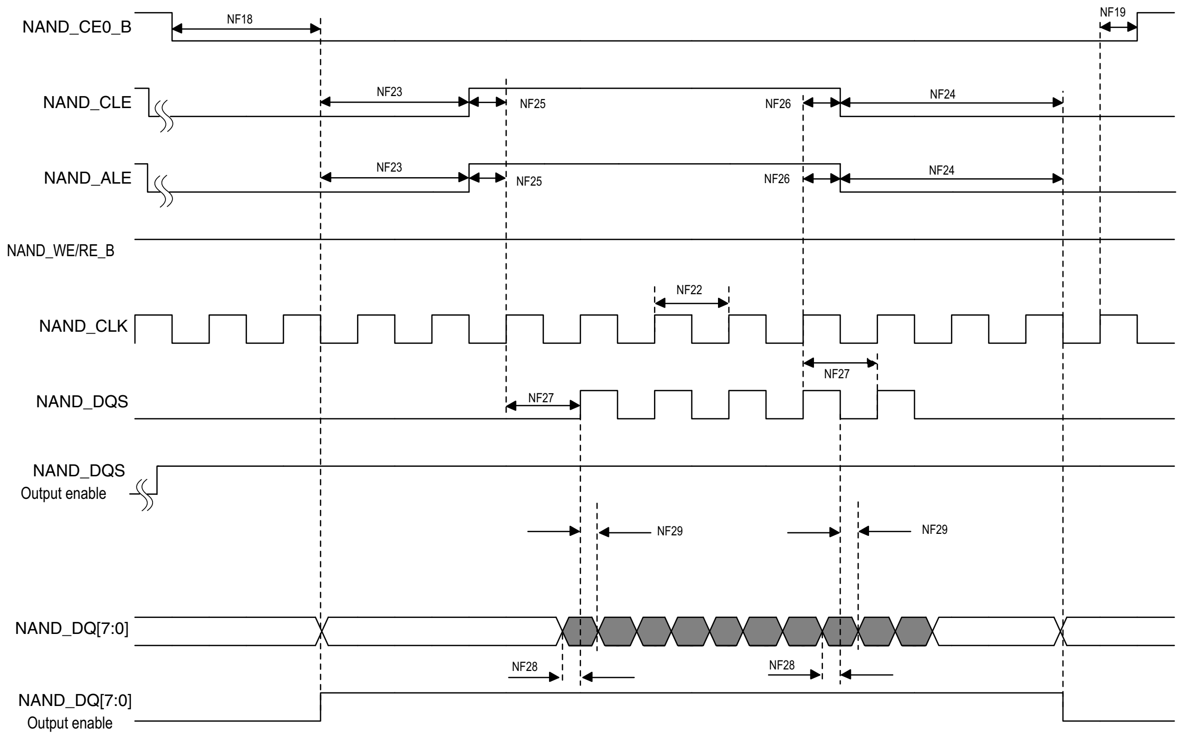

Figure 36. Source Synchronous Mode Data Write Timing Diagram

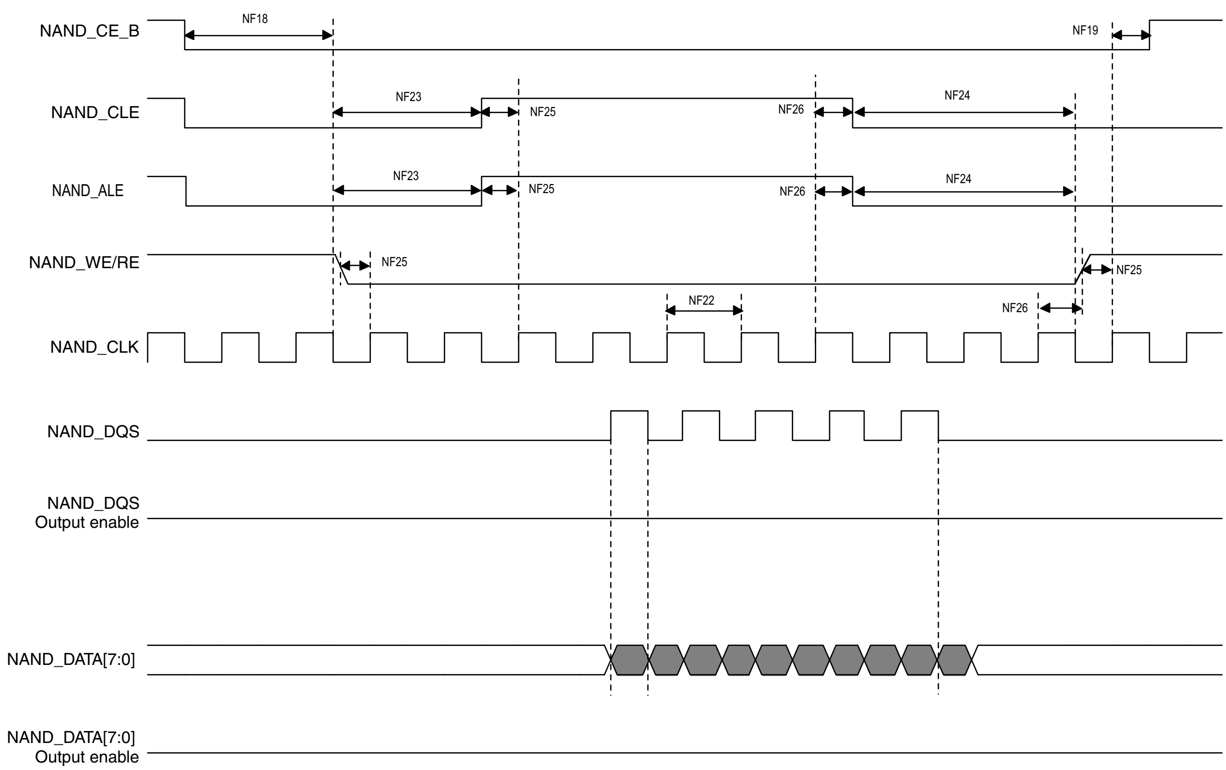

Figure 37. Source Synchronous Mode Data Read Timing Diagram

Table 50. Samsung Toggle Mode Timing Parameters[1] (continued)

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min	Max	
NF28	Data write setup	tDS[6]	0.25 × tCK - 0.32	—	ns
NF29	Data write hold	tDH[6]	0.25 × tCK - 0.79	—	ns
NF30	NAND_DQS/NAND_DQ read setup skew	tDQSQ[7]	—	3.18	—
NF31	NAND_DQS/NAND_DQ read hold skew	tQHS[7]	—	3.27	—

1 The GPMI toggle mode output timing can be controlled by the module's internal registers HW_GPMI_TIMING0_ADDRESS_SETUP, HW_GPMI_TIMING0_DATA_SETUP, and HW_GPMI_TIMING0_DATA_HOLD. This AC timing depends on these registers settings. In the table, AS/DS/DH represents each of these settings.

2 AS minimum value can be 0, while DS/DH minimum value is 1.

3 T = tCK (GPMI clock period) -0.075ns (half of maximum p-p jitter).

4 CE_DELAY represents HW_GPMI_TIMING2[CE_DELAY]. NF18 is met automatically by the design. Read/Write operation is started with enough time of ALE/CLE assertion to low level.

5 PRE_DELAY+1) ≥ (AS+DS)

6 Shown in Figure 36.

7 Shown in Figure 37.

Figure 38 shows the timing diagram of NAND_DQS/NAND_DATAxx read valid window. For DDR Toggle mode, the typical value of tDQSQ is 1.4 ns (max) and 1.4 ns (max) for tQHS at 133 MB/s. GPMI will sample NAND_DATA[7:0] at both rising and falling edge of a delayed NAND_DQS signal, which is provided by an internal DPLL. The delay value of this register can be controlled by GPMI register GPMI_READ_DDR_DLL_CTRL.SLV_DLY_TARGET (see the GPMI chapter of the i.MX 6Dual/6Quad reference manual (IMX6DQRM)). Generally, the typical delay value is equal to 0x7 which means 1/4 clock cycle delay expected. However, if the board delay is large enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

4.11 External Peripheral Interface Parameters

The following subsections provide information on external peripheral interfaces.

4.11.1 AUDMUX Timing Parameters

The AUDMUX provides a programmable interconnect logic for voice, audio, and data routing between internal serial interfaces (SSIs) and external serial interfaces (audio and voice codecs). The AC timing of AUDMUX external pins is governed by the SSI module. For more information, see the respective SSI electrical specifications found within this document.

4.11.2 ECSPI Timing Parameters

This section describes the timing parameters of the ECSPI block. The ECSPI has separate timing parameters for master and slave modes.

4.11.4 Ultra High Speed SD/SDIO/MMC Host Interface (uSDHC) AC Timing

This section describes the electrical information of the uSDHC, which includes SD/eMMC4.3 (Single Data Rate) timing and eMMC4.4/4.1 (Dual Date Rate) timing.

4.11.4.1 SD/eMMC4.3 (Single Data Rate) AC Timing

Figure 45 depicts the timing of SD/eMMC4.3, and Table 54 lists the SD/eMMC4.3 timing characteristics.

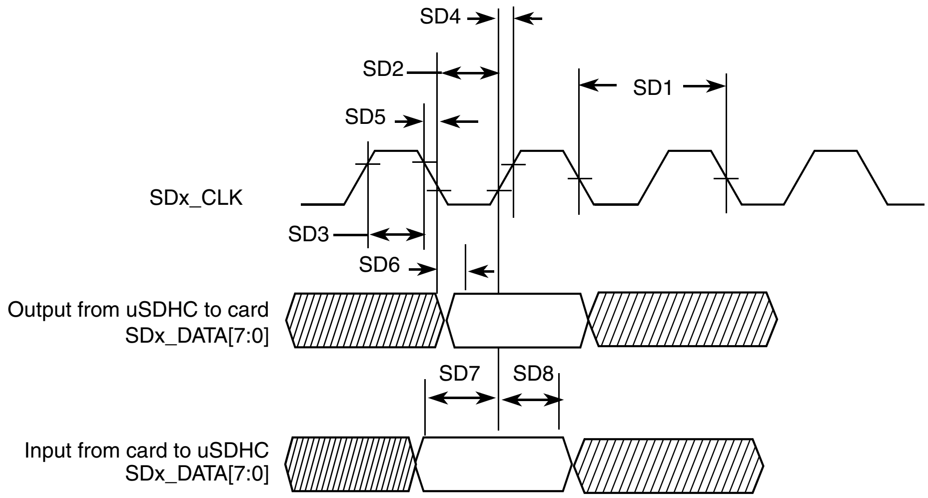

Figure 45. SD/eMMC4.3 Timing

Table 54. SD/eMMC4.3 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (Low Speed)	f_{PP}[1]	0	400	kHz
	Clock Frequency (SD/SDIO Full Speed/High Speed)	f_{PP}[2]	0	25/50	MHz
	Clock Frequency (MMC Full Speed/High Speed)	f_{PP}[3]	0	20/52	MHz
	Clock Frequency (Identification Mode)	f_{OD}	100	400	kHz
SD2	Clock Low Time	t_{WL}	7	—	ns
SD3	Clock High Time	t_{WH}	7	—	ns
SD4	Clock Rise Time	t_{TLH}	—	3	ns
SD5	Clock Fall Time	t_{THL}	—	3	ns
eSDHC Output/Card Inputs SD_CMD, SD_DATAx (Reference to SDx_CLK)					
SD6	eSDHC Output Delay	t_{OD}	–6.6	3.6	ns

4.11.4.4 Bus Operation Condition for 3.3 V and 1.8 V Signaling

Signalling level of SD/eMMC4.3 and eMMC4.4/4.41 modes is 3.3 V. Signalling level of SDR104/SDR50 mode is 1.8 V. The DC parameters for the NVCC_SD1, NVCC_SD2, and NVCC_SD3 supplies are identical to those shown in Table 22, "GPIO I/O DC Parameters," on page 39.

4.11.5 Ethernet Controller (ENET) AC Electrical Specifications

4.11.5.1 ENET MII Mode Timing

This subsection describes MII receive, transmit, asynchronous inputs, and serial management signal timings.

4.11.5.1.1 MII Receive Signal Timing (ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER, and ENET_RX_CLK)

The receiver functions correctly up to an ENET_RX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. Additionally, the processor clock frequency must exceed twice the ENET_RX_CLK frequency.

Figure 48 shows MII receive signal timings. Table 57 describes the timing parameters (M1–M4) shown in the figure.

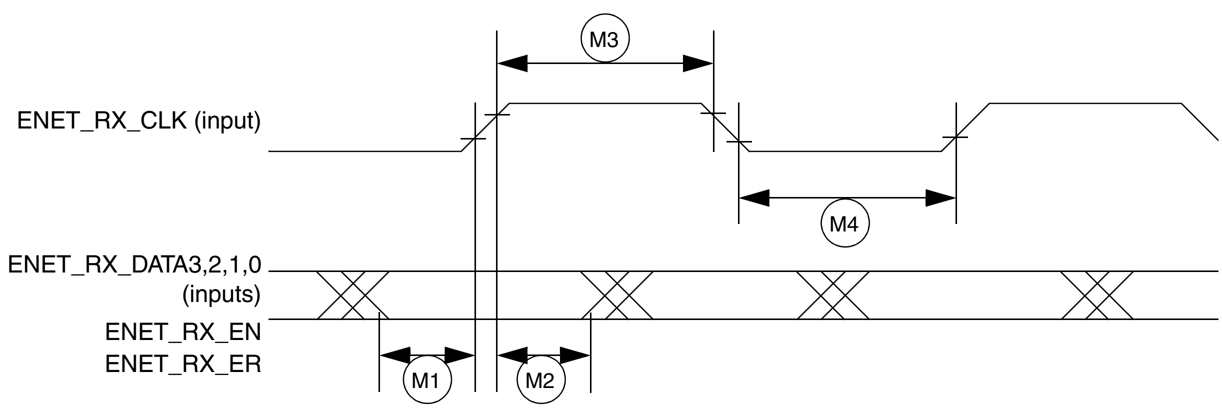

Figure 48. MII Receive Signal Timing Diagram

Table 57. MII Receive Signal Timing

ID	Characteristic[1]	Min	Max	Unit
M1	ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER to ENET_RX_CLK setup	5	—	ns
M2	ENET_RX_CLK to ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER hold	5	—	ns
M3	ENET_RX_CLK pulse width high	35%	65%	ENET_RX_CLK period
M4	ENET_RX_CLK pulse width low	35%	65%	ENET_RX_CLK period

[1] ENET_RX_EN, ENET_RX_CLK, and ENET0_RXD0 have the same timing in 10 Mbps 7-wire interface mode.

4.11.5.2 RMII Mode Timing

In RMII mode, ENET_CLK is used as the REF_CLK, which is a 50 MHz ± 50 ppm continuous reference clock. ENET_RX_EN is used as the ENET_RX_EN in RMII. Other signals under RMII mode include ENET_TX_EN, ENET0_TXD[1:0], ENET_RXD[1:0] and ENET_RX_ER.

Figure 52 shows RMII mode timings. Table 61 describes the timing parameters (M16–M21) shown in the figure.

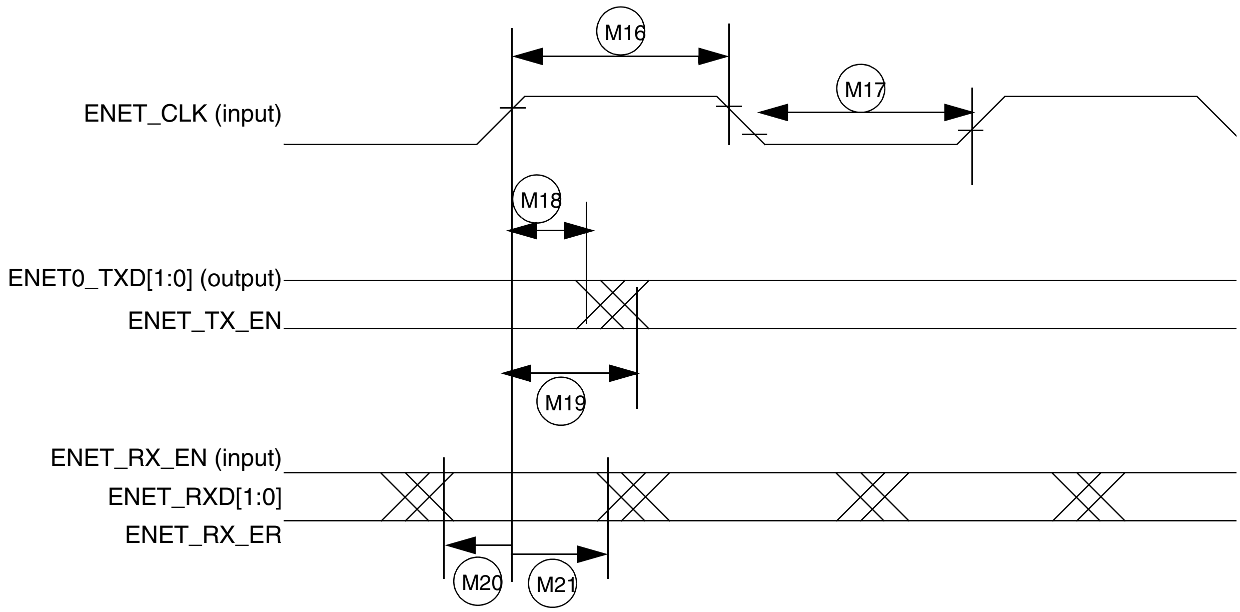

Figure 52. RMII Mode Signal Timing Diagram

Table 61. RMII Signal Timing

ID	Characteristic	Min	Max	Unit
M16	ENET_CLK pulse width high	35%	65%	ENET_CLK period
M17	ENET_CLK pulse width low	35%	65%	ENET_CLK period
M18	ENET_CLK to ENET0_TXD[1:0], ENET_TX_EN invalid	4	—	ns
M19	ENET_CLK to ENET0_TXD[1:0], ENET_TX_EN valid	—	13.5	ns
M20	ENET_RXD[1:0], ENET_RX_EN(ENET_RX_EN), ENET_RX_ER to ENET_CLK setup	4	—	ns
M21	ENET_CLK to ENET_RXD[1:0], ENET_RX_EN, ENET_RX_ER hold	2	—	ns

4.11.10.3 Electrical Characteristics

Figure 67 depicts the sensor interface timing. IPU2_CSIx_PIX_CLK signal described here is not generated by the IPU. Table 67 lists the sensor interface timing characteristics.

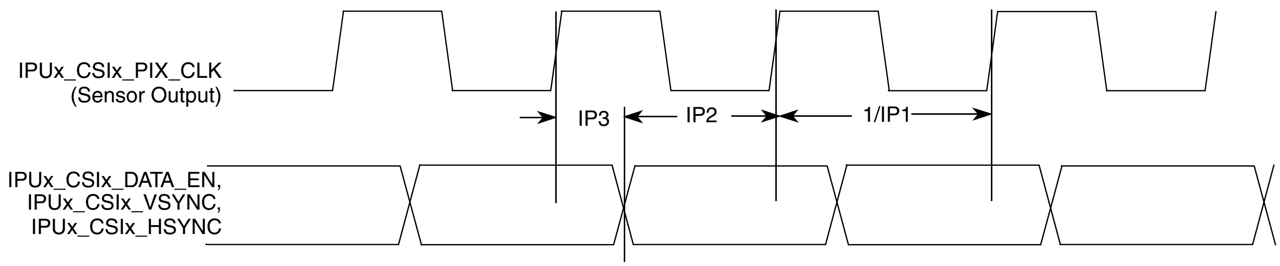

Figure 67. Sensor Interface Timing Diagram

Table 67. Sensor Interface Timing Characteristics

ID	Parameter	Symbol	Min	Max	Unit
IP1	Sensor output (pixel) clock frequency	Fpck	0.01	180	MHz
IP2	Data and control setup time	Tsu	2	—	ns
IP3	Data and control holdup time	Thd	1	—	ns

4.11.10.4 IPU Display Interface Signal Mapping

The IPU supports a number of display output video formats. Table 68 defines the mapping of the Display Interface Pins used during various supported video interface formats.

Table 68. Video Signal Cross-Reference

i.MX 6Dual/6Quad	LCD							Comment[1,2]
Port Name (x = 0, 1)	RGB, Signal Name (General)	RGB/TV Signal Allocation (Example)						
		16-bit RGB	18-bit RGB	24 Bit RGB	8-bit YCrCb[3]	16-bit YCrCb	20-bit YCrCb	
IPUx_DISPx_DAT00	DAT[0]	B[0]	B[0]	B[0]	Y/C[0]	C[0]	C[0]	—
IPUx_DISPx_DAT01	DAT[1]	B[1]	B[1]	B[1]	Y/C[1]	C[1]	C[1]	—
IPUx_DISPx_DAT02	DAT[2]	B[2]	B[2]	B[2]	Y/C[2]	C[2]	C[2]	—
IPUx_DISPx_DAT03	DAT[3]	B[3]	B[3]	B[3]	Y/C[3]	C[3]	C[3]	—
IPUx_DISPx_DAT04	DAT[4]	B[4]	B[4]	B[4]	Y/C[4]	C[4]	C[4]	—
IPUx_DISPx_DAT05	DAT[5]	G[0]	B[5]	B[5]	Y/C[5]	C[5]	C[5]	—
IPUx_DISPx_DAT06	DAT[6]	G[1]	G[0]	B[6]	Y/C[6]	C[6]	C[6]	—

- The ipp_pin_1– ipp_pin_7 are general purpose synchronous pins, that can be used to provide HSYNC, VSYNC, DRDY or any else independent signal to a display.

The IPU has a system of internal binding counters for internal events (such as, HSYNC/VSYNC) calculation. The internal event (local start point) is synchronized with internal DI_CLK. A suitable control starts from the local start point with predefined UP and DOWN values to calculate control's changing points with half DI_CLK resolution. A full description of the counter system can be found in the IPU chapter of the i.MX 6Dual/6Quad reference manual (IMX6DQRM).

4.11.10.5.2 Asynchronous Controls

The asynchronous control is a data-oriented signal that changes its value with an output data according to additional internal flags coming with the data.

There are special physical outputs to provide asynchronous controls, as follows:

- The ipp_d0_cs and ipp_d1_cs pins are dedicated to provide chip select signals to two displays.
- The ipp_pin_11– ipp_pin_17 are general purpose asynchronous pins, that can be used to provide WR. RD, RS or any other data-oriented signal to display.

NOTE

The IPU has independent signal generators for asynchronous signals toggling. When a DI decides to put a new asynchronous data on the bus, a new internal start (local start point) is generated. The signal generators calculate predefined UP and DOWN values to change pins states with half DI_CLK resolution.

4.11.10.6 Synchronous Interfaces to Standard Active Matrix TFT LCD Panels

4.11.10.6.1 IPU Display Operating Signals

The IPU uses four control signals and data to operate a standard synchronous interface:

- IPP_DISP_CLK—Clock to display
- HSYNC—Horizontal synchronization
- VSYNC—Vertical synchronization
- DRDY—Active data

All synchronous display controls are generated on the base of an internally generated "local start point". The synchronous display controls can be placed on time axis with DI's offset, up and down parameters. The display access can be whole number of DI clock (Tdiclk) only. The IPP_DATA can not be moved relative to the local start point. The data bus of the synchronous interface is output direction only.

4.11.10.6.2 LCD Interface Functional Description

Figure 68 depicts the LCD interface timing for a generic active matrix color TFT panel. In this figure, signals are shown with negative polarity. The sequence of events for active matrix interface timing is:

- DI_CLK internal DI clock is used for calculation of other controls.

Table 72. Electrical and Timing Information (continued)

Symbol	Parameters	Test Conditions	Min	Typ	Max	Unit
V_{LEAK}	Input leakage current	VGNDSH(min) = VI = VGNDSH(max) + VOH(absmax) Lane module in LP Receive Mode	-10	—	10	mA
V_{GNDSH}	Ground Shift	—	-50	—	50	mV
$V_{OH(absmax)}$	Maximum transient output voltage level	—	—	—	1.45	V
$t_{voh(absmax)}$	Maximum transient time above VOH(absmax)	—	—	—	20	ns
HS Line Drivers DC Specifications						
$\|V_{OD}\|$	HS Transmit Differential output voltage magnitude	80 Ω<= RL< = 125 Ω	140	200	270	mV
$\Delta\|V_{OD}\|$	Change in Differential output voltage magnitude between logic states	80 Ω<= RL< = 125 Ω	—	—	10	mV
V_{CMTX}	Steady-state common-mode output voltage.	80 Ω<= RL< = 125 Ω	150	200	250	mV
$\Delta V_{CMTX}(1,0)$	Changes in steady-state common-mode output voltage between logic states	80 Ω<= RL< = 125 Ω	—	—	5	mV
V_{OHHS}	HS output high voltage	80 Ω<= RL< = 125 Ω	—	—	360	mV
Z_{OS}	Single-ended output impedance.	—	40	50	62.5	Ω
ΔZ_{OS}	Single-ended output impedance mismatch.	—	—	—	10	%
LP Line Drivers DC Specifications						
V_{OL}	Output low-level SE voltage	—	-50		50	mV
V_{OH}	Output high-level SE voltage	—	1.1	1.2	1.3	V
Z_{OLP}	Single-ended output impedance.	—	110	—	—	Ω
$\Delta Z_{OLP(01-10)}$	Single-ended output impedance mismatch driving opposite level	—	—	—	20	%
$\Delta Z_{OLP(0-11)}$	Single-ended output impedance mismatch driving same level	—	—	—	5	%
HS Line Receiver DC Specifications						
V_{IDTH}	Differential input high voltage threshold	—	—	—	70	mV

Table 72. Electrical and Timing Information (continued)

Symbol	Parameters	Test Conditions	Min	Typ	Max	Unit
V_{IDTL}	Differential input low voltage threshold	—	-70	—	—	mV
V_{IHHS}	Single ended input high voltage	—	—	—	460	mV
V_{ILHS}	Single ended input low voltage	—	-40	—	—	mV
V_{CMRXDC}	Input common mode voltage	—	70	—	330	mV
Z_{ID}	Differential input impedance	—	80	—	125	Ω
LP Line Receiver DC Specifications						
V_{IL}	Input low voltage	—	—	—	550	mV
V_{IH}	Input high voltage	—	920	—	—	mV
V_{HYST}	Input hysteresis	—	25	—	—	mV
Contention Line Receiver DC Specifications						
V_{ILF}	Input low fault threshold	—	200	—	450	mV

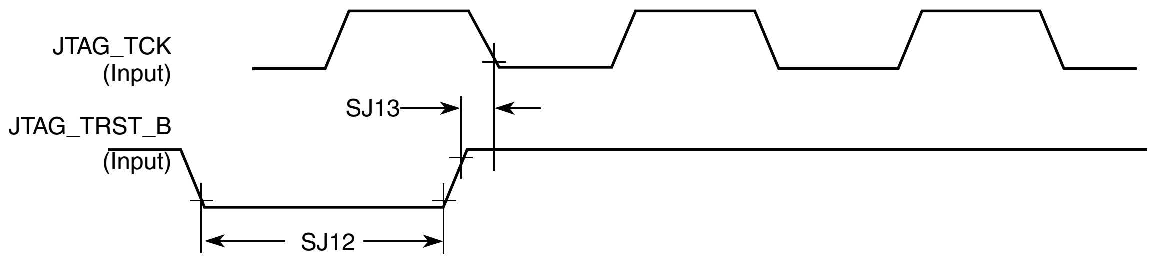

Figure 93. JTAG_TRST_B Timing Diagram

Table 83. JTAG Timing

ID	Parameter[1,2]	All Frequencies		Unit
		Min	Max	
SJ0	JTAG_TCK frequency of operation $1/(3xT_{DC})$[1]	0.001	22	MHz
SJ1	JTAG_TCK cycle time in crystal mode	45	—	ns
SJ2	JTAG_TCK clock pulse width measured at V_M[2]	22.5	—	ns
SJ3	JTAG_TCK rise and fall times	—	3	ns
SJ4	Boundary scan input data set-up time	5	—	ns
SJ5	Boundary scan input data hold time	24	—	ns
SJ6	JTAG_TCK low to output data valid	—	40	ns
SJ7	JTAG_TCK low to output high impedance	—	40	ns
SJ8	JTAG_TMS, JTAG_TDI data set-up time	5	—	ns
SJ9	JTAG_TMS, JTAG_TDI data hold time	25	—	ns
SJ10	JTAG_TCK low to JTAG_TDO data valid	—	44	ns
SJ11	JTAG_TCK low to JTAG_TDO high impedance	—	44	ns
SJ12	JTAG_TRST_B assert time	100	—	ns
SJ13	JTAG_TRST_B set-up time to JTAG_TCK low	40	—	ns

1 T_{DC} = target frequency of SJC
2 V_M = mid-point voltage

4.11.19 SPDIF Timing Parameters

The Sony/Philips Digital Interconnect Format (SPDIF) data is sent using the bi-phase marking code. When encoding, the SPDIF data signal is modulated by a clock that is twice the bit rate of the data signal.

Table 84 and Figure 94 and Figure 95 show SPDIF timing parameters for the Sony/Philips Digital Interconnect Format (SPDIF), including the timing of the modulating Rx clock (SPDIF_SR_CLK) for SPDIF in Rx mode and the timing of the modulating Tx clock (SPDIF_ST_CLK) for SPDIF in Tx mode.

Table 86. SSI Transmitter Timing with Internal Clock

ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	AUDx_TXC/AUDx_RXC clock period	81.4	—	ns
SS2	AUDx_TXC/AUDx_RXC clock high period	36.0	—	ns
SS4	AUDx_TXC/AUDx_RXC clock low period	36.0	—	ns
SS6	AUDx_TXC high to AUDx_TXFS (bl) high	—	15.0	ns
SS8	AUDx_TXC high to AUDx_TXFS (bl) low	—	15.0	ns
SS10	AUDx_TXC high to AUDx_TXFS (wl) high	—	15.0	ns
SS12	AUDx_TXC high to AUDx_TXFS (wl) low	—	15.0	ns
SS14	AUDx_TXC/AUDx_RXC Internal AUDx_TXFS rise time	—	6.0	ns
SS15	AUDx_TXC/AUDx_RXC Internal AUDx_TXFS fall time	—	6.0	ns
SS16	AUDx_TXC high to AUDx_TXD valid from high impedance	—	15.0	ns
SS17	AUDx_TXC high to AUDx_TXD high/low	—	15.0	ns
SS18	AUDx_TXC high to AUDx_TXD high impedance	—	15.0	ns
Synchronous Internal Clock Operation				
SS42	AUDx_RXD setup before AUDx_TXC falling	10.0	—	ns
SS43	AUDx_RXD hold after AUDx_TXC falling	0.0	—	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal AUDx_TXC/AUDx_RXC and/or the frame sync AUDx_TXFS/AUDx_RXFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- The terms, WL and BL, refer to Word Length(WL) and Bit Length(BL).
- For internal Frame Sync operation using external clock, the frame sync timing is the same as that of transmit data (for example, during AC97 mode of operation).

4.11.22 USB HSIC Timings

This section describes the electrical information of the USB HSIC port.

NOTE

HSIC is a DDR signal. The following timing specification is for both rising and falling edges.

4.11.22.1 Transmit Timing

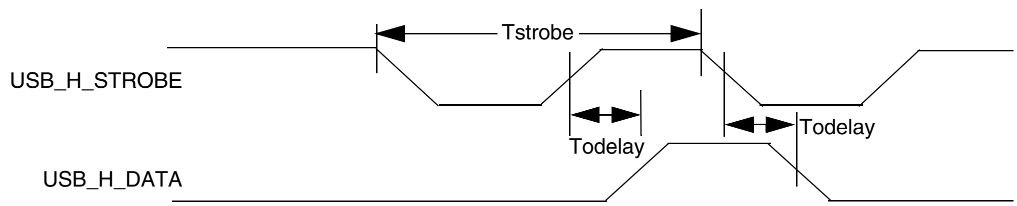

Figure 104. USB HSIC Transmit Waveform

Table 95. USB HSIC Transmit Parameters

Name	Parameter	Min	Max	Unit	Comment
Tstrobe	strobe period	4.166	4.167	ns	—
Todelay	data output delay time	550	1350	ps	Measured at 50% point
Tslew	strobe/data rising/falling time	0.7	2	V/ns	Averaged from 30% – 70% points

4.11.22.2 Receive Timing

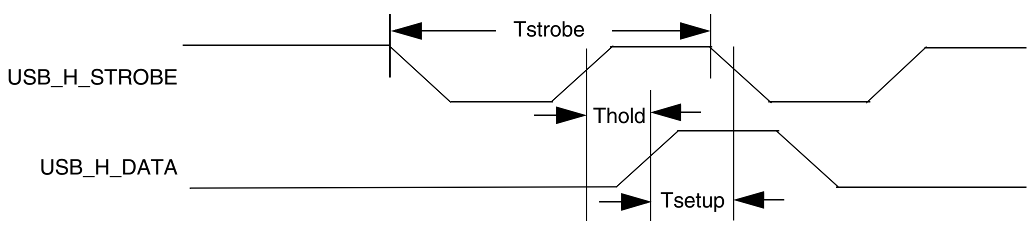

Figure 105. USB HSIC Receive Waveform

Table 96. USB HSIC Receive Parameters[1]

Name	Parameter	Min	Max	Unit	Comment
Tstrobe	strobe period	4.166	4.167	ns	—
Thold	data hold time	300	—	ps	Measured at 50% point
Tsetup	data setup time	365	—	ps	Measured at 50% point
Tslew	strobe/data rising/falling time	0.7	2	V/ns	Averaged from 30% – 70% points

[1] The timings in the table are guaranteed when:
—AC I/O voltage is between 0.9x to 1x of the I/O supply
—DDR_SEL configuration bits of the I/O are set to (10)b

Table 97. Fuses and Associated Pins Used for Boot (continued)

Pin	Direction at Reset	eFuse Name
EIM_A18	Input	BOOT_CFG3[2]
EIM_A19	Input	BOOT_CFG3[3]
EIM_A20	Input	BOOT_CFG3[4]
EIM_A21	Input	BOOT_CFG3[5]
EIM_A22	Input	BOOT_CFG3[6]
EIM_A23	Input	BOOT_CFG3[7]
EIM_A24	Input	BOOT_CFG4[0]
EIM_WAIT	Input	BOOT_CFG4[1]
EIM_LBA	Input	BOOT_CFG4[2]
EIM_EB0	Input	BOOT_CFG4[3]
EIM_EB1	Input	BOOT_CFG4[4]
EIM_RW	Input	BOOT_CFG4[5]
EIM_EB2	Input	BOOT_CFG4[6]
EIM_EB3	Input	BOOT_CFG4[7]

[1] Pin value overrides fuse settings for BT_FUSE_SEL = ‘0’. Signal Configuration as Fuse Override Input at Power Up. These are special I/O lines that control the boot up configuration during product development. In production, the boot configuration can be controlled by fuses.

5.2 Boot Devices Interfaces Allocation

Table 98 lists the interfaces that can be used by the boot process in accordance with the specific boot mode configuration. The table also describes the interface’s specific modes and IOMUXC allocation, which are configured during boot when appropriate.

Table 98. Interfaces Allocation During Boot

Interface	IP Instance	Allocated Pads During Boot	Comment
SPI	ECSPI-1	EIM_D17, EIM_D18, EIM_D16, EIM_EB2, EIM_D19, EIM_D24, EIM_D25	—
SPI	ECSPI-2	CSI0_DAT10, CSI0_DAT9, CSI0_DAT8, CSI0_DAT11, EIM_LBA, EIM_D24, EIM_D25	—
SPI	ECSPI-3	DISP0_DAT2, DISP0_DAT1, DISP0_DAT0, DISP0_DAT3, DISP0_DAT4, DISP0_DAT5, DISP0_DAT6	—
SPI	ECSPI-4	EIM_D22, EIM_D28, EIM_D21, EIM_D20, EIM_A25, EIM_D24, EIM_D25	—
SPI	ECSPI-5	SD1_DAT0, SD1_CMD, SD1_CLK, SD1_DAT1, SD1_DAT2, SD1_DAT3, SD2_DAT3	—
EIM	EIM	EIM_DA[15:0], EIM_D[31:16], CSI0_DAT[19:4], CSI0_DATA_EN, CSI0_VSYNC	Used for NOR, OneNAND boot Only CS0 is supported

Table 99. 21 x 21 mm Supplies Contact Assignment (continued)

Supply Rail Name	Ball(s) Position(s)	Remark
VDDHIGH_CAP	H10, J10	Secondary supply for the 2.5 V domain (internal regulator output—requires capacitor if internal regulator is used)
VDDHIGH_IN	H9, J9	Primary supply for the 2.5 V regulator
VDDPU_CAP	H17, J17, K17, L17, M17, N17, P17	Secondary supply for the VPU and GPU (internal regulator output—requires capacitor if internal regulator is used)
VDDSOC_CAP	R10, T10, T13, T14, U10, U13, U14	Secondary supply for the SoC and PU (internal regulator output—requires capacitor if internal regulator is used)
VDDSOC_IN	H16, J16, K16, L16, M16, N16, P16, R16, T16, U16	Primary supply for the SoC and PU regulators
VDDUSB_CAP	F9	Secondary supply for the 3 V domain (internal regulator output—requires capacitor if internal regulator is used)
ZQPAD	AE17	—

Table 100 displays an alpha-sorted list of the signal assignments including power rails. The table also includes out of reset pad state.

Table 100. 21 x 21 mm Functional Contact Assignments

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function (Signal Name)	Input/Output	Value[2]
BOOT_MODE0	C12	VDD_SNVS_IN	GPIO	ALT0	SRC_BOOT_MODE0	Input	PD (100K)
BOOT_MODE1	F12	VDD_SNVS_IN	GPIO	ALT0	SRC_BOOT_MODE1	Input	PD (100K)
CLK1_N	C7	VDD_HIGH_CAP	—	—	CLK1_N	—	—
CLK1_P	D7	VDD_HIGH_CAP	—	—	CLK1_P	—	—
CLK2_N	C5	VDD_HIGH_CAP	—	—	CLK2_N	—	—
CLK2_P	D5	VDD_HIGH_CAP	—	—	CLK2_P	—	—
CSI_CLK0M	F4	NVCC_MIPI	—	—	CSI_CLK_N	—	—
CSI_CLK0P	F3	NVCC_MIPI	—	—	CSI_CLK_P	—	—
CSI_D0M	E4	NVCC_MIPI	—	—	CSI_DATA0_N	—	—
CSI_D0P	E3	NVCC_MIPI	—	—	CSI_DATA0_P	—	—
CSI_D1M	D1	NVCC_MIPI	—	—	CSI_DATA1_N	—	—
CSI_D1P	D2	NVCC_MIPI	—	—	CSI_DATA1_P	—	—
CSI_D2M	E1	NVCC_MIPI	—	—	CSI_DATA2_N	—	—
CSI_D2P	E2	NVCC_MIPI	—	—	CSI_DATA2_P	—	—
CSI_D3M	F2	NVCC_MIPI	—	—	CSI_DATA3_N	—	—

Table 100. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function (Signal Name)	Input/Output	Value[2]
PCIE_TXM	A3	PCIE_VPH	—	—	PCIE_TX_N	—	—
PCIE_TXP	B3	PCIE_VPH	—	—	PCIE_TX_P	—	—
PMIC_ON_REQ	D11	VDD_SNVS_IN	GPIO	ALT0	SNVS_PMIC_ON_REQ	Output	Open Drain with PU (100K)
PMIC_STBY_REQ	F11	VDD_SNVS_IN	GPIO	ALT0	CCM_PMIC_STBY_REQ	Output	0
POR_B	C11	VDD_SNVS_IN	GPIO	ALT0	SRC_POR_B	Input	PU (100K)
RGMII_RD0	C24	NVCC_RGMII	DDR	ALT5	GPIO6_IO25	Input	PU (100K)
RGMII_RD1	B23	NVCC_RGMII	DDR	ALT5	GPIO6_IO27	Input	PU (100K)
RGMII_RD2	B24	NVCC_RGMII	DDR	ALT5	GPIO6_IO28	Input	PU (100K)
RGMII_RD3	D23	NVCC_RGMII	DDR	ALT5	GPIO6_IO29	Input	PU (100K)
RGMII_RX_CTL	D22	NVCC_RGMII	DDR	ALT5	GPIO6_IO24	Input	PD (100K)
RGMII_RXC	B25	NVCC_RGMII	DDR	ALT5	GPIO6_IO30	Input	PD (100K)
RGMII_TD0	C22	NVCC_RGMII	DDR	ALT5	GPIO6_IO20	Input	PU (100K)
RGMII_TD1	F20	NVCC_RGMII	DDR	ALT5	GPIO6_IO21	Input	PU (100K)
RGMII_TD2	E21	NVCC_RGMII	DDR	ALT5	GPIO6_IO22	Input	PU (100K)
RGMII_TD3	A24	NVCC_RGMII	DDR	ALT5	GPIO6_IO23	Input	PU (100K)
RGMII_TX_CTL	C23	NVCC_RGMII	DDR	ALT5	GPIO6_IO26	Input	PD (100K)
RGMII_TXC	D21	NVCC_RGMII	DDR	ALT5	GPIO6_IO19	Input	PD (100K)
RTC_XTALI	D9	VDD_SNVS_CAP	—	—	RTC_XTALI	—	—
RTC_XTALO	C9	VDD_SNVS_CAP	—	—	RTC_XTALO	—	—
SATA_RXM	A14	SATA_VPH	—	—	SATA_PHY_RX_N	—	—
SATA_RXP	B14	SATA_VPH	—	—	SATA_PHY_RX_P	—	—
SATA_TXM	B12	SATA_VPH	—	—	SATA_PHY_TX_N	—	—
SATA_TXP	A12	SATA_VPH	—	—	SATA_PHY_TX_P	—	—
SD1_CLK	D20	NVCC_SD1	GPIO	ALT5	GPIO1_IO20	Input	PU (100K)
SD1_CMD	B21	NVCC_SD1	GPIO	ALT5	GPIO1_IO18	Input	PU (100K)
SD1_DAT0	A21	NVCC_SD1	GPIO	ALT5	GPIO1_IO16	Input	PU (100K)
SD1_DAT1	C20	NVCC_SD1	GPIO	ALT5	GPIO1_IO17	Input	PU (100K)
SD1_DAT2	E19	NVCC_SD1	GPIO	ALT5	GPIO1_IO19	Input	PU (100K)
SD1_DAT3	F18	NVCC_SD1	GPIO	ALT5	GPIO1_IO21	Input	PU (100K)
SD2_CLK	C21	NVCC_SD2	GPIO	ALT5	GPIO1_IO10	Input	PU (100K)
SD2_CMD	F19	NVCC_SD2	GPIO	ALT5	GPIO1_IO11	Input	PU (100K)
SD2_DAT0	A22	NVCC_SD2	GPIO	ALT5	GPIO1_IO15	Input	PU (100K)
SD2_DAT1	E20	NVCC_SD2	GPIO	ALT5	GPIO1_IO14	Input	PU (100K)
SD2_DAT2	A23	NVCC_SD2	GPIO	ALT5	GPIO1_IO13	Input	PU (100K)
SD2_DAT3	B22	NVCC_SD2	GPIO	ALT5	GPIO1_IO12	Input	PU (100K)