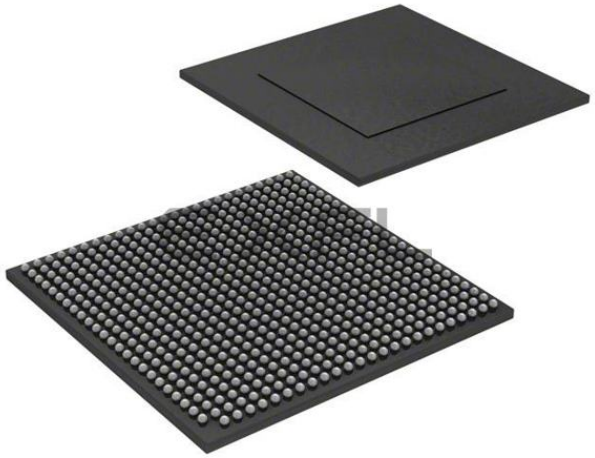

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Not For New Designs
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	4 Core, 32-Bit
Speed	852MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (1)
SATA	SATA 3Gbps (1)
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-40°C ~ 125°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	624-FBGA, FCBGA
Supplier Device Package	624-FCBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6q4avt08acr

2 Architectural Overview

The following subsections provide an architectural overview of the i.MX 6Dual/6Quad processor system.

2.1 Block Diagram

Figure 2 shows the functional modules in the i.MX 6Dual/6Quad processor system.

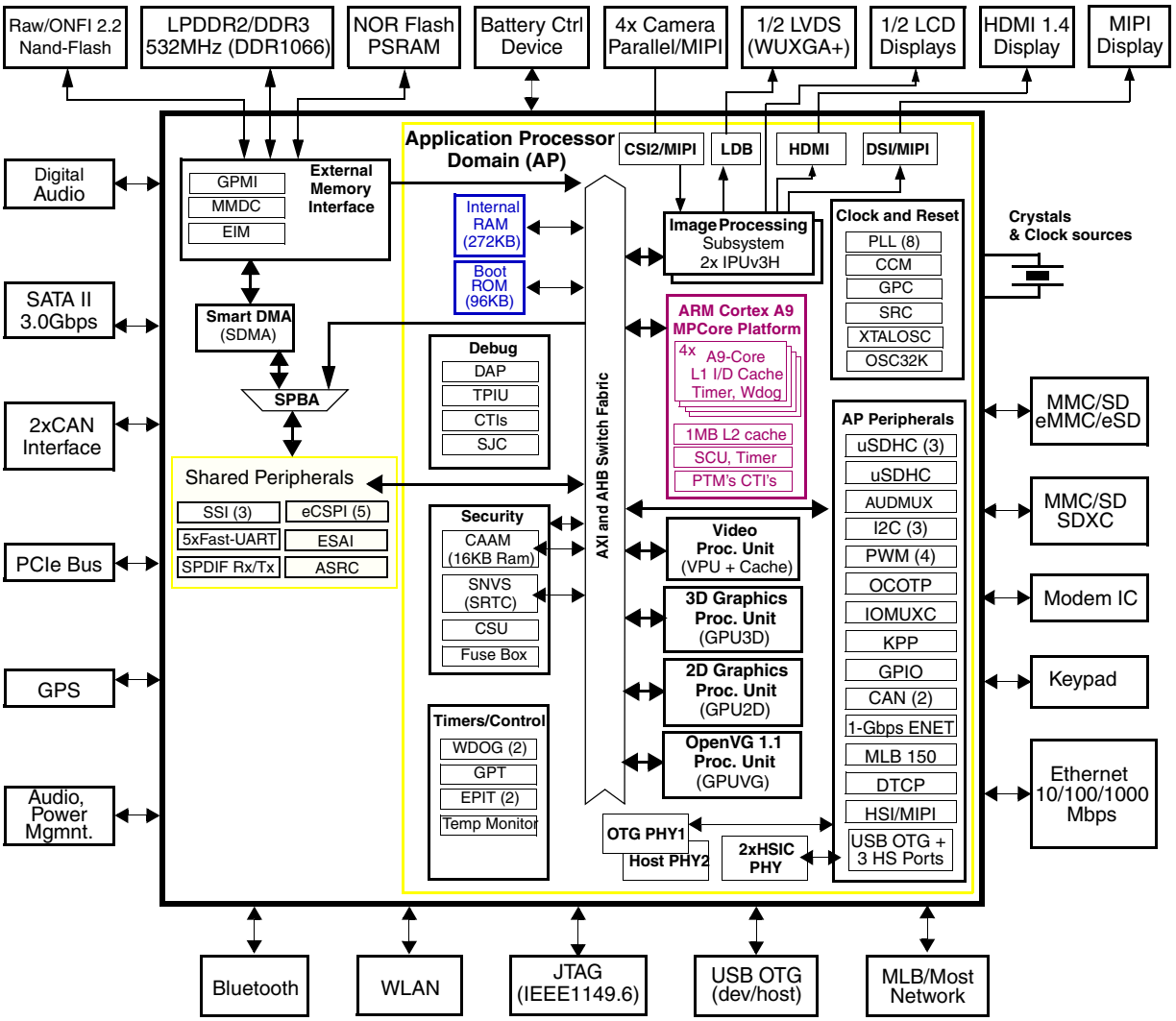


Figure 2. i.MX 6Dual/6Quad Automotive Grade System Block Diagram

NOTE

The numbers in brackets indicate number of module instances. For example, PWM (4) indicates four separate PWM peripherals.

4.6 I/O DC Parameters

This section includes the DC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2 and DDR3/DDR3L modes
- LVDS I/O
- MLB I/O

NOTE

The term ‘OVDD’ in this section refers to the associated supply rail of an input or output.

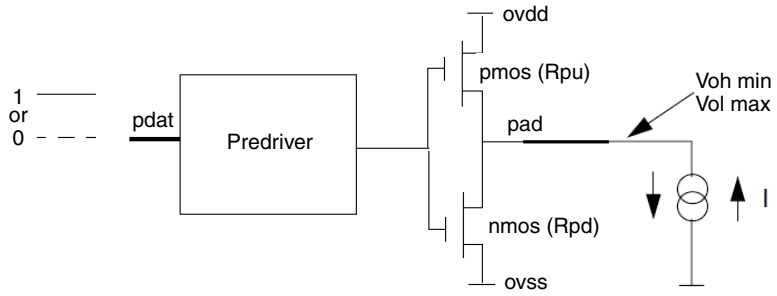


Figure 3. Circuit for Parameters Voh and Vol for I/O Cells

4.6.1 XTALI and RTC_XTALI (Clock Inputs) DC Parameters

Table 21 shows the DC parameters for the clock inputs.

Table 21. XTALI and RTC_XTALI DC Parameters

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
XTALI high-level DC input voltage	Vih	—	0.8 x NVCC_PLL_OUT	—	NVCC_PLL_ OUT	V
XTALI low-level DC input voltage	Vil	—	0	—	0.2	V
RTC_XTALI high-level DC input voltage	Vih	—	0.8	—	1.1	V
RTC_XTALI low-level DC input voltage	Vil	—	0	—	0.2	V
Input capacitance	C_{IN}	Simulated data	—	5	—	pF
Startup current	$I_{XTALI\_STARTUP}$	Power-on startup for 0.15msec with a driven 32KHz RTC clock @ 1.1V. This current draw is present even if an external clock source directly drives XTALI	—	—	600	uA
DC input current	I_{XTALI_DC}	—	—	—	2.5	uA

4.7.1 General Purpose I/O AC Parameters

The I/O AC parameters for GPIO in slow and fast modes are presented in the Table 27 and Table 28, respectively. Note that the fast or slow I/O behavior is determined by the appropriate control bits in the IOMUXC control registers.

Table 27. General Purpose I/O AC Parameters 1.8 V Mode

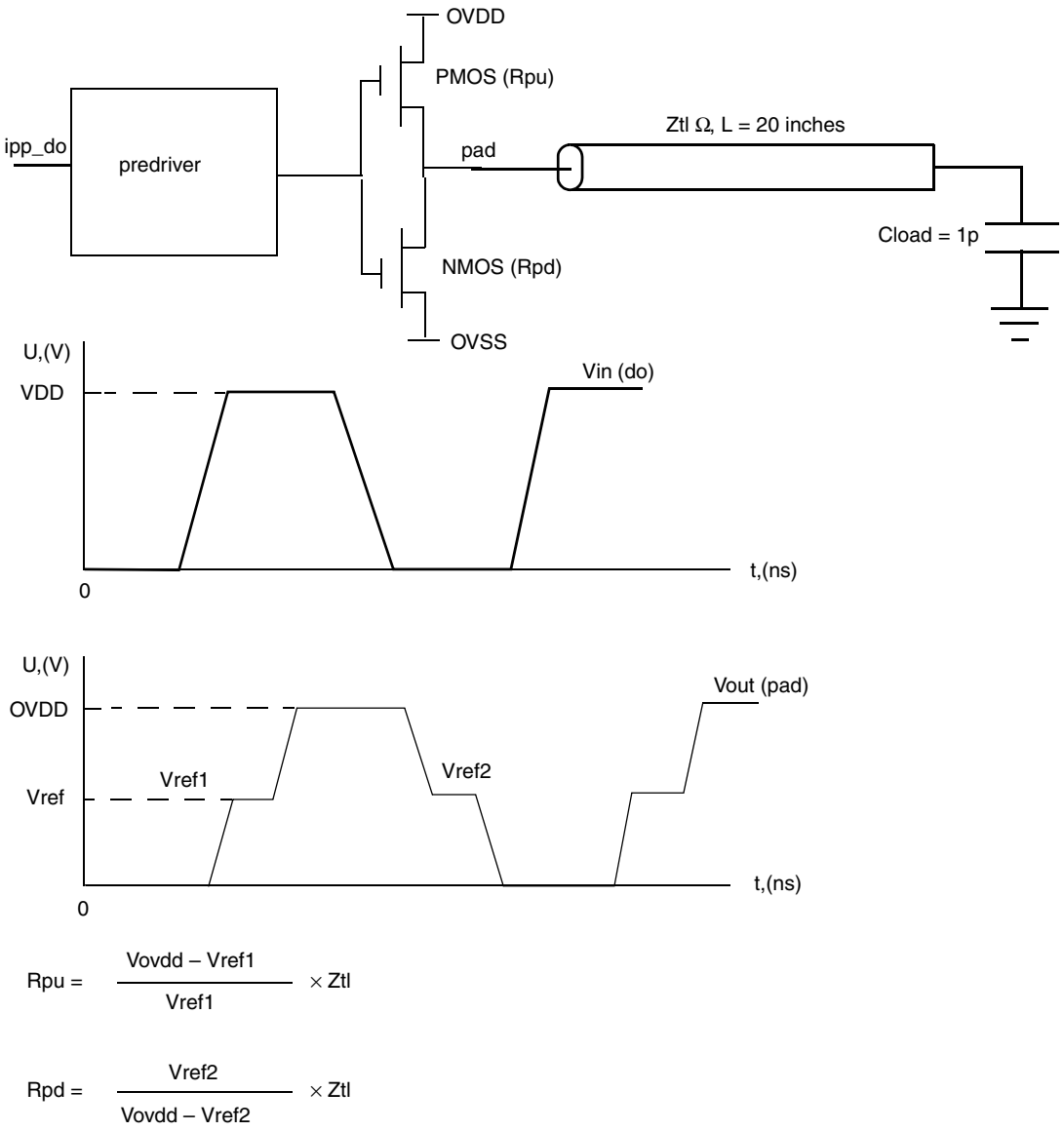
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times, rise/fall (Max Drive, ipp_dse=111)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	2.72/2.79 1.51/1.54	ns
Output Pad Transition Times, rise/fall (High Drive, ipp_dse=101)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.20/3.36 1.96/2.07	
Output Pad Transition Times, rise/fall (Medium Drive, ipp_dse=100)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.64/3.88 2.27/2.53	
Output Pad Transition Times, rise/fall (Low Drive. ipp_dse=011)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	4.32/4.50 3.16/3.17	
Input Transition Times[1]	trm	—	—	—	25	ns

1 Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

Table 28. General Purpose I/O AC Parameters 3.3 V Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times, rise/fall (Max Drive, ipp_dse=101)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	1.70/1.79 1.06/1.15	ns
Output Pad Transition Times, rise/fall (High Drive, ipp_dse=011)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	2.35/2.43 1.74/1.77	
Output Pad Transition Times, rise/fall (Medium Drive, ipp_dse=010)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.13/3.29 2.46/2.60	
Output Pad Transition Times, rise/fall (Low Drive. ipp_dse=001)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	5.14/5.57 4.77/5.15	
Input Transition Times[1]	trm	—	—	—	25	ns

1 Hysteresis mode is recommended for inputs with transition times greater than 25 ns.



$$Rpu = \frac{Vovdd - Vref1}{Vref1} \times Ztl$$

$$Rpd = \frac{Vref2}{Vovdd - Vref2} \times Ztl$$

Figure 9. Impedance Matching Load for Measurement

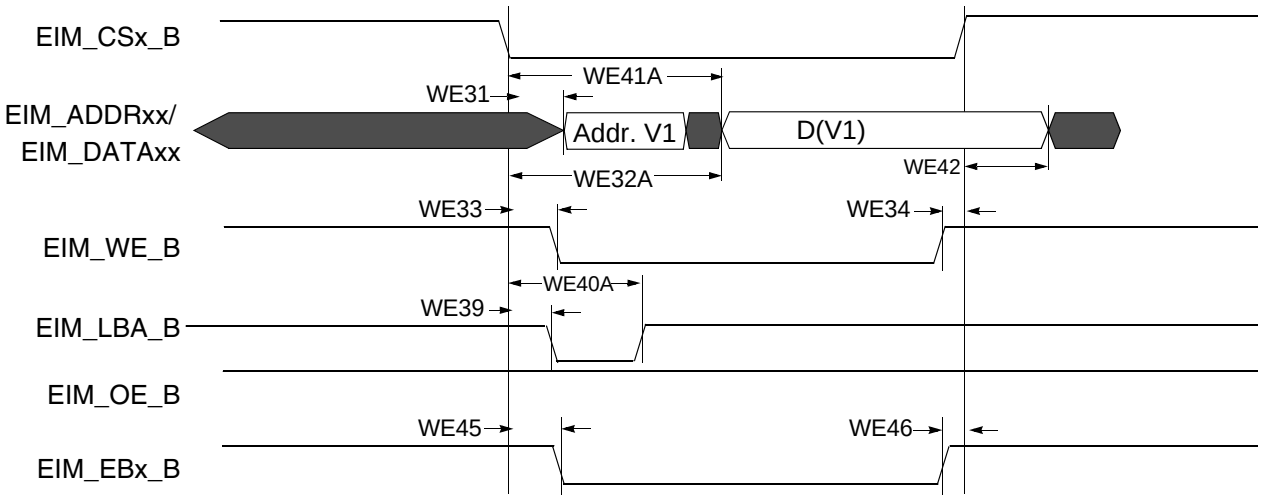


Figure 21. Asynchronous A/D Muxed Write Access

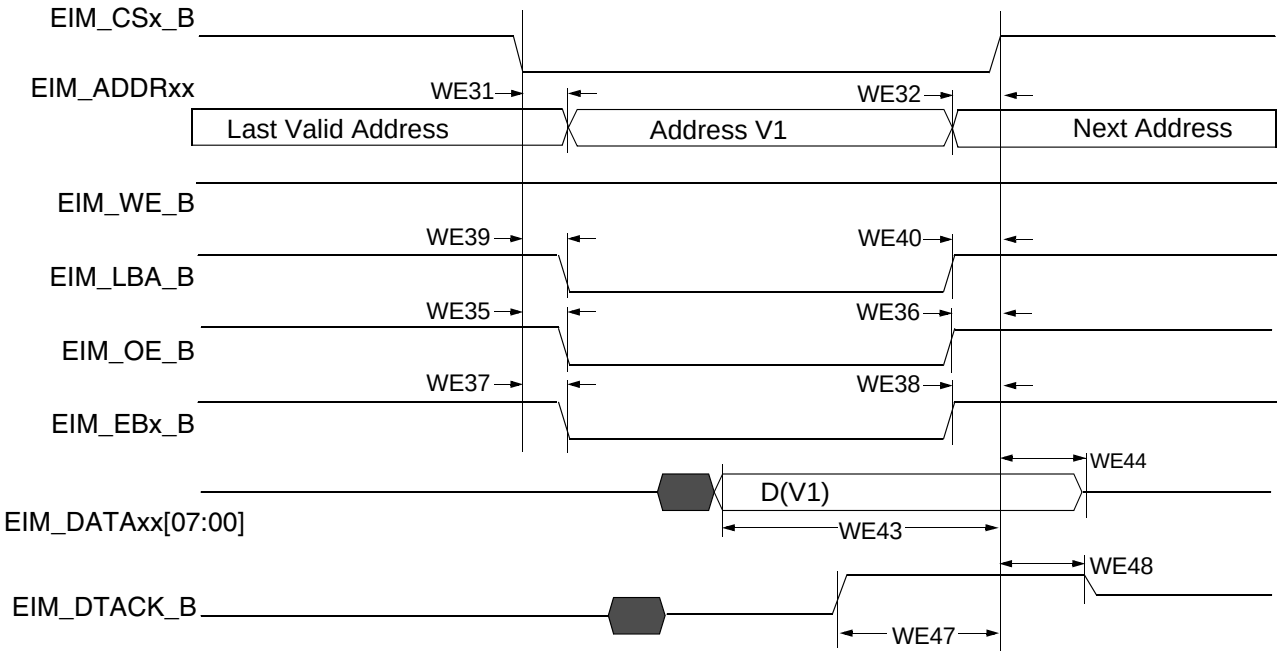


Figure 22. DTACK Mode Read Access (DAP=0)

Table 42. DDR3/DDR3L Timing Parameter (continued)

ID	Parameter[1,2]	Symbol	CK = 532 MHz		Unit
			Min	Max	
DDR4	DRAM_CSx_B, DRAM_RAS_B, DRAM_CAS_B, DRAM_SDCKEx, DRAM_SDWE_B, DRAM_ODTx setup time	tIS	500	—	ps
DDR5	DRAM_CSx_B, DRAM_RAS_B, DRAM_CAS_B, DRAM_SDCKEx, DRAM_SDWE_B, DRAM_ODTx hold time	tIH	400	—	ps
DDR6	Address output setup time	tIS	500	—	ps
DDR7	Address output hold time	tIH	400	—	ps

1 All measurements are in reference to Vref level.

2 Measurements were done using balanced load and 25 Ω resistor from outputs to DRAM_VREF.

Figure 25 shows the DDR3/DDR3L write timing diagram. The timing parameters for this diagram appear in Table 43.

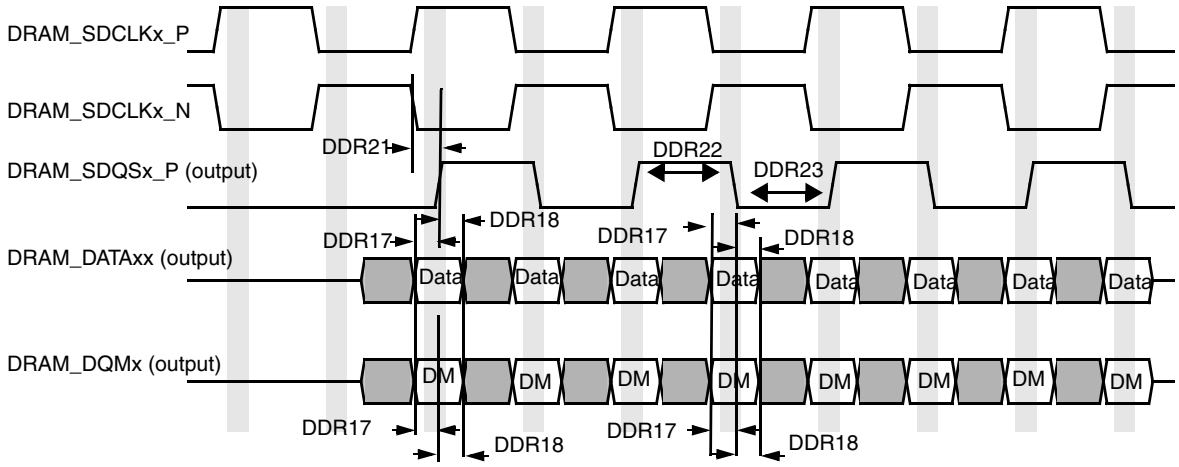


Figure 25. DDR3/DDR3L Write Cycle

Table 43. DDR3/DDR3L Write Cycle

ID	Parameter[1,2,3]	Symbol	CK = 532 MHz		Unit
			Min	Max	
DDR17	DRAM_DATAxx and DRAM_DQMx setup time to DRAM_SDQSx_P (differential strobe)	tDS	125[4]	—	ps
DDR18	DRAM_DATAxx and DRAM_DQMx hold time to DRAM_SDQSx_P (differential strobe)	tDH	150[4]	—	ps
DDR21	DRAM_SDQSx_P latching rising transitions to associated clock edges	tDQSS	-0.25	+0.25	tCK
DDR22	DRAM_SDQSx_P high level width	tDQSH	0.45	0.55	tCK
DDR23	DRAM_SDQSx_P low level width	tDQSL	0.45	0.55	tCK

1 To receive the reported setup and hold values, write calibration should be performed to locate the DRAM_SDQSx_P in the middle of DRAM_DATAxx window.

2 All measurements are in reference to Vref level.

3 Measurements were taken using balanced load and 25 Ω resistor from outputs to DRAM_VREF

4.10.1 Asynchronous Mode AC Timing (ONFI 1.0 Compatible)

Asynchronous mode AC timings are provided as multiplications of the clock cycle and fixed delay. The Maximum I/O speed of GPMI in Asynchronous mode is about 50 MB/s. Figure 30 through Figure 33 depict the relative timing between GPMI signals at the module level for different operations under Asynchronous mode. Table 48 describes the timing parameters (NF1–NF17) that are shown in the figures.

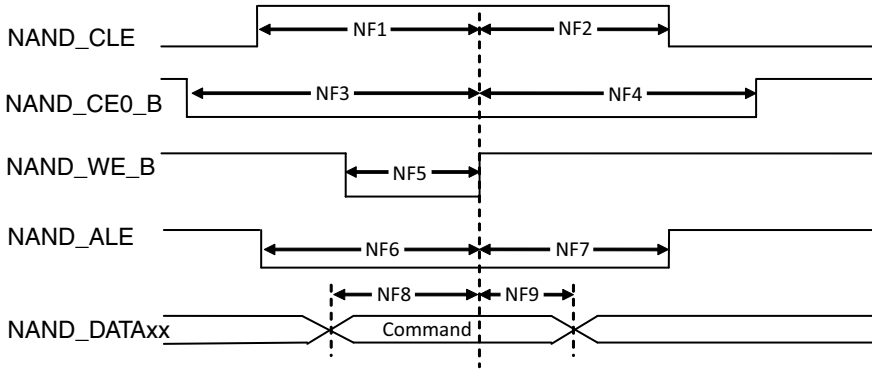


Figure 30. Command Latch Cycle Timing Diagram

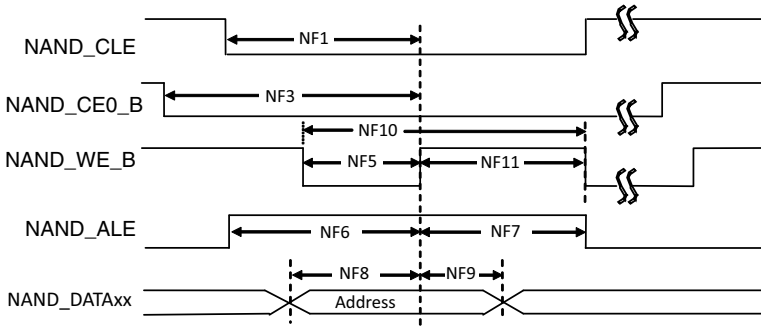


Figure 31. Address Latch Cycle Timing Diagram

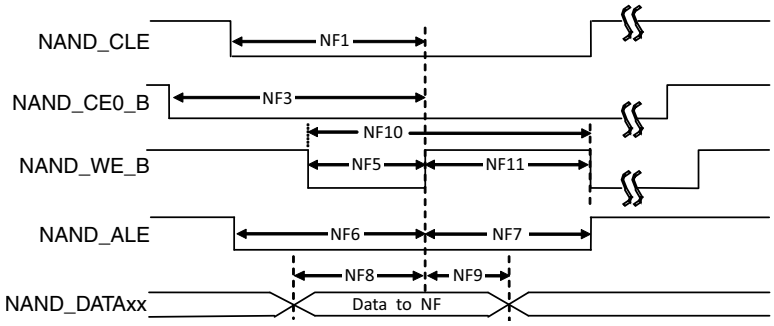


Figure 32. Write Data Latch Cycle Timing Diagram

4.11.4 Ultra High Speed SD/SDIO/MMC Host Interface (uSDHC) AC Timing

This section describes the electrical information of the uSDHC, which includes SD/eMMC4.3 (Single Data Rate) timing and eMMC4.4/4.1 (Dual Date Rate) timing.

4.11.4.1 SD/eMMC4.3 (Single Data Rate) AC Timing

Figure 45 depicts the timing of SD/eMMC4.3, and Table 54 lists the SD/eMMC4.3 timing characteristics.

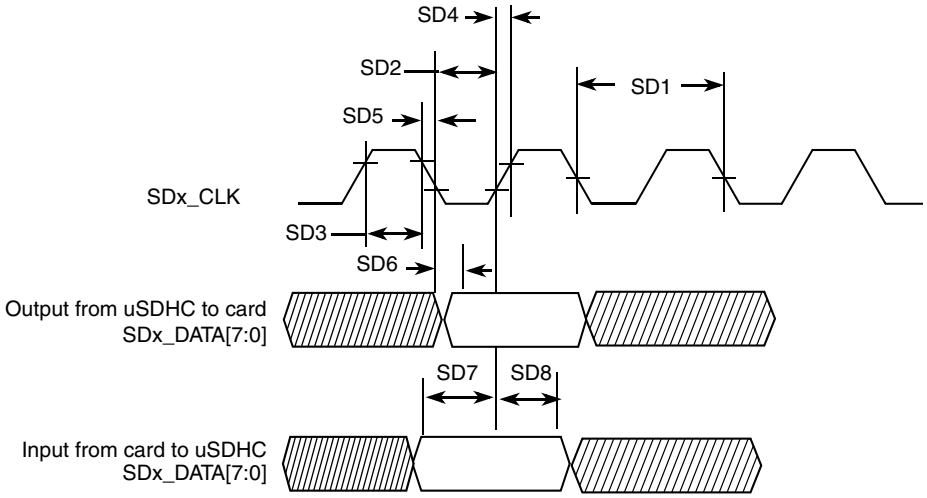


Figure 45. SD/eMMC4.3 Timing

Table 54. SD/eMMC4.3 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (Low Speed)	f_{PP}[1]	0	400	kHz
	Clock Frequency (SD/SDIO Full Speed/High Speed)	f_{PP}[2]	0	25/50	MHz
	Clock Frequency (MMC Full Speed/High Speed)	f_{PP}[3]	0	20/52	MHz
	Clock Frequency (Identification Mode)	f_{OD}	100	400	kHz
SD2	Clock Low Time	t_{WL}	7	—	ns
SD3	Clock High Time	t_{WH}	7	—	ns
SD4	Clock Rise Time	t_{TLH}	—	3	ns
SD5	Clock Fall Time	t_{THL}	—	3	ns
eSDHC Output/Card Inputs SD_CMD, SD_DATAx (Reference to SDx_CLK)					
SD6	eSDHC Output Delay	t_{OD}	–6.6	3.6	ns

Table 59. MII Asynchronous Inputs Signal Timing

ID	Characteristic	Min	Max	Unit
M9[1]	ENET_CRS to ENET_COL minimum pulse width	1.5	—	ENET_TX_CLK period

[1] ENET_COL has the same timing in 10-Mbit 7-wire interface mode.

4.11.5.1.4 MII Serial Management Channel Timing (ENET_MDIO and ENET_MDC)

The MDC frequency is designed to be equal to or less than 2.5 MHz to be compatible with the IEEE 802.3 MII specification. However the ENET can function correctly with a maximum MDC frequency of 15 MHz.

Figure 51 shows MII asynchronous input timings. Table 60 describes the timing parameters (M10–M15) shown in the figure.

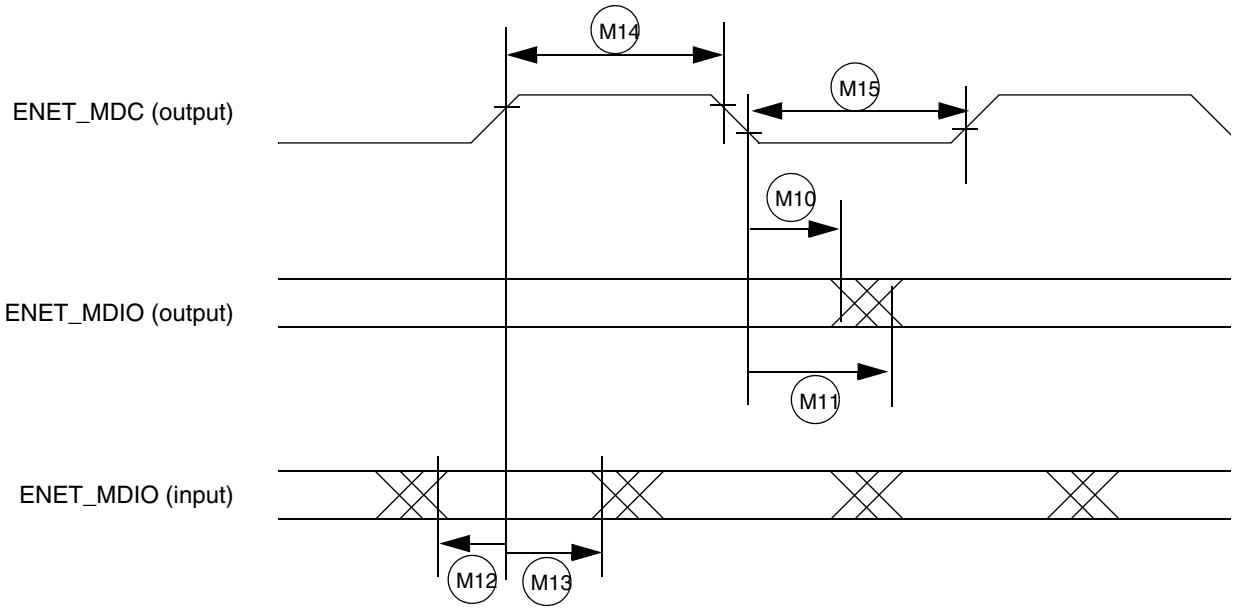


Figure 51. MII Serial Management Channel Timing Diagram

Table 60. MII Serial Management Channel Timing

ID	Characteristic	Min	Max	Unit
M10	ENET_MDC falling edge to ENET_MDIO output invalid (minimum propagation delay)	0	—	ns
M11	ENET_MDC falling edge to ENET_MDIO output valid (maximum propagation delay)	—	5	ns
M12	ENET_MDIO (input) to ENET_MDC rising edge setup	18	—	ns
M13	ENET_MDIO (input) to ENET_MDC rising edge hold	0	—	ns
M14	ENET_MDC pulse width high	40%	60%	ENET_MDC period
M15	ENET_MDC pulse width low	40%	60%	ENET_MDC period

Table 65. I²C Module Timing Parameters (continued)

ID	Parameter	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
IC9	Bus free time between a STOP and START condition	4.7	—	1.3	—	µs
IC10	Rise time of both I2Cx_SDA and I2Cx_SCL signals	—	1000	$20 + 0.1C_b$[4]	300	ns
IC11	Fall time of both I2Cx_SDA and I2Cx_SCL signals	—	300	$20 + 0.1C_b$[4]	300	ns
IC12	Capacitive load for each bus line (C_b)	—	400	—	400	pF

1 A device must internally provide a hold time of at least 300 ns for I2Cx_SDA signal to bridge the undefined region of the falling edge of I2Cx_SCL.

2 The maximum hold time has only to be met if the device does not stretch the LOW period (ID no IC5) of the I2Cx_SCL signal.

3 A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement of Set-up time (ID No IC7) of 250 ns must be met. This automatically is the case if the device does not stretch the LOW period of the I2Cx_SCL signal. If such a device does stretch the LOW period of the I2Cx_SCL signal, it must output the next data bit to the I2Cx_SDA line max_rise_time (IC9) + data_setup_time (IC7) = 1000 + 250 = 1250 ns (according to the Standard-mode I2C-bus specification) before the I2Cx_SCL line is released.

4 C_b = total capacitance of one bus line in pF.

4.11.10 Image Processing Unit (IPU) Module Parameters

The purpose of the IPU is to provide comprehensive support for the flow of data from an image sensor and/or to a display device. This support covers all aspects of these activities:

- Connectivity to relevant devices—cameras, displays, graphics accelerators, and TV encoders.
- Related image processing and manipulation: sensor image signal processing, display processing, image conversions, and other related functions.
- Synchronization and control capabilities, such as avoidance of tearing artifacts.

4.11.10.3 Electrical Characteristics

Figure 67 depicts the sensor interface timing. IPU2_CSIx_PIX_CLK signal described here is not generated by the IPU. Table 67 lists the sensor interface timing characteristics.

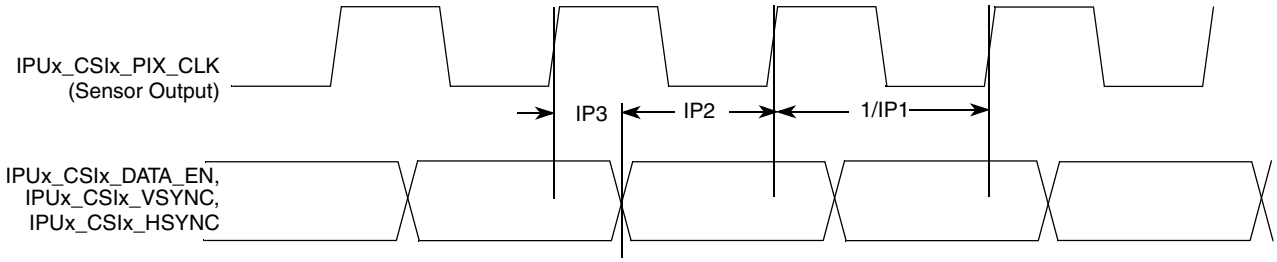


Figure 67. Sensor Interface Timing Diagram

Table 67. Sensor Interface Timing Characteristics

ID	Parameter	Symbol	Min	Max	Unit
IP1	Sensor output (pixel) clock frequency	Fpck	0.01	180	MHz
IP2	Data and control setup time	Tsu	2	—	ns
IP3	Data and control holdup time	Thd	1	—	ns

4.11.10.4 IPU Display Interface Signal Mapping

The IPU supports a number of display output video formats. Table 68 defines the mapping of the Display Interface Pins used during various supported video interface formats.

Table 68. Video Signal Cross-Reference

i.MX 6Dual/6Quad	LCD							Comment[1,2]
Port Name (x = 0, 1)	RGB, Signal Name (General)	RGB/TV Signal Allocation (Example)						
		16-bit RGB	18-bit RGB	24 Bit RGB	8-bit YCrCb[3]	16-bit YCrCb	20-bit YCrCb	
IPUx_DISPx_DAT00	DAT[0]	B[0]	B[0]	B[0]	Y/C[0]	C[0]	C[0]	—
IPUx_DISPx_DAT01	DAT[1]	B[1]	B[1]	B[1]	Y/C[1]	C[1]	C[1]	—
IPUx_DISPx_DAT02	DAT[2]	B[2]	B[2]	B[2]	Y/C[2]	C[2]	C[2]	—
IPUx_DISPx_DAT03	DAT[3]	B[3]	B[3]	B[3]	Y/C[3]	C[3]	C[3]	—
IPUx_DISPx_DAT04	DAT[4]	B[4]	B[4]	B[4]	Y/C[4]	C[4]	C[4]	—
IPUx_DISPx_DAT05	DAT[5]	G[0]	B[5]	B[5]	Y/C[5]	C[5]	C[5]	—
IPUx_DISPx_DAT06	DAT[6]	G[1]	G[0]	B[6]	Y/C[6]	C[6]	C[6]	—

Table 68. Video Signal Cross-Reference (continued)

i.MX 6Dual/6Quad	LCD							Comment[1,2]
Port Name (x = 0, 1)	RGB, Signal Name (General)	RGB/TV Signal Allocation (Example)						
		16-bit RGB	18-bit RGB	24 Bit RGB	8-bit YCrCb[3]	16-bit YCrCb	20-bit YCrCb	
IPUx_DISPx_DAT07	DAT[7]	G[2]	G[1]	B[7]	Y/C[7]	C[7]	C[7]	—
IPUx_DISPx_DAT08	DAT[8]	G[3]	G[2]	G[0]	—	Y[0]	C[8]	—
IPUx_DISPx_DAT09	DAT[9]	G[4]	G[3]	G[1]	—	Y[1]	C[9]	—
IPUx_DISPx_DAT10	DAT[10]	G[5]	G[4]	G[2]	—	Y[2]	Y[0]	—
IPUx_DISPx_DAT11	DAT[11]	R[0]	G[5]	G[3]	—	Y[3]	Y[1]	—
IPUx_DISPx_DAT12	DAT[12]	R[1]	R[0]	G[4]	—	Y[4]	Y[2]	—
IPUx_DISPx_DAT13	DAT[13]	R[2]	R[1]	G[5]	—	Y[5]	Y[3]	—
IPUx_DISPx_DAT14	DAT[14]	R[3]	R[2]	G[6]	—	Y[6]	Y[4]	—
IPUx_DISPx_DAT15	DAT[15]	R[4]	R[3]	G[7]	—	Y[7]	Y[5]	—
IPUx_DISPx_DAT16	DAT[16]	—	R[4]	R[0]	—	—	Y[6]	—
IPUx_DISPx_DAT17	DAT[17]	—	R[5]	R[1]	—	—	Y[7]	—
IPUx_DISPx_DAT18	DAT[18]	—	—	R[2]	—	—	Y[8]	—
IPUx_DISPx_DAT19	DAT[19]	—	—	R[3]	—	—	Y[9]	—
IPUx_DISPx_DAT20	DAT[20]	—	—	R[4]	—	—	—	—
IPUx_DISPx_DAT21	DAT[21]	—	—	R[5]	—	—	—	—
IPUx_DISPx_DAT22	DAT[22]	—	—	R[6]	—	—	—	—
IPUx_DISPx_DAT23	DAT[23]	—	—	R[7]	—	—	—	—
IPUx_DIx_DISP_CLK	PixCLK							—
IPUx_DIx_PIN01	—							May be required for anti-tearing
IPUx_DIx_PIN02	HSYNC							—
IPUx_DIx_PIN03	VSYNC							VSYNC out
IPUx_DIx_PIN04	—							Additional frame/row synchronous signals with programmable timing
IPUx_DIx_PIN05	—							
IPUx_DIx_PIN06	—							
IPUx_DIx_PIN07	—							
IPUx_DIx_PIN08	—							

4.11.12.9 Low-Power Receiver Timing

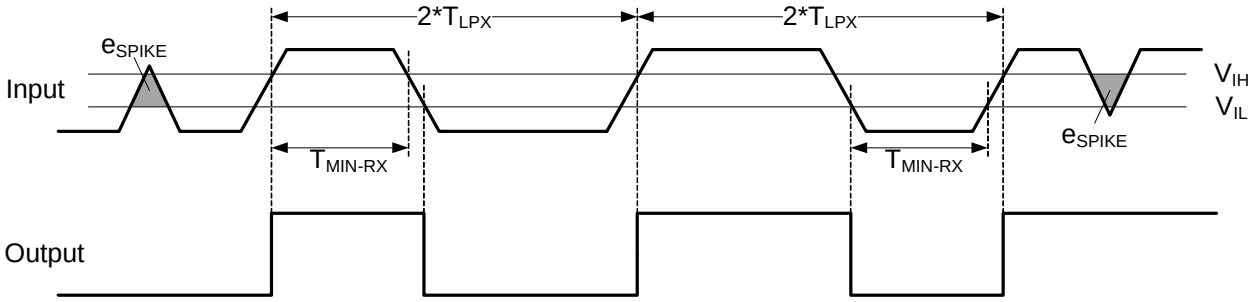


Figure 78. Input Glitch Rejection of Low-Power Receivers

4.11.13 HSI Host Controller Timing Parameters

This section describes the timing parameters of the HSI Host Controller which are compliant with High-Speed Synchronous Serial Interface (HSI) Physical Layer specification version 1.01.

4.11.13.1 Synchronous Data Flow

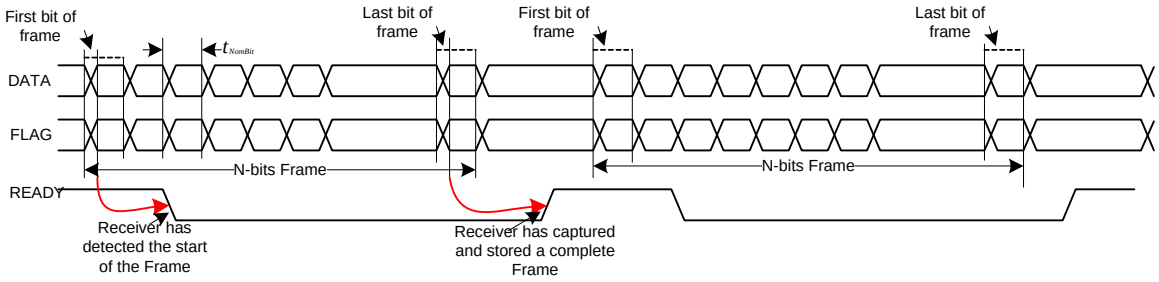


Figure 79. Synchronized Data Flow READY Signal Timing (Frame and Stream Transmission)

4.11.13.2 Pipelined Data Flow

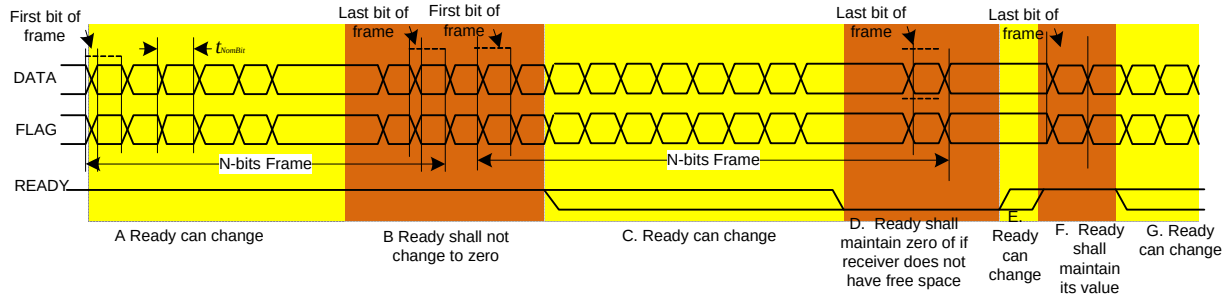


Figure 80. Pipelined Data Flow READY Signal Timing (Frame Transmission Mode)

4.11.13.9 DATA and FLAG Signal Timing

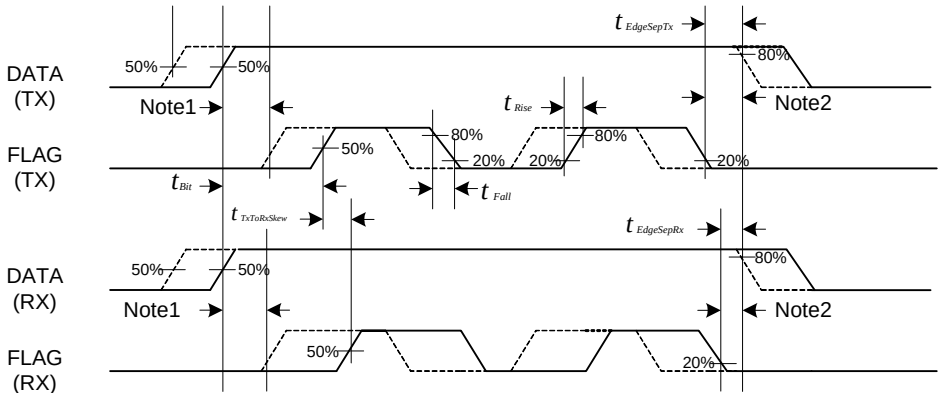


Figure 86. DATA and FLAG Signal Timing

4.11.14 MediaLB (MLB) Characteristics

4.11.14.1 MediaLB (MLB) DC Characteristics

Table 75 lists the MediaLB 3-pin interface electrical characteristics.

Table 75. MediaLB 3-Pin Interface Electrical DC Specifications

Parameter	Symbol	Test Conditions	Min	Max	Unit
Maximum input voltage	—	—	—	3.6	V
Low level input threshold	V_{IL}	—	—	0.7	V
High level input threshold	V_{IH}	See Note[1]	1.8	—	V
Low level output threshold	V_{OL}	I_{OL} = 6 mA	—	0.4	V
High level output threshold	V_{OH}	I_{OH} = –6 mA	2.0	—	V
Input leakage current	I_L	0 < V_{in} < VDD	—	±10	µA

[1] Higher V_{IH} thresholds can be used; however, the risks associated with less noise margin in the system must be evaluated and assumed by the customer.

Table 76 lists the MediaLB 6-pin interface electrical characteristics.

Table 76. MediaLB 6-Pin Interface Electrical DC Specifications

Parameter	Symbol	Test Conditions	Min	Max	Unit
Driver Characteristics					
Differential output voltage (steady-state): I V_{O+} - V_{O-} I	V_{OD}	See Note[1]	300	500	mV
Difference in differential output voltage between (high/low) steady-states: I $V_{OD, high}$ - $V_{OD, low}$ I	ΔV_{OD}	—	-50	50	mV

Table 89. SSI Receiver Timing with External Clock

ID	Parameter	Min	Max	Unit
External Clock Operation				
SS22	AUDx_TXC/AUDx_RXC clock period	81.4	—	ns
SS23	AUDx_TXC/AUDx_RXC clock high period	36	—	ns
SS24	AUDx_TXC/AUDx_RXC clock rise time	—	6.0	ns
SS25	AUDx_TXC/AUDx_RXC clock low period	36	—	ns
SS26	AUDx_TXC/AUDx_RXC clock fall time	—	6.0	ns
SS28	AUDx_RXC high to AUDx_TXFS (bl) high	–10	15.0	ns
SS30	AUDx_RXC high to AUDx_TXFS (bl) low	10	—	ns
SS32	AUDx_RXC high to AUDx_TXFS (wl) high	–10	15.0	ns
SS34	AUDx_RXC high to AUDx_TXFS (wl) low	10	—	ns
SS35	AUDx_TXC/AUDx_RXC External AUDx_TXFS rise time	—	6.0	ns
SS36	AUDx_TXC/AUDx_RXC External AUDx_TXFS fall time	—	6.0	ns
SS40	AUDx_RXD setup time before AUDx_RXC low	10	—	ns
SS41	AUDx_RXD hold time after AUDx_RXC low	2	—	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal AUDx_TXC/AUDx_RXC and/or the frame sync AUDx_TXFS/AUDx_RXFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- AUDx_TXC and AUDx_RXC refer to the Transmit and Receive sections of the SSI.
- The terms, WL and BL, refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the frame sync timing is same as that of transmit data (for example, during AC97 mode of operation).

4.11.21 UART I/O Configuration and Timing Parameters

4.11.21.1 UART RS-232 I/O Configuration in Different Modes

The i.MX 6Dual/6Quad UART interfaces can serve both as DTE or DCE device. This can be configured by the DCEDTE control bit (default 0 – DCE mode). Table 90 shows the UART I/O configuration based on the enabled mode.

Table 90. UART I/O Configuration vs. Mode

Port	DTE Mode		DCE Mode	
	Direction	Description	Direction	Description
UARTx_RTS_B	Output	RTS from DTE to DCE	Input	RTS from DTE to DCE
UARTx_CTS_B	Input	CTS from DCE to DTE	Output	CTS from DCE to DTE
UARTx_DTR_B	Output	DTR from DTE to DCE	Input	DTR from DTE to DCE
UARTx_DSR_B	Input	DSR from DCE to DTE	Output	DSR from DCE to DTE
UARTx_DCD_B	Input	DCD from DCE to DTE	Output	DCD from DCE to DTE
UARTx_RI_B	Input	RING from DCE to DTE	Output	RING from DCE to DTE
UARTx_TX_DATA	Input	Serial data from DCE to DTE	Output	Serial data from DCE to DTE
UARTx_RX_DATA	Output	Serial data from DTE to DCE	Input	Serial data from DTE to DCE

6.2.2 21 x 21 mm Ground, Power, Sense, and Reference Contact Assignments

Table 99 shows the device connection list for ground, power, sense, and reference contact signals.

Table 99. 21 x 21 mm Supplies Contact Assignment

Supply Rail Name	Ball(s) Position(s)	Remark
CSI_REXT	D4	—
DRAM_VREF	AC2	—
DSI_REXT	G4	—
FA_ANA	A5	—
GND	A13, A25, A4, A8, AA10, AA13, AA16, AA19, AA22, AD4, D3, F8, J15, L10, M15, P15, T15, U8, W17, AA7, AD7, D6, G10, J18, L12, M18, P18, T17, V19, W18, AB24, AE1, D8, G19, J2, L15, M8, P8, T19, V8, W19, AB3, AE25, E5, G3, J8, L18, N10, R12, T8, W10, W3, AD10, B4, E6, H12, K10, L2, N15, R15, U11, W11, W7, AD13, C1, E7, H15, K12, L5, N18, R17, U12, W12, W8, AD16, C10, F5, H18, K15, L8, N8, R8, U15, W13, W9, AD19, C4, F6, H8, K18, M10, P10, T11, U17, W15, Y24, AD22, C6, F7, J12, K8, M12, P12, T12, U19, W16, Y5	—
GPANAIO	C8	—
HDMI_DDCCEC	K2	Analog ground reference for the Hot Plug detect signal
HDMI_REF	J1	—
HDMI_VP	L7	—
HDMI_VPH	M7	—
NVCC_CSI	N7	Supply of the camera sensor interface
NVCC_DRAM	R18, T18, U18, V10, V11, V12, V13, V14, V15, V16, V17, V18, V9	Supply of the DDR interface
NVCC_EIM0	K19	Supply of the EIM interface
NVCC_EIM1	L19	Supply of the EIM interface
NVCC_EIM2	M19	Supply of the EIM interface
NVCC_ENET	R19	Supply of the ENET interface
NVCC_GPIO	P7	Supply of the GPIO interface
NVCC_JTAG	J7	Supply of the JTAG tap controller interface
NVCC_LCD	P19	Supply of the LCD interface
NVCC_LVDS2P5	V7	Supply of the LVDS display interface and DDR pre-drivers. Even if the LVDS interface is not used, this supply must remain powered.
NVCC_MIPI	K7	Supply of the MIPI interface

Table 99. 21 x 21 mm Supplies Contact Assignment (continued)

Supply Rail Name	Ball(s) Position(s)	Remark
NVCC_NANDF	G15	Supply of the RAW NAND Flash Memories interface
NVCC_PLL_OUT	E8	—
NVCC_RGMII	G18	Supply of the ENET interface
NVCC_SD1	G16	Supply of the SD card interface
NVCC_SD2	G17	Supply of the SD card interface
NVCC_SD3	G14	Supply of the SD card interface
PCIE_VP	H7	—
PCIE_REXT	A2	—
PCIE_VPH	G7	PCI PHY supply
PCIE_VPTX	G8	PCI PHY supply
SATA_REXT	C14	—
SATA_VP	G13	—
SATA_VPH	G12	—
USB_H1_VBUS	D10	—
USB_OTG_VBUS	E9	—
VDD_CACHE_CAP	N12	Cache supply input. This input should be connected to (driven by) VDD_SOC_CAP. The external capacitor used for VDD_SOC_CAP is sufficient for this supply.
VDD_FA	B5	—
VDD_SNVS_CAP	G9	Secondary supply for the SNVS (internal regulator output—requires capacitor if internal regulator is used)
VDD_SNVS_IN	G11	Primary supply for the SNVS regulator
VDDARM_CAP	H13, J13, K13, L13, M13, N13, P13, R13	Secondary supply for the ARM0 and ARM1 cores (internal regulator output—requires capacitor if internal regulator is used)
VDDARM_IN	H14, J14, K14, L14, M14, N14, P14, R14	Primary supply for the ARM0 and ARM1 core regulator
VDDARM23_CAP	H11, J11, K11, L11, M11, N11, P11, R11	Secondary supply for the ARM2 and ARM3 cores (internal regulator output—requires capacitor if internal regulator is used)
VDDARM23_IN	K9, L9, M9, N9, P9, R9, T9, U9	Primary supply for the ARM2 and ARM3 core regulator

Table 100. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function (Signal Name)	Input/Output	Value[2]
EIM_DA10	M22	NVCC_EIM2	GPIO	ALT0	EIM_AD10	Input	PU (100K)
EIM_DA11	M20	NVCC_EIM2	GPIO	ALT0	EIM_AD11	Input	PU (100K)
EIM_DA12	M24	NVCC_EIM2	GPIO	ALT0	EIM_AD12	Input	PU (100K)
EIM_DA13	M23	NVCC_EIM2	GPIO	ALT0	EIM_AD13	Input	PU (100K)
EIM_DA14	N23	NVCC_EIM2	GPIO	ALT0	EIM_AD14	Input	PU (100K)
EIM_DA15	N24	NVCC_EIM2	GPIO	ALT0	EIM_AD15	Input	PU (100K)
EIM_EB0	K21	NVCC_EIM2	GPIO	ALT0	EIM_EB0_B	Output	1
EIM_EB1	K23	NVCC_EIM2	GPIO	ALT0	EIM_EB1_B	Output	1
EIM_EB2	E22	NVCC_EIM0	GPIO	ALT5	GPIO2_IO30	Input	PU (100K)
EIM_EB3	F23	NVCC_EIM0	GPIO	ALT5	GPIO2_IO31	Input	PU (100K)
EIM_LBA	K22	NVCC_EIM1	GPIO	ALT0	EIM_LBA_B	Output	1
EIM_OE	J24	NVCC_EIM1	GPIO	ALT0	EIM_OE	Output	1
EIM_RW	K20	NVCC_EIM1	GPIO	ALT0	EIM_RW	Output	1
EIM_WAIT	M25	NVCC_EIM2	GPIO	ALT0	EIM_WAIT	Input	PU (100K)
ENET_CRS_DV	U21	NVCC_ENET	GPIO	ALT5	GPIO1_IO25	Input	PU (100K)
ENET_MDC	V20	NVCC_ENET	GPIO	ALT5	GPIO1_IO31	Input	PU (100K)
ENET_MDIO	V23	NVCC_ENET	GPIO	ALT5	GPIO1_IO22	Input	PU (100K)
ENET_REF_CLK[3]	V22	NVCC_ENET	GPIO	ALT5	GPIO1_IO23	Input	PU (100K)
ENET_RX_ER	W23	NVCC_ENET	GPIO	ALT5	GPIO1_IO24	Input	PU (100K)
ENET_RXD0	W21	NVCC_ENET	GPIO	ALT5	GPIO1_IO27	Input	PU (100K)
ENET_RXD1	W22	NVCC_ENET	GPIO	ALT5	GPIO1_IO26	Input	PU (100K)
ENET_TX_EN	V21	NVCC_ENET	GPIO	ALT5	GPIO1_IO28	Input	PU (100K)
ENET_TXD0	U20	NVCC_ENET	GPIO	ALT5	GPIO1_IO30	Input	PU (100K)
ENET_TXD1	W20	NVCC_ENET	GPIO	ALT5	GPIO1_IO29	Input	PU (100K)
GPIO_0	T5	NVCC_GPIO	GPIO	ALT5	GPIO1_IO00	Input	PD (100K)
GPIO_1	T4	NVCC_GPIO	GPIO	ALT5	GPIO1_IO01	Input	PU (100K)
GPIO_16	R2	NVCC_GPIO	GPIO	ALT5	GPIO7_IO11	Input	PU (100K)
GPIO_17	R1	NVCC_GPIO	GPIO	ALT5	GPIO7_IO12	Input	PU (100K)
GPIO_18	P6	NVCC_GPIO	GPIO	ALT5	GPIO7_IO13	Input	PU (100K)
GPIO_19	P5	NVCC_GPIO	GPIO	ALT5	GPIO4_IO05	Input	PU (100K)
GPIO_2	T1	NVCC_GPIO	GPIO	ALT5	GPIO1_IO02	Input	PU (100K)
GPIO_3	R7	NVCC_GPIO	GPIO	ALT5	GPIO1_IO03	Input	PU (100K)
GPIO_4	R6	NVCC_GPIO	GPIO	ALT5	GPIO1_IO04	Input	PU (100K)
GPIO_5	R4	NVCC_GPIO	GPIO	ALT5	GPIO1_IO05	Input	PU (100K)
GPIO_6	T3	NVCC_GPIO	GPIO	ALT5	GPIO1_IO06	Input	PU (100K)
GPIO_7	R3	NVCC_GPIO	GPIO	ALT5	GPIO1_IO07	Input	PU (100K)

Table 102. 21 x 21 mm, 0.8 mm Pitch Ball Map (continued)

	M	N	P	R	T	U	V	W
1	CSI0_DAT10	CSI0_DAT4	CSI0_PIXCLK	GPIO_17	GPIO_2	LVDS0_TX0_P	LVDS0_TX2_P	LVDS0_TX3_P
2	CSI0_DAT12	CSI0_VSYNC	CSI0_DAT5	GPIO_16	GPIO_9	LVDS0_TX0_N	LVDS0_TX2_N	LVDS0_TX3_N
3	CSI0_DAT11	CSI0_DAT7	CSI0_DATA_EN	GPIO_7	GPIO_6	LVDS0_TX1_P	LVDS0_CLK_P	GND
4	CSI0_DAT14	CSI0_DAT6	CSI0_MCLK	GPIO_5	GPIO_1	LVDS0_TX1_N	LVDS0_CLK_N	KEY_ROW2
5	CSI0_DAT15	CSI0_DAT9	GPIO_19	GPIO_8	GPIO_0	KEY_COL3	KEY_ROW4	KEY_COL0
6	CSI0_DAT18	CSI0_DAT8	GPIO_18	GPIO_4	KEY_COL4	KEY_ROW1	KEY_ROW0	KEY_COL2
7	HDMI_VPH	NVCC_CSI	NVCC_GPIO	GPIO_3	KEY_ROW3	KEY_COL1	NVCC_LVDS2P5	GND
8	GND	GND	GND	GND	GND	GND	GND	GND
9	VDDARM23_IN	VDDARM23_IN	VDDARM23_IN	VDDARM23_IN	VDDARM23_IN	VDDARM23_IN	NVCC_DRAM	GND
10	GND	GND	GND	VDDSOC_CAP	VDDSOC_CAP	VDDSOC_CAP	NVCC_DRAM	GND
11	VDDARM23_CAP	VDDARM23_CAP	VDDARM23_CAP	VDDARM23_CAP	GND	GND	NVCC_DRAM	GND
12	GND	VDD_CACHE_CAP	GND	GND	GND	GND	NVCC_DRAM	GND
13	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDSOC_CAP	VDDSOC_CAP	NVCC_DRAM	GND
14	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDSOC_CAP	VDDSOC_CAP	NVCC_DRAM	DRAM_A4
15	GND	GND	GND	GND	GND	GND	NVCC_DRAM	GND
16	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	NVCC_DRAM	GND
17	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP	GND	GND	GND	NVCC_DRAM	GND
18	GND	GND	GND	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	GND
19	NVCC_EIM2	DI0_DISP_CLK	NVCC_LCD	NVCC_ENET	GND	GND	GND	GND
20	EIM_DA11	DI0_PIN3	DISP0_DAT4	DISP0_DAT13	DISP0_DAT21	ENET_TXD0	ENET_MDC	ENET_TXD1
21	EIM_DA9	DI0_PIN15	DISP0_DAT3	DISP0_DAT10	DISP0_DAT16	ENET_CRS_DV	ENET_TX_EN	ENET_RXD0
22	EIM_DA10	EIM_BCLK	DISP0_DAT1	DISP0_DAT8	DISP0_DAT15	DISP0_DAT20	ENET_REF_CLK	ENET_RXD1
23	EIM_DA13	EIM_DA14	DISP0_DAT2	DISP0_DAT6	DISP0_DAT11	DISP0_DAT19	ENET_MDIO	ENET_RX_ER
24	EIM_DA12	EIM_DA15	DISP0_DAT0	DISP0_DAT7	DISP0_DAT12	DISP0_DAT17	DISP0_DAT22	DISP0_DAT23
25	EIM_WAIT	DI0_PIN2	DI0_PIN4	DISP0_DAT5	DISP0_DAT9	DISP0_DAT14	DISP0_DAT18	DRAM_D63