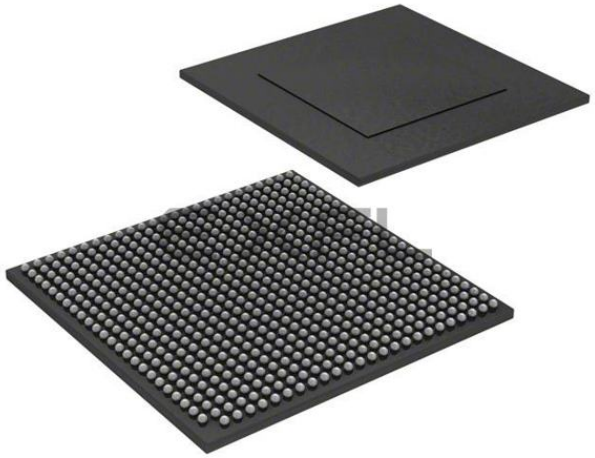

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	4 Core, 32-Bit
Speed	852MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (1)
SATA	SATA 3Gbps (1)
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-40°C ~ 125°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	624-FBGA, FCBGA
Supplier Device Package	624-FCBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6q4avt08adr

1.2 Features

The i.MX 6Dual/6Quad processors are based on ARM Cortex-A9 MPCore platform, which has the following features:

- ARM Cortex-A9 MPCore 4xCPU processor (with TrustZone®)
- The core configuration is symmetric, where each core includes:
  - 32 KByte L1 Instruction Cache
  - 32 KByte L1 Data Cache
  - Private Timer and Watchdog
  - Cortex-A9 NEON MPE (Media Processing Engine) Co-processor

The ARM Cortex-A9 MPCore complex includes:

- General Interrupt Controller (GIC) with 128 interrupt support
- Global Timer
- Snoop Control Unit (SCU)
- 1 MB unified I/D L2 cache, shared by two/four cores
- Two Master AXI (64-bit) bus interfaces output of L2 cache
- Frequency of the core (including Neon and L1 cache) as per Table 6.
- NEON MPE coprocessor
  - SIMD Media Processing Architecture
  - NEON register file with 32x64-bit general-purpose registers
  - NEON Integer execute pipeline (ALU, Shift, MAC)
  - NEON dual, single-precision floating point execute pipeline (FADD, FMUL)
  - NEON load/store and permute pipeline

The SoC-level memory system consists of the following additional components:

  - Boot ROM, including HAB (96 KB)
  - Internal multimedia / shared, fast access RAM (OCRAM, 256 KB)
  - Secure/non-secure RAM (16 KB)
- External memory interfaces:
  - 16-bit, 32-bit, and 64-bit DDR3-1066, LVDDR3-1066, and 1/2 LPDDR2-1066 channels, supporting DDR interleaving mode, for 2x32 LPDDR2-1066
  - 8-bit NAND-Flash, including support for Raw MLC/SLC, 2 KB, 4 KB, and 8 KB page size, BA-NAND, PBA-NAND, LBA-NAND, OneNAND™ and others. BCH ECC up to 40 bit.
  - 16/32-bit NOR Flash. All EIMv2 pins are muxed on other interfaces.
  - 16/32-bit PSRAM, Cellular RAM

Each i.MX 6Dual/6Quad processor enables the following interfaces to external devices (some of them are muxed and not available simultaneously):

- Hard Disk Drives—SATA II, 3.0 Gbps

Table 8. Maximum Supply Currents

Power Supply	Conditions	Maximum Current		Unit
		Power Virus	CoreMark	
i.MX 6Quad: VDD_ARM_IN + VDD_ARM23_IN	• ARM frequency = 996 MHz • ARM LDOs set to 1.3V • T_j = 125°C	3920	2500	mA
	• ARM frequency = 852 MHz • ARM LDOs set to 1.3V • T_j = 125°C	3630	2260	mA
i.MX 6Dual: VDD_ARM_IN	• ARM frequency = 996 MHz • ARM LDOs set to 1.3V • T_j = 125°C	2350	1500	mA
	• ARM frequency = 852 MHz • ARM LDOs set to 1.3V • T_j = 125°C	2110	1360	mA
i.MX 6Dual: or i.MX 6Quad: VDD_SOC_IN	• Running 3DMark • GPU frequency = 600 MHz • SOC LDO set to 1.3V • T_j = 125°C	2500		mA
VDD_HIGH_IN	—	125[1]		mA
VDD_SNVS_IN	—	275[2]		µA
USB_OTG_VBUS/ USB_H1_VBUS (LDO 3P0)	—	25[3]		mA
Primary Interface (IO) Supplies				
NVCC_DRAM	—	(see note[4])		
NVCC_ENET	N=10	Use maximum IO equation[5]		
NVCC_LCD	N=29	Use maximum IO equation[5]		
NVCC_GPIO	N=24	Use maximum IO equation[5]		
NVCC_CSI	N=20	Use maximum IO equation[5]		
NVCC_EIM0	N=19	Use maximum IO equation[5]		
NVCC_EIM1	N=14	Use maximum IO equation[5]		
NVCC_EIM2	N=20	Use maximum IO equation[5]		
NVCC_JTAG	N=6	Use maximum IO equation[5]		
NVCC_RGMII	N=6	Use maximum IO equation[5]		
NVCC_SD1	N=6	Use maximum IO equation[5]		
NVCC_SD2	N=6	Use maximum IO equation[5]		
NVCC_SD3	N=11	Use maximum IO equation[5]		
NVCC_NANDF	N=26	Use maximum IO equation[5]		
NVCC_MIPI	—	25.5		mA

4.1.9 PCIe 2.0 Maximum Power Consumption

Table 12 provides PCIe PHY currents for certain operating modes.

Table 12. PCIe PHY Current Drain

Mode	Test Conditions	Supply	Max Current	Unit
P0: Normal Operation	5G Operations	PCIE_VP (1.1 V)	40	mA
		PCIE_VPTX (1.1 V)	20	
		PCIE_VPH (2.5 V)	21	
	2.5G Operations	PCIE_VP (1.1 V)	27	
		PCIE_VPTX (1.1 V)	20	
		PCIE_VPH (2.5 V)	20	
P0s: Low Recovery Time Latency, Power Saving State	5G Operations	PCIE_VP (1.1 V)	30	mA
		PCIE_VPTX (1.1 V)	2.4	
		PCIE_VPH (2.5 V)	18	
	2.5G Operations	PCIE_VP (1.1 V)	20	
		PCIE_VPTX (1.1 V)	2.4	
		PCIE_VPH (2.5 V)	18	
P1: Longer Recovery Time Latency, Lower Power State	—	PCIE_VP (1.1 V)	12	mA
		PCIE_VPTX (1.1 V)	2.4	
		PCIE_VPH (2.5 V)	12	
Power Down	—	PCIE_VP (1.1 V)	1.3	mA
		PCIE_VPTX (1.1 V)	0.18	
		PCIE_VPH (2.5 V)	0.36	

4.2 Power Supplies Requirements and Restrictions

The system design must comply with power-up sequence, power-down sequence, and steady state guidelines as described in this section to ensure the reliable operation of the device. Any deviation from these sequences may result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting
- Irreversible damage to the processor

4.2.1 Power-Up Sequence

For power-up sequence, the restrictions are as follows:

- VDD_SNVS_IN supply must be turned ON before any other power supply. It may be connected (shorted) with VDD_HIGH_IN supply.
- If a coin cell is used to power VDD_SNVS_IN, then ensure that it is connected before any other supply is switched on.
- If the external SRC_POR_B signal is used to control the processor POR, then SRC_POR_B must be immediately asserted at power-up and remain asserted until the VDD_ARM_CAP, VDD_SOC_CAP, and VDD_PU_CAP supplies are stable. VDD_ARM_IN and VDD_SOC_IN may be applied in either order with no restrictions. In the absence of an external reset feeding the SRC_POR_B input, the internal POR module takes control. See the i.MX 6Dual/6Quad reference manual (IMX6DQRM) for further details and to ensure that all necessary requirements are being met.
- If the external SRC_POR_B signal is not used (always held high or left unconnected), the processor defaults to the internal POR function (where the PMU controls generation of the POR based on the power supplies). If the internal POR function is used, the following power supply requirements must be met:
  - VDD_ARM_IN and VDD_SOC_IN may be supplied from the same source, or
  - VDD_SOC_IN can be supplied before VDD_ARM_IN with a maximum delay of 1 ms.

NOTE

Ensure that there is no back voltage (leakage) from any supply on the board towards the 3.3 V supply (for example, from the external components that use both the 1.8 V and 3.3 V supplies).

NOTE

USB_OTG_VBUS and USB_H1_VBUS are not part of the power supply sequence and can be powered at any time.

4.2.2 Power-Down Sequence

No special restrictions for i.MX 6Dual/6Quad SoC.

Table 40. EIM Bus Timing Parameters (continued)

ID	Parameter	Min[1]	Max[1]	Unit
WE4	Clock rise to address valid	-0.5 × t × (k+1) - 1.25	-0.5 × t × (k+1) + 2.25	ns
WE5	Clock rise to address invalid	0.5 × t × (k+1) - 1.25	0.5 × t × (k+1) + 2.25	ns
WE6	Clock rise to EIM_CSx_B valid	-0.5 × t × (k+1) - 1.25	-0.5 × t × (k+1) + 2.25	ns
WE7	Clock rise to EIM_CSx_B invalid	0.5 × t × (k+1) - 1.25	0.5 × t × (k+1) + 2.25	ns
WE8	Clock rise to EIM_WE_B valid	-0.5 × t × (k+1) - 1.25	-0.5 × t × (k+1) + 2.25	ns
WE9	Clock rise to EIM_WE_B invalid	0.5 × t × (k+1) - 1.25	0.5 × t × (k+1) + 2.25	ns
WE10	Clock rise to EIM_OE_B valid	-0.5 × t × (k+1) - 1.25	-0.5 × t × (k+1) + 2.25	ns
WE11	Clock rise to EIM_OE_B invalid	0.5 × t × (k+1) - 1.25	0.5 × t × (k+1) + 2.25	ns
WE12	Clock rise to EIM_EBx_B valid	-0.5 × t × (k+1) - 1.25	-0.5 × t × (k+1) + 2.25	ns
WE13	Clock rise to EIM_EBx_B invalid	0.5 × t × (k+1) - 1.25	0.5 × t × (k+1) + 2.25	ns
WE14	Clock rise to EIM_LBA_B valid	-0.5 × t × (k+1) - 1.25	-0.5 × t × (k+1) + 2.25	ns
WE15	Clock rise to EIM_LBA_B invalid	0.5 × t × (k+1) - 1.25	0.5 × t × (k+1) + 2.25	ns
WE16	Clock rise to output data valid	-0.5 × t × (k+1) - 1.25	-0.5 × t × (k+1) + 2.25	ns
WE17	Clock rise to output data invalid	0.5 × t × (k+1) - 1.25	0.5 × t × (k+1) + 2.25	ns
WE18	Input data setup time to clock rise	2.3	—	ns
WE19	Input data hold time from clock rise	2	—	ns
WE20	EIM_WAIT_B setup time to clock rise	2	—	ns
WE21	EIM_WAIT_B hold time from clock rise	2	—	ns

1 k represents register setting BCD value.

2 t is clock period (1/Freq). For 104 MHz, t = 9.165 ns.

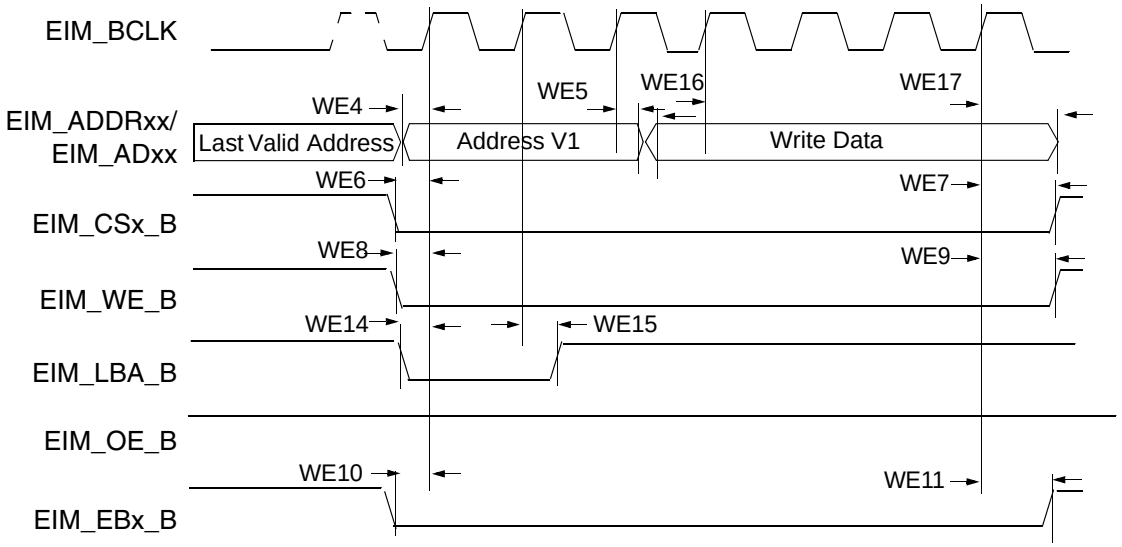

Figure 16. Muxed Address/Data (A/D) Mode, Synchronous Write Access, WSC=6,ADVA=0, ADVN=1, and ADH=1

NOTE

In 32-bit muxed address/data (A/D) mode the 16 MSBs are driven on the data bus.

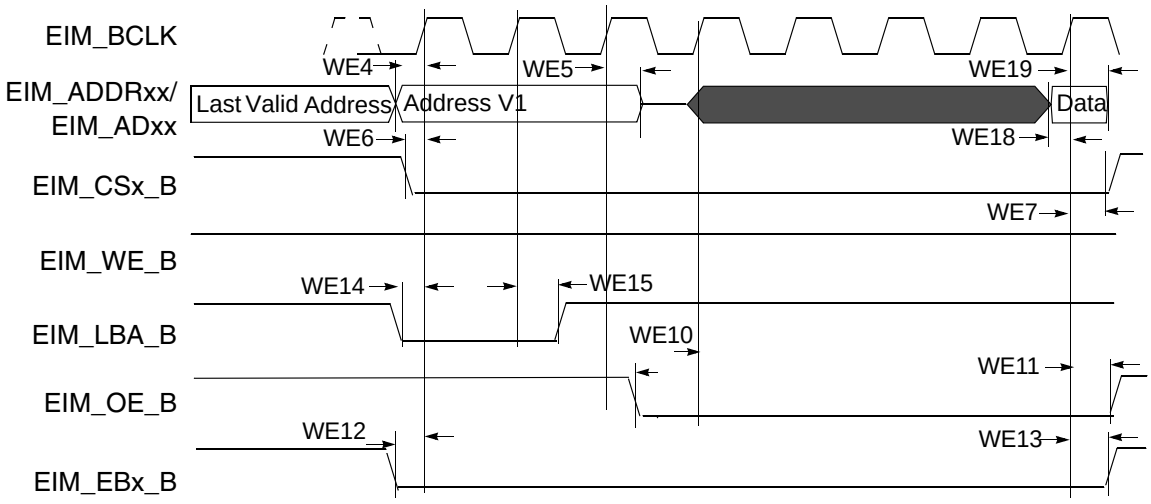

Figure 17. 16-Bit Muxed A/D Mode, Synchronous Read Access, WSC=7, RADVN=1, ADH=1, OEA=0

4.9.3.4 General EIM Timing-Asynchronous Mode

Figure 18 through Figure 22 and Table 41 provide timing parameters relative to the chip select (CS) state for asynchronous and DTACK EIM accesses with corresponding EIM bit fields and the timing parameters mentioned above.

Asynchronous read & write access length in cycles may vary from what is shown in Figure 18 through Figure 21 as RWSC, OEN & CSN is configured differently. See the i.MX 6Dual/6Quad reference manual (IMX6DQRM) for the EIM programming model.

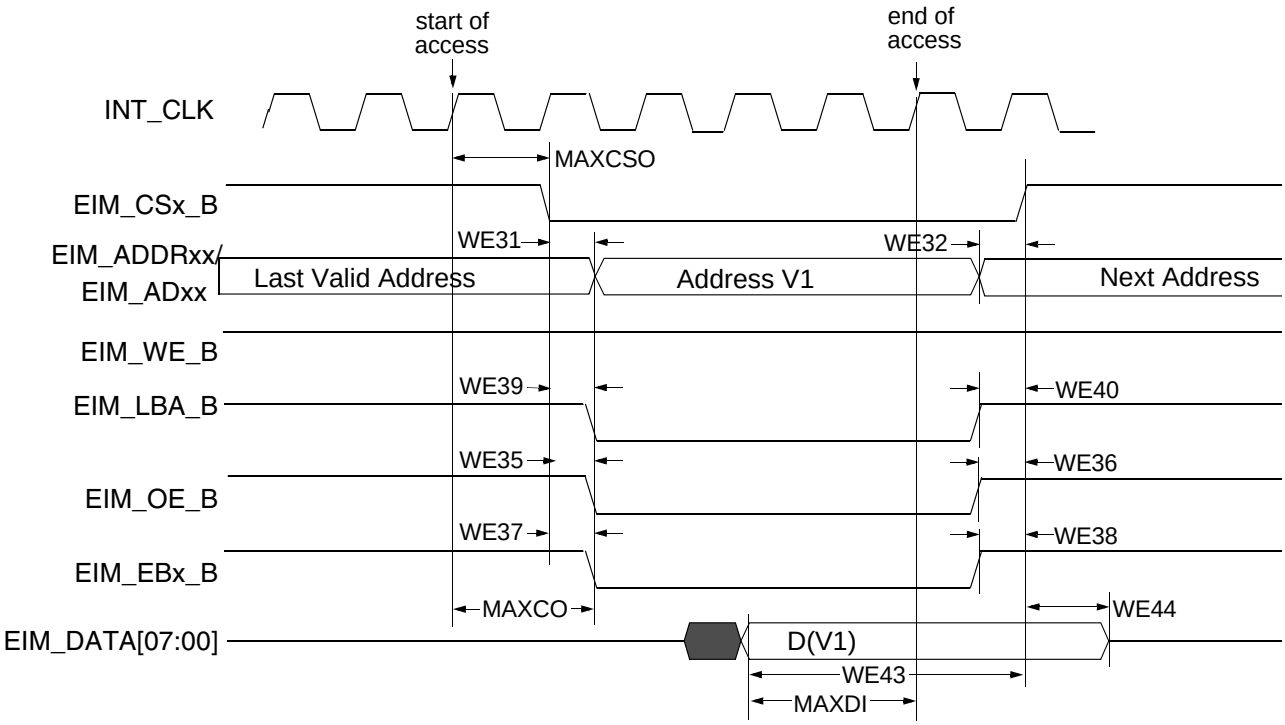

Figure 18. Asynchronous Memory Read Access (RWSC = 5)

4.10.1 Asynchronous Mode AC Timing (ONFI 1.0 Compatible)

Asynchronous mode AC timings are provided as multiplications of the clock cycle and fixed delay. The Maximum I/O speed of GPMI in Asynchronous mode is about 50 MB/s. Figure 30 through Figure 33 depict the relative timing between GPMI signals at the module level for different operations under Asynchronous mode. Table 48 describes the timing parameters (NF1–NF17) that are shown in the figures.

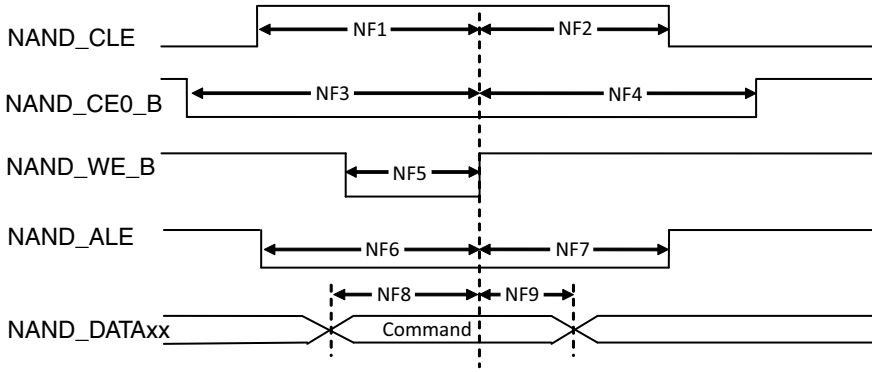

Figure 30. Command Latch Cycle Timing Diagram

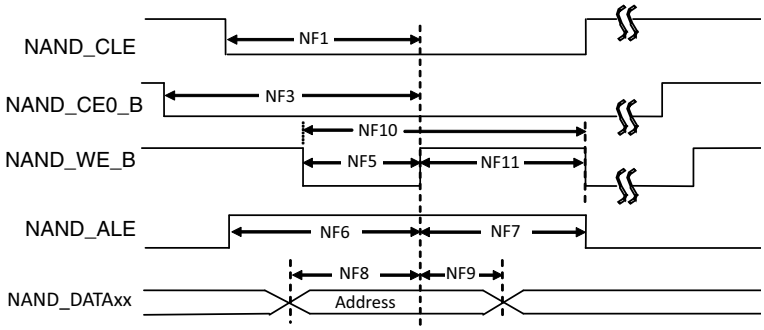

Figure 31. Address Latch Cycle Timing Diagram

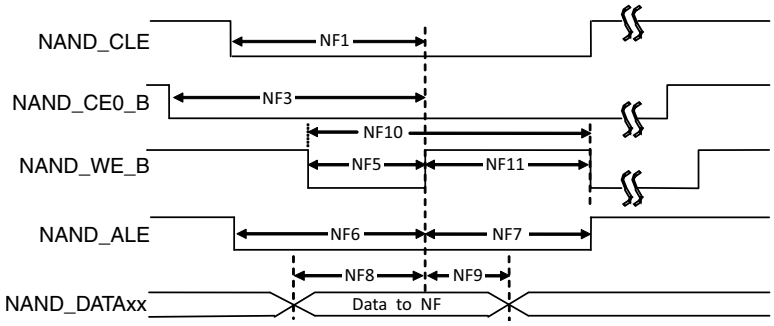

Figure 32. Write Data Latch Cycle Timing Diagram

4.11.4.3 SDR50/SDR104 AC Timing

Figure 47 depicts the timing of SDR50/SDR104, and Table 56 lists the SDR50/SDR104 timing characteristics.

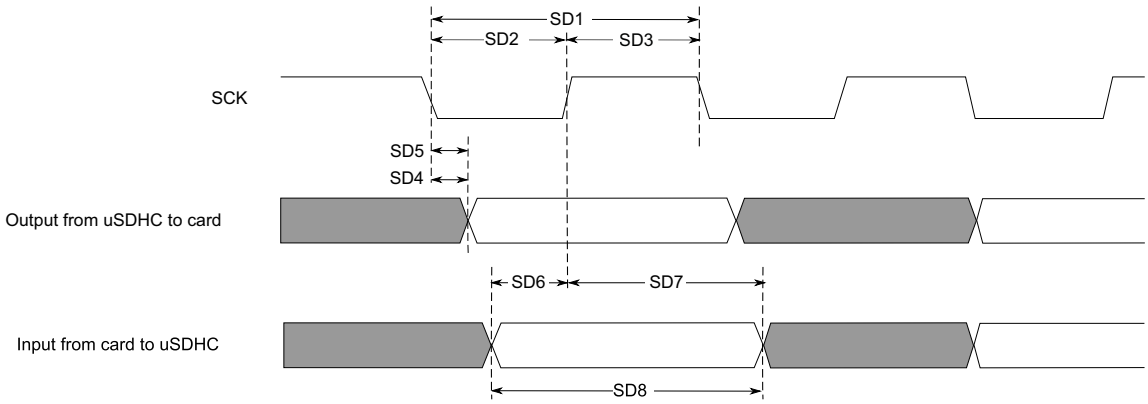

Figure 47. SDR50/SDR104 Timing

Table 56. SDR50/SDR104 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency Period	t_{CLK}	4.8	—	ns
SD2	Clock Low Time	t_{CL}	$0.3 \times t_{CLK}$	$0.7 \times t_{CLK}$	ns
SD2	Clock High Time	t_{CH}	$0.3 \times t_{CLK}$	$0.7 \times t_{CLK}$	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR50 (Reference to SDx_CLK)					
SD4	uSDHC Output Delay	t_{OD}	–3	1	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR104 (Reference to SDx_CLK)					
SD5	uSDHC Output Delay	t_{OD}	–1.6	1	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR50 (Reference to SDx_CLK)					
SD6	uSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD7	uSDHC Input Hold Time	t_{IH}	1.5	—	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR104 (Reference to SDx_CLK)[1]					
SD8	Card Output Data Window	t_{ODW}	$0.5 \times t_{CLK}$	—	ns

[1]Data window in SDR100 mode is variable.

4.11.4.4 Bus Operation Condition for 3.3 V and 1.8 V Signaling

Signalling level of SD/eMMC4.3 and eMMC4.4/4.41 modes is 3.3 V. Signalling level of SDR104/SDR50 mode is 1.8 V. The DC parameters for the NVCC_SD1, NVCC_SD2, and NVCC_SD3 supplies are identical to those shown in Table 22, "GPIO I/O DC Parameters," on page 39.

4.11.5 Ethernet Controller (ENET) AC Electrical Specifications

4.11.5.1 ENET MII Mode Timing

This subsection describes MII receive, transmit, asynchronous inputs, and serial management signal timings.

4.11.5.1.1 MII Receive Signal Timing (ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER, and ENET_RX_CLK)

The receiver functions correctly up to an ENET_RX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. Additionally, the processor clock frequency must exceed twice the ENET_RX_CLK frequency.

Figure 48 shows MII receive signal timings. Table 57 describes the timing parameters (M1–M4) shown in the figure.

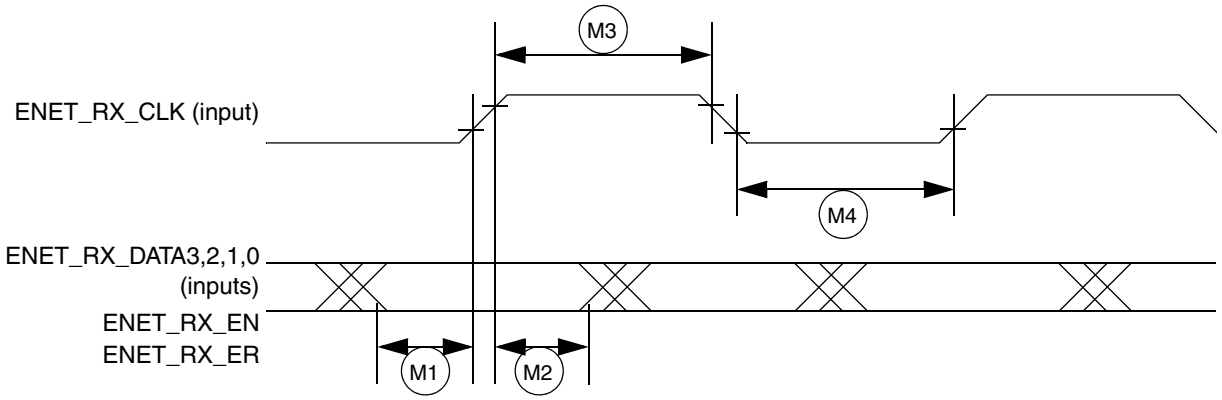

Figure 48. MII Receive Signal Timing Diagram

Table 57. MII Receive Signal Timing

ID	Characteristic[1]	Min	Max	Unit
M1	ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER to ENET_RX_CLK setup	5	—	ns
M2	ENET_RX_CLK to ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER hold	5	—	ns
M3	ENET_RX_CLK pulse width high	35%	65%	ENET_RX_CLK period
M4	ENET_RX_CLK pulse width low	35%	65%	ENET_RX_CLK period

[1] ENET_RX_EN, ENET_RX_CLK, and ENET0_RXD0 have the same timing in 10 Mbps 7-wire interface mode.

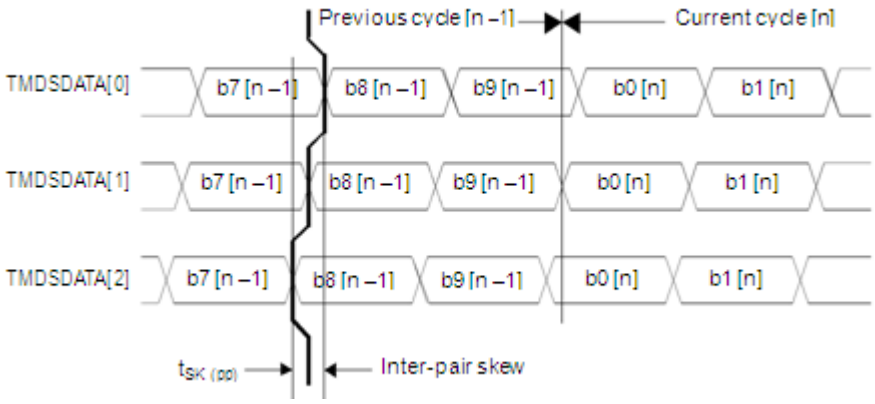

Figure 62. Inter-Pair Skew Definition

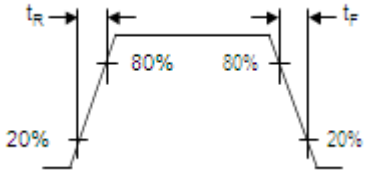

Figure 63. TMDS Output Signals Rise and Fall Time Definition

Table 64. Switching Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TMDS Drivers Specifications						
—	Maximum serial data rate	—	—	—	3.4	Gbps
$F_{TMDSCLK}$	TMDSCLK frequency	On TMDSCLKP/N outputs	25	—	340	MHz
$P_{TMDSCLK}$	TMDSCLK period	RL = 50 Ω See Figure 59.	2.94	—	40	ns
t_{CDC}	TMDSCLK duty cycle	$t_{CDC} = t_{CPH} / P_{TMDSCLK}$ RL = 50 Ω See Figure 59.	40	50	60	%
t_{CPH}	TMDSCLK high time	RL = 50 Ω See Figure 59.	4	5	6	UI
t_{CPL}	TMDSCLK low time	RL = 50 Ω See Figure 59.	4	5	6	UI
—	TMDSCLK jitter[1]	RL = 50 Ω	—	—	0.25	UI
$t_{SK(p)}$	Intra-pair (pulse) skew	RL = 50 Ω See Figure 61.	—	—	0.15	UI
$t_{SK(pp)}$	Inter-pair skew	RL = 50 Ω See Figure 62.	—	—	1	UI
t_R	Differential output signal rise time	20–80% RL = 50 Ω See Figure 63.	75	—	0.4 UI	ps

Table 64. Switching Characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_F	Differential output signal fall time	20–80% RL = 50 Ω See Figure 63.	75	—	0.4 UI	ps
—	Differential signal overshoot	Referred to 2x V_{SWING}	—	—	15	%
—	Differential signal undershoot	Referred to 2x V_{SWING}	—	—	25	%
Data and Control Interface Specifications						
$t_{Power\text{-}up}$[2]	HDMI 3D Tx PHY power-up time	From power-down to HSI_TX_READY assertion	—	—	3.35	ms

1 Relative to ideal recovery clock, as specified in the HDMI specification, version 1.4a, section 4.2.3.

2 For information about latencies and associated timings, see Section 4.11.7.1, "Latencies and Timing Information."

4.11.9 I²C Module Timing Parameters

This section describes the timing parameters of the I²C module. Figure 64 depicts the timing of I²C module, and Table 65 lists the I²C module timing characteristics.

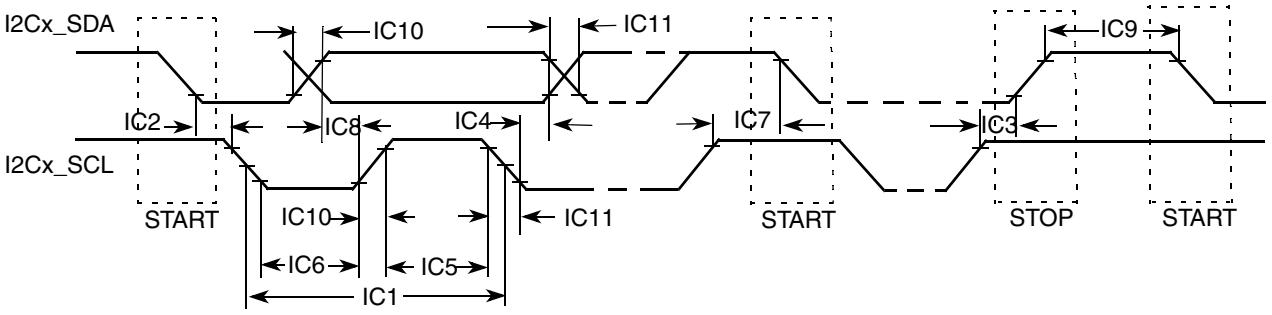

Figure 64. I²C Bus Timing

Table 65. I²C Module Timing Parameters

ID	Parameter	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
IC1	I2Cx_SCL cycle time	10	—	2.5	—	µs
IC2	Hold time (repeated) START condition	4.0	—	0.6	—	µs
IC3	Set-up time for STOP condition	4.0	—	0.6	—	µs
IC4	Data hold time	0[1]	3.45[2]	0[1]	0.9[2]	µs
IC5	HIGH Period of I2Cx_SCL Clock	4.0	—	0.6	—	µs
IC6	LOW Period of the I2Cx_SCL Clock	4.7	—	1.3	—	µs
IC7	Set-up time for a repeated START condition	4.7	—	0.6	—	µs
IC8	Data set-up time	250	—	100[3]	—	ns

- IPP_DISP_CLK latches data into the panel on its negative edge (when positive polarity is selected). In active mode, IPP_DISP_CLK runs continuously.
- HSYNC causes the panel to start a new line. (Usually IPUx_DIx_PIN02 is used as HSYNC.)
- VSYNC causes the panel to start a new frame. It always encompasses at least one HSYNC pulse. (Usually IPUx_DIx_PIN03 is used as VSYNC.)
- DRDY acts like an output enable signal to the CRT display. This output enables the data to be shifted onto the display. When disabled, the data is invalid and the trace is off.
(DRDY can be used either synchronous or asynchronous generic purpose pin as well.)

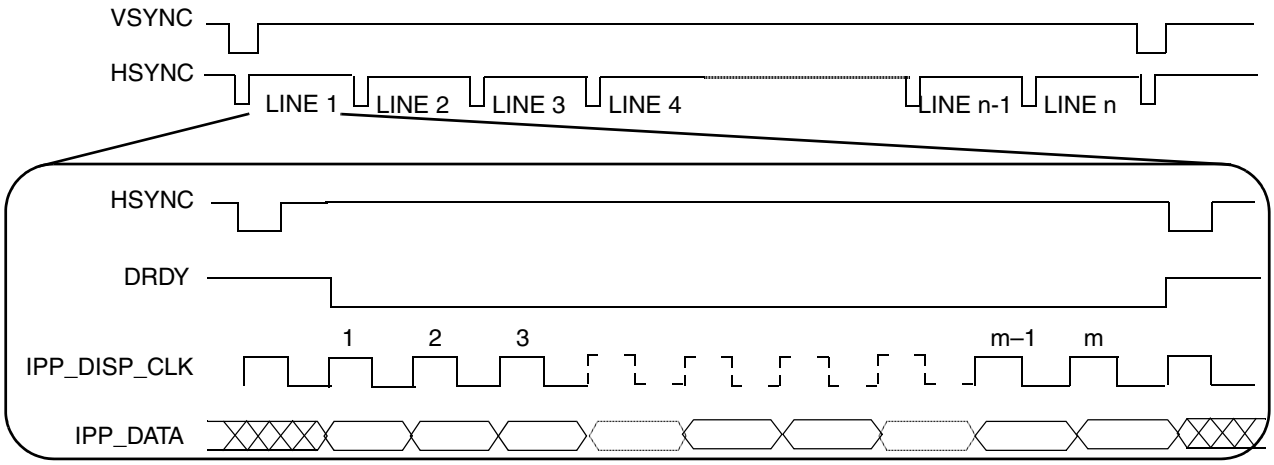

Figure 68. Interface Timing Diagram for TFT (Active Matrix) Panels

4.11.10.6.3 TFT Panel Sync Pulse Timing Diagrams

Figure 69 depicts the horizontal timing (timing of one line), including both the horizontal sync pulse and the data. All the parameters shown in the figure are programmable. All controls are started by corresponding internal events—local start points. The timing diagrams correspond to inverse polarity of the IPP_DISP_CLK signal and active-low polarity of the HSYNC, VSYNC, and DRDY signals.

Table 72. Electrical and Timing Information (continued)

Symbol	Parameters	Test Conditions	Min	Typ	Max	Unit
V_{IDTL}	Differential input low voltage threshold	—	-70	—	—	mV
V_{IHHS}	Single ended input high voltage	—	—	—	460	mV
V_{ILHS}	Single ended input low voltage	—	-40	—	—	mV
V_{CMRXDC}	Input common mode voltage	—	70	—	330	mV
Z_{ID}	Differential input impedance	—	80	—	125	Ω
LP Line Receiver DC Specifications						
V_{IL}	Input low voltage	—	—	—	550	mV
V_{IH}	Input high voltage	—	920	—	—	mV
V_{HYST}	Input hysteresis	—	25	—	—	mV
Contention Line Receiver DC Specifications						
V_{ILF}	Input low fault threshold	—	200	—	450	mV

4.11.12.6 High-Speed Clock Timing

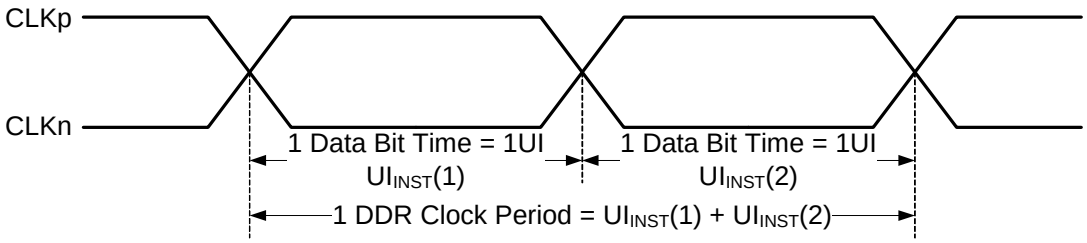

Figure 75. DDR Clock Definition

4.11.12.7 Forward High-Speed Data Transmission Timing

The timing relationship of the DDR Clock differential signal to the Data differential signal is shown in Figure 76:

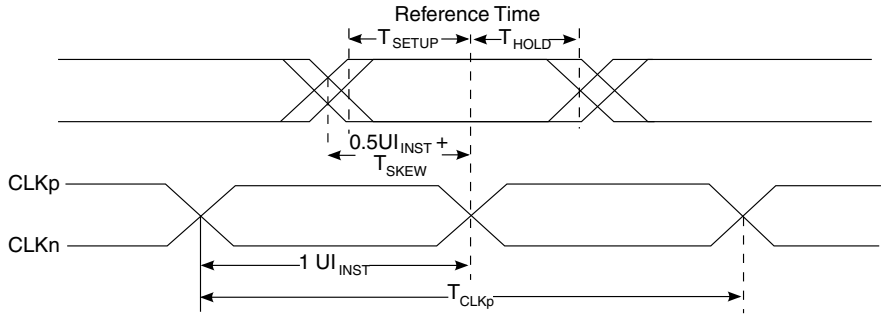

Figure 76. Data to Clock Timing Definitions

4.11.12.8 Reverse High-Speed Data Transmission Timing

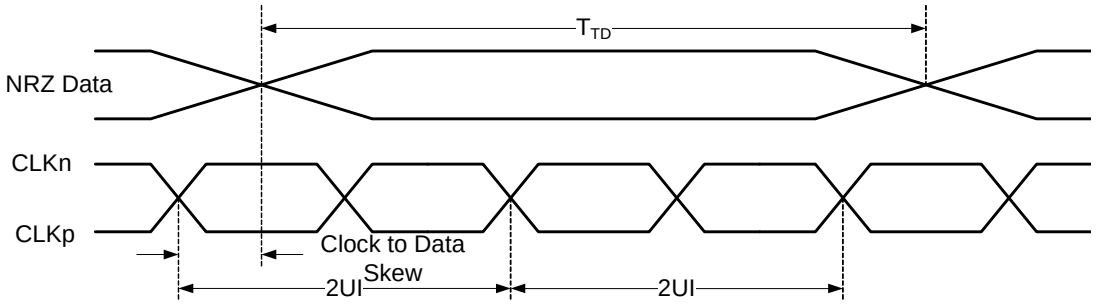

Figure 77. Reverse High-Speed Data Transmission Timing at Slave Side

4.11.13.6 Frame Transmission Mode (Synchronized Data Flow)

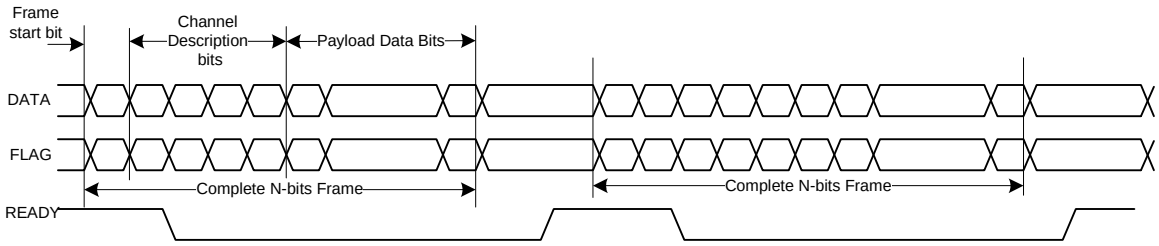

Figure 84. Frame Transmission Mode Transfer of Two Frames (Synchronized Data Flow)

4.11.13.7 Frame Transmission Mode (Pipelined Data Flow)

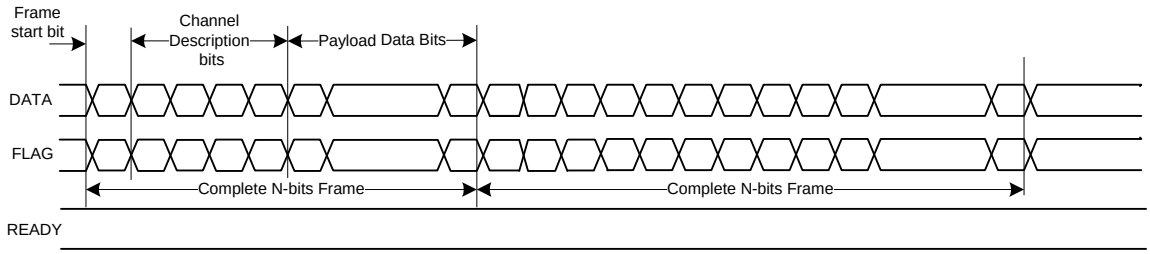

Figure 85. Frame Transmission Mode Transfer of Two Frames (Pipelined Data Flow)

4.11.13.8 DATA and FLAG Signal Timing Requirement for a 15 pF Load

Table 74. DATA and FLAG Timing

Parameter	Description	1 Mbit/s	100 Mbit/s
$t_{Bit, nom}$	Nominal bit time	1000 ns	10 ns
$t_{Rise, min}$ and $t_{Fall, min}$	Minimum allowed rise and fall time	2 ns	2 ns
$t_{TxToRxSkew, maxfq}$	Maximum skew between transmitter and receiver package pins	50 ns	0.5 ns
$t_{EageSepTx, min}$	Minimum allowed separation of signal transitions at transmitter package pins, including all timing defects, for example, jitter and skew, inside the transmitter.	400 ns	4 ns
$t_{EageSepRx, min}$	Minimum separation of signal transitions, measured at the receiver package pins, including all timing defects, for example, jitter and skew, inside the receiver.	350 ns	3.5 ns

Table 98. Interfaces Allocation During Boot (continued)

Interface	IP Instance	Allocated Pads During Boot	Comment
NAND Flash	GPMI	NANDF_CLE, NANDF_ALE, NANDF_WP_B, SD4_CMD, SD4_CLK, NANDF_RB0, SD4_DAT0, NANDF_CS0, NANDF_CS1, NANDF_CS2, NANDF_CS3, NANDF_D[7:0]	8 bit Only CS0 is supported
SD/MMC	USDHC-1	SD1_CLK, SD1_CMD,SD1_DAT0, SD1_DAT1, SD1_DAT2, SD1_DAT3, NANDF_D0, NANDF_D1, NANDF_D2, NANDF_D3, KEY_COL1	1, 4, or 8 bit
SD/MMC	USDHC-2	SD2_CLK, SD2_CMD, SD2_DAT0, SD2_DAT1, SD2_DAT2, SD2_DAT3, NANDF_D4, NANDF_D5, NANDF_D6, NANDF_D7, KEY_ROW1	1, 4, or 8 bit
SD/MMC	USDHC-3	SD3_CLK, SD3_CMD, SD3_DAT0, SD3_DAT1, SD3_DAT2, SD3_DAT3, SD3_DAT4, SD3_DAT5, SD3_DAT6, SD3_DAT7, GPIO_18	1, 4, or 8 bit
SD/MMC	USDHC-4	SD4_CLK, SD4_CMD, SD4_DAT0, SD4_DAT1, SD4_DAT2, SD4_DAT3, SD4_DAT4, SD4_DAT5, SD4_DAT6, SD4_DAT7, NANDF_CS1	1, 4, or 8 bit
I2C	I2C-1	EIM_D28, EIM_D21	—
I2C	I2C-2	EIM_D16, EIM_EB2	—
I2C	I2C-3	EIM_D18, EIM_D17	—
SATA	SATA_PHY	SATA_TXM, SATA_TXP, SATA_RXP, SATA_RXM, SATA_REXT	—
USB	USB-OTG PHY	USB_OTG_DP USB_OTG_DN USB_OTG_VBUS	—

Table 100. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function (Signal Name)	Input/Output	Value[2]
SD3_CLK	D14	NVCC_SD3	GPIO	ALT5	GPIO7_IO03	Input	PU (100K)
SD3_CMD	B13	NVCC_SD3	GPIO	ALT5	GPIO7_IO02	Input	PU (100K)
SD3_DAT0	E14	NVCC_SD3	GPIO	ALT5	GPIO7_IO04	Input	PU (100K)
SD3_DAT1	F14	NVCC_SD3	GPIO	ALT5	GPIO7_IO05	Input	PU (100K)
SD3_DAT2	A15	NVCC_SD3	GPIO	ALT5	GPIO7_IO06	Input	PU (100K)
SD3_DAT3	B15	NVCC_SD3	GPIO	ALT5	GPIO7_IO07	Input	PU (100K)
SD3_DAT4	D13	NVCC_SD3	GPIO	ALT5	GPIO7_IO01	Input	PU (100K)
SD3_DAT5	C13	NVCC_SD3	GPIO	ALT5	GPIO7_IO00	Input	PU (100K)
SD3_DAT6	E13	NVCC_SD3	GPIO	ALT5	GPIO6_IO18	Input	PU (100K)
SD3_DAT7	F13	NVCC_SD3	GPIO	ALT5	GPIO6_IO17	Input	PU (100K)
SD3_RST	D15	NVCC_SD3	GPIO	ALT5	GPIO7_IO08	Input	PU (100K)
SD4_CLK	E16	NVCC_NANDF	GPIO	ALT5	GPIO7_IO10	Input	PU (100K)
SD4_CMD	B17	NVCC_NANDF	GPIO	ALT5	GPIO7_IO09	Input	PU (100K)
SD4_DAT0	D18	NVCC_NANDF	GPIO	ALT5	GPIO2_IO08	Input	PU (100K)
SD4_DAT1	B19	NVCC_NANDF	GPIO	ALT5	GPIO2_IO09	Input	PU (100K)
SD4_DAT2	F17	NVCC_NANDF	GPIO	ALT5	GPIO2_IO10	Input	PU (100K)
SD4_DAT3	A20	NVCC_NANDF	GPIO	ALT5	GPIO2_IO11	Input	PU (100K)
SD4_DAT4	E18	NVCC_NANDF	GPIO	ALT5	GPIO2_IO12	Input	PU (100K)
SD4_DAT5	C19	NVCC_NANDF	GPIO	ALT5	GPIO2_IO13	Input	PU (100K)
SD4_DAT6	B20	NVCC_NANDF	GPIO	ALT5	GPIO2_IO14	Input	PU (100K)
SD4_DAT7	D19	NVCC_NANDF	GPIO	ALT5	GPIO2_IO15	Input	PU (100K)
TAMPER	E11	VDD_SNVS_IN	GPIO	ALT0	SNVS_TAMPER	Input	PD (100K)
TEST_MODE	E12	VDD_SNVS_IN	—	—	TCU_TEST_MODE	Input	PD (100K)
USB_H1_DN	F10	VDD_USB_CAP	—	—	USB_H1_DN	—	—
USB_H1_DP	E10	VDD_USB_CAP	—	—	USB_H1_DP	—	—
USB_OTG_CHD_B	B8	VDD_USB_CAP	—	—	USB_OTG_CHD_B	—	—
USB_OTG_DN	B6	VDD_USB_CAP	—	—	USB_OTG_DN	—	—
USB_OTG_DP	A6	VDD_USB_CAP	—	—	USB_OTG_DP	—	—
XTALI	A7	NVCC_PLL	—	—	XTALI	—	—
XTALO	B7	NVCC_PLL	—	—	XTALO	—	—

1 The state immediately after reset and before ROM firmware or software has executed.

2 Variance of the pull-up and pull-down strengths are shown in the tables as follows:

- Table 22, "GPIO I/O DC Parameters," on page 39.
- Table 23, "LPDDR2 I/O DC Electrical Parameters," on page 40
- Table 24, "DDR3/DDR3L I/O DC Electrical Parameters," on page 40

Table 101. Signals with Differing Before Reset and After Reset States (continued)

Ball Name	Before Reset State	
	Input/Output	Value
EIM_EB0	Input	PD (100K)
EIM_EB1	Input	PD (100K)
EIM_EB2	Input	PD (100K)
EIM_EB3	Input	PD (100K)
EIM_LBA	Input	PD (100K)
EIM_RW	Input	PD (100K)
EIM_WAIT	Input	PD (100K)
GPIO_17	Output	Drive state unknown (x)
GPIO_19	Output	Drive state unknown (x)
KEY_COL0	Output	Drive state unknown (x)

6.2.3 21 x 21 mm, 0.8 mm Pitch Ball Map

Table 102 shows the FCPBGA 21 x 21 mm, 0.8 mm pitch ball map.

Table 102. 21 x 21 mm, 0.8 mm Pitch Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
A		PCIE_REXT	PCIE_TXM	GND	FA_ANA	USB_OTG_DP	XTALI	GND	MLB_SN	MLB_DP	MLB_CN	SATA_TXP	GND	SATA_RXM	SD3_DAT2	NANDF_ALE	NANDF_CS2	NANDF_D0	NANDF_D4	SD4_DAT3	SD1_DAT0	SD2_DAT0	SD2_DAT2	RGMII_TD3	GND
B	PCIE_RXM	PCIE_RXP	PCIE_TXP	GND	VDD_FA	USB_OTG_DN	XTALO	USB_OTG_CHD_B	MLB_SP	MLB_DN	MLB_CP	SATA_TXM	SD3_CMD	SATA_RXP	SD3_DAT3	NANDF_RB0	SD4_CMD	NANDF_D5	SD4_DAT1	SD4_DAT6	SD1_CMD	SD2_DAT3	RGMII_RD1	RGMII_RD2	RGMII_RXC
C	GND	JTAG_TRSTB	JTAG_TMS	GND	CLK2_N	GND	CLK1_N	GPANAIO	RTC_XTALO	GND	POR_B	BOOT_MODE0	SD3_DAT5	SATA_REXT	NANDF_CLE	NANDF_CS1	NANDF_D1	NANDF_D7	SD4_DAT5	SD1_DAT1	SD2_CLK	RGMII_TD0	RGMII_TX_CTL	RGMII_RD0	EIM_D16
D	CSI_D1M	CSI_D1P	GND	CSI_REXT	CLK2_P	GND	CLK1_P	GND	RTC_XTALI	USB_H1_VBUS	PMIC_ON_REQ	ONOFF	SD3_DAT4	SD3_CLK	SD3_RST	NANDF_CS3	NANDF_D3	SD4_DAT0	SD4_DAT7	SD1_CLK	RGMII_TXC	RGMII_RX_CTL	RGMII_RD3	EIM_D18	EIM_D23

Table 102. 21 x 21 mm, 0.8 mm Pitch Ball Map (continued)

	W	V	U	T	R	P	N	M
1	LVDS0_TX3_P	LVDS0_TX2_P	LVDS0_TX0_P	GPIO_2	GPIO_17	CSI0_PIXCLK	CSI0_DAT4	CSI0_DAT10
2	LVDS0_TX3_N	LVDS0_TX2_N	LVDS0_TX0_N	GPIO_9	GPIO_16	CSI0_DAT5	CSI0_VSYNC	CSI0_DAT12
3	GND	LVDS0_CLK_P	LVDS0_TX1_P	GPIO_6	GPIO_7	CSI0_DATA_EN	CSI0_DAT7	CSI0_DAT11
4	KEY_ROW2	LVDS0_CLK_N	LVDS0_TX1_N	GPIO_1	GPIO_5	CSI0_MCLK	CSI0_DAT6	CSI0_DAT14
5	KEY_COL0	KEY_ROW4	KEY_COL3	GPIO_0	GPIO_8	GPIO_19	CSI0_DAT9	CSI0_DAT15
6	KEY_COL2	KEY_ROW0	KEY_ROW1	KEY_COL4	GPIO_4	GPIO_18	CSI0_DAT8	CSI0_DAT18
7	GND	NVCC_LVDS2P5	KEY_COL1	KEY_ROW3	GPIO_3	NVCC_GPIO	NVCC_CSI	HDMI_VPH
8	GND	GND	GND	GND	GND	GND	GND	GND
9	GND	NVCC_DRAM	VDDARM23_IN	VDDARM23_IN	VDDARM23_IN	VDDARM23_IN	VDDARM23_IN	VDDARM23_IN
10	GND	NVCC_DRAM	VDDSOC_CAP	VDDSOC_CAP	VDDSOC_CAP	GND	GND	GND
11	GND	NVCC_DRAM	GND	GND	VDDARM23_CAP	VDDARM23_CAP	VDDARM23_CAP	VDDARM23_CAP
12	GND	NVCC_DRAM	GND	GND	GND	GND	VDD_CACHE_CAP	GND
13	GND	NVCC_DRAM	VDDSOC_CAP	VDDSOC_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP
14	DRAM_A4	NVCC_DRAM	VDDSOC_CAP	VDDSOC_CAP	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN
15	GND	NVCC_DRAM	GND	GND	GND	GND	GND	GND
16	GND	NVCC_DRAM	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN
17	GND	NVCC_DRAM	GND	GND	GND	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP
18	GND	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	GND	GND	GND
19	GND	GND	GND	GND	NVCC_ENET	NVCC_LCD	DI0_DISP_CLK	NVCC_EIM2
20	ENET_TXD1	ENET_MDC	ENET_TXD0	DISP0_DAT21	DISP0_DAT13	DISP0_DAT4	DI0_PIN3	EIM_DA11
21	ENET_RXD0	ENET_TX_EN	ENET_CRS_DV	DISP0_DAT16	DISP0_DAT10	DISP0_DAT3	DI0_PIN15	EIM_DA9
22	ENET_RXD1	ENET_REF_CLK	DISP0_DAT20	DISP0_DAT15	DISP0_DAT8	DISP0_DAT1	EIM_BCLK	EIM_DA10
23	ENET_RX_ER	ENET_MDIO	DISP0_DAT19	DISP0_DAT11	DISP0_DAT6	DISP0_DAT2	EIM_DA14	EIM_DA13
24	DISP0_DAT23	DISP0_DAT22	DISP0_DAT17	DISP0_DAT12	DISP0_DAT7	DISP0_DAT0	EIM_DA15	EIM_DA12
25	DRAM_D63	DISP0_DAT18	DISP0_DAT14	DISP0_DAT9	DISP0_DAT5	DI0_PIN4	DI0_PIN2	EIM_WAIT