Freescale Semiconductor - MCIMX6Q4AVT10AC Datasheet

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	4 Core, 32-Bit
Speed	1GHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (1)
SATA	SATA 3Gbps (1)
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-40°C ~ 125°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	624-FBGA, FCBGA
Supplier Device Package	624-FCBGA (21x21)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcimx6q4avt10ac

1.1 Ordering Information

Table 1shows examples of orderable part numbers covered by this data sheet. This table does not include all possible orderable part numbers. The latest part numbers are available on freescale.com/imx6series. If your desired part number is not listed in the table, or you have questions about available parts, see freescale.com/imx6series or contact your Freescale representative.

Table 1. Example Orderable Part Numbers

Part Number	Quad/Dual CPU	Options	Speed[1] Grade	Temperature Grade	Package
MCIMX6Q6AVT10AC	i.MX 6Quad	With VPU, GPU	1 GHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6Q6AVT10AD	i.MX 6Quad	With VPU, GPU	1 GHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6Q4AVT10AC	i.MX 6Quad	With GPU, no VPU	1 GHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6Q4AVT10AD	i.MX 6Quad	With GPU, no VPU	1 GHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6Q6AVT08AC	i.MX 6Quad	With VPU, GPU	852 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6Q6AVT08AD	i.MX 6Quad	With VPU, GPU	852 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6Q4AVT08AC	i.MX 6Quad	With GPU, no VPU	852 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6Q4AVT08AD	i.MX 6Quad	With GPU, no VPU	852 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6D6AVT10AC	i.MX 6Dual	With VPU, GPU	1 GHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6D6AVT10AD	i.MX 6Dual	With VPU, GPU	1 GHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6D4AVT10AC	i.MX 6Dual	With GPU, no VPU	1 GHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6D4AVT10AD	i.MX 6Dual	With GPU, no VPU	1 GHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6D6AVT08AC	i.MX 6Dual	With VPU, GPU	852 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6D6AVT08AD	i.MX 6Dual	With VPU, GPU	852 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6D4AVT08AC	i.MX 6Dual	With GPU, no VPU	852 MHz	Automotive1	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6D4AVT08AD	i.MX 6Dual	With GPU, no VPU	852 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)

[1] If a 24 MHz input clock is used (required for USB), the maximum SoC speed is limited to 996 MHz.

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
ROM 96KB	Boot ROM	Internal Memory	Supports secure and regular Boot Modes. Includes read protection on 4K region for content protection
ROMCP	ROM Controller with Patch	Data Path	ROM Controller with ROM Patch support
SATA	Serial ATA	Connectivity Peripherals	The SATA controller and PHY is a complete mixed-signal IP solution designed to implement SATA II, 3.0 Gbps HDD connectivity.
SDMA	Smart Direct Memory Access	System Control Peripherals	The SDMA is multi-channel flexible DMA engine. It helps in maximizing system performance by off-loading the various cores in dynamic data routing. It has the following features: • Powered by a 16-bit Instruction-Set micro-RISC engine • Multi-channel DMA supporting up to 32 time-division multiplexed DMA channels • 48 events with total flexibility to trigger any combination of channels • Memory accesses including linear, FIFO, and 2D addressing • Shared peripherals between ARM and SDMA • Very fast context-switching with 2-level priority based preemptive multi-tasking • DMA units with auto-flush and prefetch capability • Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address) • DMA ports can handle unit-directional and bi-directional flows (copy mode) • Up to 8-word buffer for configurable burst transfers • Support of byte-swapping and CRC calculations • Library of Scripts and API is available
SJC	System JTAG Controller	System Control Peripherals	The SJC provides JTAG interface, which complies with JTAG TAP standards, to internal logic. The i.MX 6Dual/6Quad processors use JTAG port for production, testing, and system debugging. In addition, the SJC provides BSR (Boundary Scan Register) standard support, which complies with IEEE1149.1 and IEEE1149.6 standards. The JTAG port must be accessible during platform initial laboratory bring-up, for manufacturing tests and troubleshooting, as well as for software debugging by authorized entities. The i.MX 6Dual/6Quad SJC incorporates three security modes for protecting against unauthorized accesses. Modes are selected through eFUSE configuration.
SNVS	Secure Non-Volatile Storage	Security	Secure Non-Volatile Storage, including Secure Real Time Clock, Security State Machine, Master Key Control, and Violation/Tamper Detection and reporting.
SPDIF	Sony Philips Digital Interconnect Format	Multimedia Peripherals	A standard audio file transfer format, developed jointly by the Sony and Phillips corporations. It supports Transmitter and Receiver functionality.

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
WDOG-2 (TZ)	Watchdog (TrustZone)	Timer Peripherals	The TrustZone Watchdog (TZ WDOG) timer module protects against TrustZone starvation by providing a method of escaping normal mode and forcing a switch to the TZ mode. TZ starvation is a situation where the normal OS prevents switching to the TZ mode. Such a situation is undesirable as it can compromise the system's security. Once the TZ WDOG module is activated, it must be serviced by TZ software on a periodic basis. If servicing does not take place, the timer times out. Upon a time-out, the TZ WDOG asserts a TZ mapped interrupt that forces switching to the TZ mode. If it is still not served, the TZ WDOG asserts a security violation signal to the CSU. The TZ WDOG module cannot be programmed or deactivated by a normal mode Software.
EIM	NOR-Flash /PSRAM interface	Connectivity Peripherals	The EIM NOR-FLASH / PSRAM provides: • Support 16-bit (in muxed IO mode only) PSRAM memories (sync and async operating modes), at slow frequency • Support 16-bit (in muxed IO mode only) NOR-Flash memories, at slow frequency • Multiple chip selects
XTALOSC	Crystal Oscillator interface	—	The XTALOSC module enables connectivity to external crystal oscillator device. In a typical application use-case, it is used for 24 MHz oscillator.

3.1 Special Signal Considerations

The package contact assignments can be found in Section 6, "Package Information and Contact Assignments." Signal descriptions are defined in the i.MX 6Dual/6Quad reference manual (IMX6DQRM). Special signal consideration information is contained in the Hardware Development Guide for i.MX 6Quad, 6Dual, 6DualLite, 6Solo Families of Applications Processors (IMX6DQ6SDLHDG).

3.2 Recommended Connections for Unused Analog Interfaces

The recommended connections for unused analog interfaces can be found in the section, "Unused analog interfaces," of the Hardware Development Guide for i.MX 6Quad, 6Dual, 6DualLite, 6Solo Families of Applications Processors (IMX6DQ6SDLHDG).

4.1.3 Operating Ranges

Table 6 provides the operating ranges of the i.MX 6Dual/6Quad processors.

Table 6. Operating Ranges

Parameter Description	Symbol	Min	Typ	Max[1]	Unit	Comment[2]
Run mode: LDO enabled	VDD_ARM_IN VDD_ARM23_IN[3]	1.35[4]	—	1.5	V	LDO Output Set Point (VDD_ARM_CAP[5]) of 1.225 V minimum for operation up to 852 MHz or 996 MHz (depending on the device speed grade).
		1.275[4]	—	1.5	V	LDO Output Set Point (VDD_ARM_CAP[5]) of 1.150 V minimum for operation up to 792 MHz.
		1.05[4]	—	1.5	V	LDO Output Set Point (VDD_ARM_CAP[5]) of 0.925 V minimum for operation up to 396 MHz.
	VDD_SOC_IN[6]	1.350[4]	—	1.5	V	264 MHz < VPU ≤ 352 MHz; VDDSOC and VDDPU LDO outputs (VDD_SOC_CAP and VDD_PU_CAP) require 1.225 V minimum.
		1.275[4,7]	—	1.5	V	VPU ≤ 264 MHz; VDDSOC and VDDPU LDO outputs (VDD_SOC_CAP and VDD_PU_CAP) require 1.15 V minimum.
Run mode: LDO bypassed[8]	VDD_ARM_IN VDD_ARM23_IN[3]	1.225	—	1.3	V	LDO bypassed for operation up to 852 MHz or 996 MHz (depending on the device speed grade).
		1.150	—	1.3	V	LDO bypassed for operation up to 792 MHz.
		0.925	—	1.3	V	LDO bypassed for operation up to 396 MHz.
	VDD_SOC_IN[6]	1.225	—	1.3	V	264 MHz < VPU ≤ 352 MHz
		1.15	—	1.3	V	VPU ≤ 264 MHz
Standby/DSM mode	VDD_ARM_IN VDD_ARM23_IN[3]	0.9	—	1.3	V	See Table 9, "Stop Mode Current and Power Consumption," on page 26.
	VDD_SOC_IN	0.9	—	1.3	V	
VDD_HIGH internal regulator	VDD_HIGH_IN[9]	2.7	—	3.3	V	Must match the range of voltages that the rechargeable backup battery supports.
Backup battery supply range	VDD_SNVS_IN[9]	2.8	—	3.3	V	Should be supplied from the same supply as VDD_HIGH_IN, if the system does not require keeping real time and other data on OFF state.
USB supply voltages	USB_OTG_VBUS	4.4	—	5.25	V	—
	USB_H1_VBUS	4.4	—	5.25	V	—
DDR I/O supply	NVCC_DRAM	1.14	1.2	1.3	V	LPDDR2
		1.425	1.5	1.575	V	DDR3
		1.283	1.35	1.45	V	DDR3_L
Supply for RGMII I/O power group[10]	NVCC_RGMII	1.15	—	2.625	V	• 1.15 V – 1.30 V in HSIC 1.2 V mode • 1.43 V – 1.58 V in RGMII 1.5 V mode • 1.70 V – 1.90 V in RGMII 1.8 V mode • 2.25 V – 2.625 V in RGMII 2.5 V mode

4.2 Power Supplies Requirements and Restrictions

The system design must comply with power-up sequence, power-down sequence, and steady state guidelines as described in this section to ensure the reliable operation of the device. Any deviation from these sequences may result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting
- Irreversible damage to the processor

4.2.1 Power-Up Sequence

For power-up sequence, the restrictions are as follows:

- VDD_SNVS_IN supply must be turned ON before any other power supply. It may be connected (shorted) with VDD_HIGH_IN supply.
- If a coin cell is used to power VDD_SNVS_IN, then ensure that it is connected before any other supply is switched on.
- If the external SRC_POR_B signal is used to control the processor POR, then SRC_POR_B must be immediately asserted at power-up and remain asserted until the VDD_ARM_CAP, VDD_SOC_CAP, and VDD_PU_CAP supplies are stable. VDD_ARM_IN and VDD_SOC_IN may be applied in either order with no restrictions. In the absence of an external reset feeding the SRC_POR_B input, the internal POR module takes control. See the i.MX 6Dual/6Quad reference manual (IMX6DQRM) for further details and to ensure that all necessary requirements are being met.
- If the external SRC_POR_B signal is not used (always held high or left unconnected), the processor defaults to the internal POR function (where the PMU controls generation of the POR based on the power supplies). If the internal POR function is used, the following power supply requirements must be met:
  - VDD_ARM_IN and VDD_SOC_IN may be supplied from the same source, or
  - VDD_SOC_IN can be supplied before VDD_ARM_IN with a maximum delay of 1 ms.

NOTE

Ensure that there is no back voltage (leakage) from any supply on the board towards the 3.3 V supply (for example, from the external components that use both the 1.8 V and 3.3 V supplies).

NOTE

USB_OTG_VBUS and USB_H1_VBUS are not part of the power supply sequence and can be powered at any time.

4.2.2 Power-Down Sequence

No special restrictions for i.MX 6Dual/6Quad SoC.

from either a ~3 V backup battery (VDD_SNVS_IN) or VDD_HIGH_IN such as the oscillator consumes power from VDD_HIGH_IN when that supply is available and transitions to the back up battery when VDD_HIGH_IN is lost.

In addition, if the clock monitor determines that the OSC32K is not present, then the source of the 32 kHz clock will automatically switch to the internal ring oscillator.

CAUTION

The internal RTC oscillator does not provide an accurate frequency and is affected by process, voltage, and temperature variations. Freescale strongly recommends using an external crystal as the RTC_XTALI reference. If the internal oscillator is used instead, careful consideration must be given to the timing implications on all of the SoC modules dependent on this clock.

The OSC32k runs from VDD_SNVS_CAP, which comes from the VDD_HIGH_IN/VDD_SNVS_IN power mux. The target battery is a ~3 V coin cell. Proper choice of coin cell type is necessary for chosen VDD_HIGH_IN range. Appropriate series resistor (Rs) must be used when connecting the coin cell. Rs depends on the charge current limit that depends on the chosen coin cell. For example, for Panasonic ML621:

- Average Discharge Voltage is 2.5 V
- Maximum Charge Current is 0.6 mA

For a charge voltage of 3.2 V, Rs = (3.2-2.5)/0.6 m = 1.17 k

NOTE

Always refer to the chosen coin cell manufacturer's data sheet for the latest information.

Table 20. OSC32K Main Characteristics

Parameter	Min	Typ	Max	Comments
Fosc	—	32.768 kHz	—	This frequency is nominal and determined mainly by the crystal selected. 32.0 K would work as well.
Current consumption	—	4 µA	—	The typical value shown is only for the oscillator, driven by an external crystal. If the internal ring oscillator is used instead of an external crystal, then approximately 25 µA should be added to this value.
Bias resistor	—	14 MΩ	—	This the integrated bias resistor that sets the amplifier into a high gain state. Any leakage through the ESD network, external board leakage, or even a scope probe that is significant relative to this value will debias the amplifier. The debiasing will result in low gain, and will impact the circuit's ability to start up and maintain oscillations.
Target Crystal Properties				
Cload	—	10 pF	—	Usually crystals can be purchased tuned for different Cloads. This Cload value is typically 1/2 of the capacitances realized on the PCB on either side of the quartz. A higher Cload will decrease oscillation margin, but increases current oscillating through the crystal.
ESR	—	50 kΩ	100 kΩ	Equivalent series resistance of the crystal. Choosing a crystal with a higher value will decrease the oscillating margin.

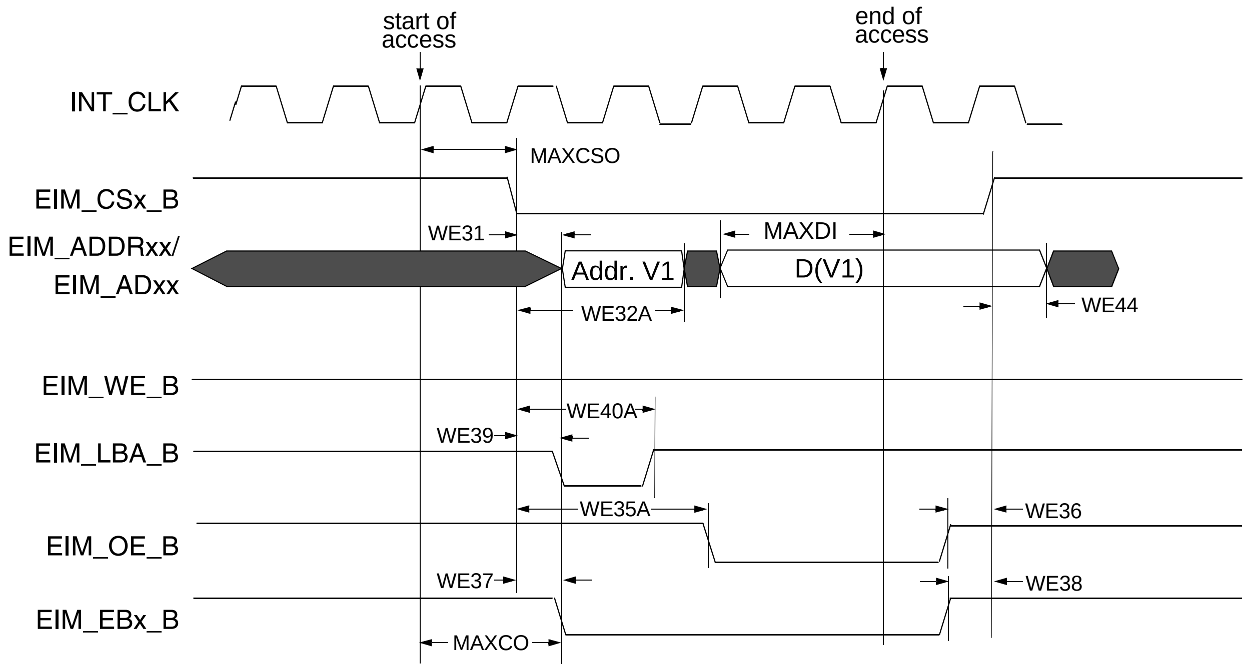

Figure 19. Asynchronous A/D Muxed Read Access (RWSC = 5)

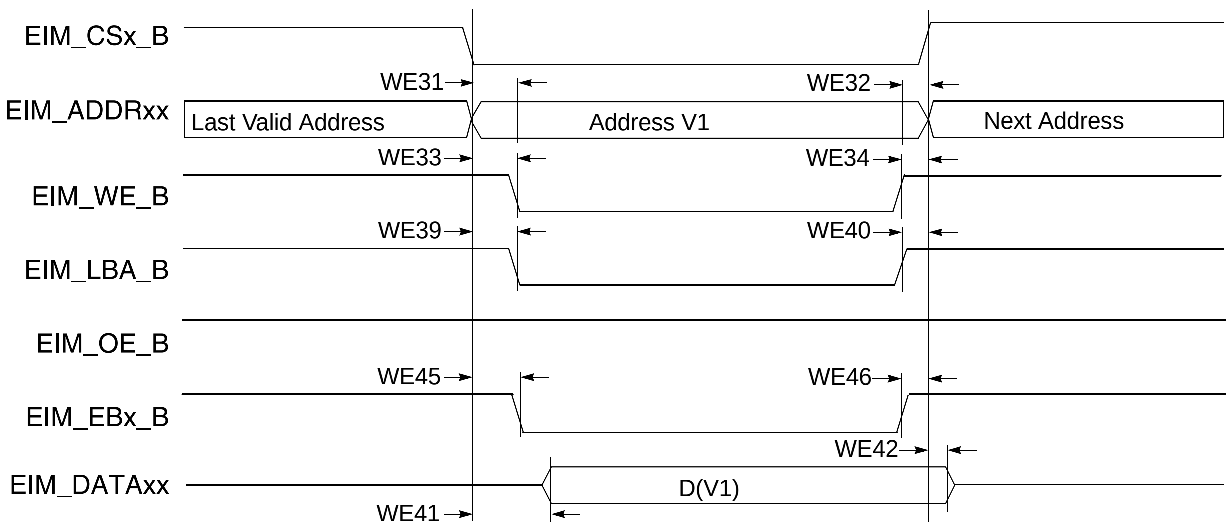

Figure 20. Asynchronous Memory Write Access

4.11.3 Enhanced Serial Audio Interface (ESAI) Timing Parameters

The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. Table 53 shows the interface timing values. The number field in the table refers to timing signals found in Figure 43 and Figure 44.

Table 53. Enhanced Serial Audio Interface (ESAI) Timing

ID	Parameter[1,2]	Symbol	Expression[2]	Min	Max	Condition[3]	Unit
62	Clock cycle[4]	t_{SSICC}	$4 \times T_C$ $4 \times T_C$	30.0 30.0	— —	i ck i ck	ns
63	Clock high period: • For internal clock • For external clock	— —	$2 \times T_C - 9.0$ $2 \times T_C$	6 15	— —	— —	ns
64	Clock low period: • For internal clock • For external clock	— —	$2 \times T_C - 9.0$ $2 \times T_C$	6 15	— —	— —	ns
65	ESAI_RX_CLK rising edge to ESAI_RX_FS out (bl) high	— —	— —	— —	19.0 7.0	x ck i ck a	ns
66	ESAI_RX_CLK rising edge to ESAI_RX_FS out (bl) low	— —	— —	— —	19.0 7.0	x ck i ck a	ns
67	ESAI_RX_CLK rising edge to ESAI_RX_FS out (wr) high[5]	— —	— —	— —	19.0 9.0	x ck i ck a	ns
68	ESAI_RX_CLK rising edge to ESAI_RX_FS out (wr) low[5]	— —	— —	— —	19.0 9.0	x ck i ck a	ns
69	ESAI_RX_CLK rising edge to ESAI_RX_FS out (wl) high	— —	— —	— —	19.0 6.0	x ck i ck a	ns
70	ESAI_RX_CLK rising edge to ESAI_RX_FSout (wl) low	— —	— —	— —	17.0 7.0	x ck i ck a	ns
71	Data in setup time before ESAI_RX_CLK (serial clock in synchronous mode) falling edge	— —	— —	12.0 19.0	— —	x ck i ck	ns
72	Data in hold time after ESAI_RX_CLK falling edge	— —	— —	3.5 9.0	— —	x ck i ck	ns
73	ESAI_RX_FS input (bl, wr) high before ESAI_RX_CLK falling edge[5]	— —	— —	2.0 19.0	— —	x ck i ck a	ns
74	ESAI_RX_FS input (wl) high before ESAI_RX_CLK falling edge	— —	— —	2.0 19.0	— —	x ck i ck a	ns
75	ESAI_RX_FS input hold time after ESAI_RX_CLK falling edge	— —	— —	2.5 8.5	— —	x ck i ck a	ns
78	ESAI_TX_CLK rising edge to ESAI_TX_FS out (bl) high	— —	— —	— —	19.0 8.0	x ck i ck	ns
79	ESAI_TX_CLK rising edge to ESAI_TX_FS out (bl) low	— —	— —	— —	20.0 10.0	x ck i ck	ns
80	ESAI_TX_CLK rising edge to ESAI_TX_FS out (wr) high[5]	— —	— —	— —	20.0 10.0	x ck i ck	ns

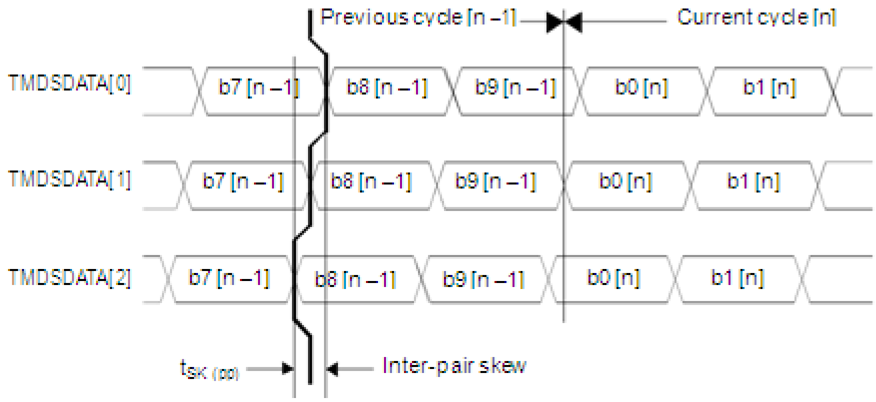

Figure 62. Inter-Pair Skew Definition

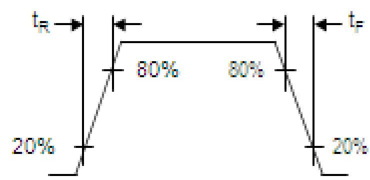

Figure 63. TMDS Output Signals Rise and Fall Time Definition

Table 64. Switching Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TMDS Drivers Specifications						
—	Maximum serial data rate	—	—	—	3.4	Gbps
$F_{TMDSCLK}$	TMDSCLK frequency	On TMDSCLKP/N outputs	25	—	340	MHz
$P_{TMDSCLK}$	TMDSCLK period	RL = 50 Ω See Figure 59.	2.94	—	40	ns
t_{CDC}	TMDSCLK duty cycle	$t_{CDC} = t_{CPH} / P_{TMDSCLK}$ RL = 50 Ω See Figure 59.	40	50	60	%
t_{CPH}	TMDSCLK high time	RL = 50 Ω See Figure 59.	4	5	6	UI
t_{CPL}	TMDSCLK low time	RL = 50 Ω See Figure 59.	4	5	6	UI
—	TMDSCLK jitter[1]	RL = 50 Ω	—	—	0.25	UI
$t_{SK(p)}$	Intra-pair (pulse) skew	RL = 50 Ω See Figure 61.	—	—	0.15	UI
$t_{SK(pp)}$	Inter-pair skew	RL = 50 Ω See Figure 62.	—	—	1	UI
t_R	Differential output signal rise time	20–80% RL = 50 Ω See Figure 63.	75	—	0.4 UI	ps

4.11.10.3 Electrical Characteristics

Figure 67 depicts the sensor interface timing. IPU2_CSIx_PIX_CLK signal described here is not generated by the IPU. Table 67 lists the sensor interface timing characteristics.

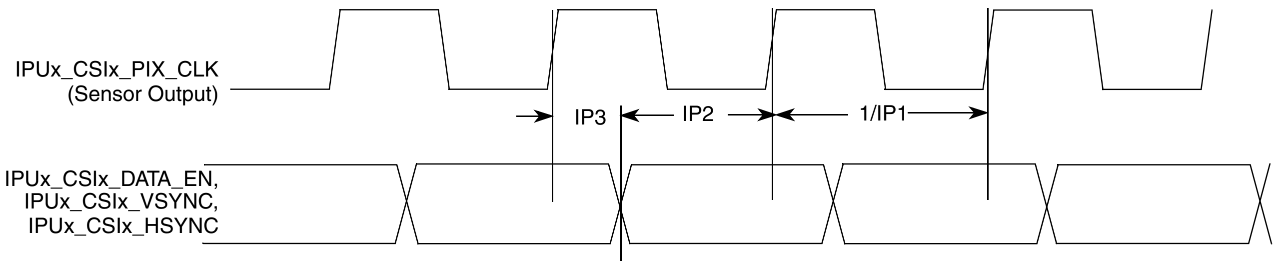

Figure 67. Sensor Interface Timing Diagram

Table 67. Sensor Interface Timing Characteristics

ID	Parameter	Symbol	Min	Max	Unit
IP1	Sensor output (pixel) clock frequency	Fpck	0.01	180	MHz
IP2	Data and control setup time	Tsu	2	—	ns
IP3	Data and control holdup time	Thd	1	—	ns

4.11.10.4 IPU Display Interface Signal Mapping

The IPU supports a number of display output video formats. Table 68 defines the mapping of the Display Interface Pins used during various supported video interface formats.

Table 68. Video Signal Cross-Reference

i.MX 6Dual/6Quad	LCD							Comment[1,2]
Port Name (x = 0, 1)	RGB, Signal Name (General)	RGB/TV Signal Allocation (Example)						
		16-bit RGB	18-bit RGB	24 Bit RGB	8-bit YCrCb[3]	16-bit YCrCb	20-bit YCrCb	
IPUx_DISPx_DAT00	DAT[0]	B[0]	B[0]	B[0]	Y/C[0]	C[0]	C[0]	—
IPUx_DISPx_DAT01	DAT[1]	B[1]	B[1]	B[1]	Y/C[1]	C[1]	C[1]	—
IPUx_DISPx_DAT02	DAT[2]	B[2]	B[2]	B[2]	Y/C[2]	C[2]	C[2]	—
IPUx_DISPx_DAT03	DAT[3]	B[3]	B[3]	B[3]	Y/C[3]	C[3]	C[3]	—
IPUx_DISPx_DAT04	DAT[4]	B[4]	B[4]	B[4]	Y/C[4]	C[4]	C[4]	—
IPUx_DISPx_DAT05	DAT[5]	G[0]	B[5]	B[5]	Y/C[5]	C[5]	C[5]	—
IPUx_DISPx_DAT06	DAT[6]	G[1]	G[0]	B[6]	Y/C[6]	C[6]	C[6]	—

- The ipp_pin_1– ipp_pin_7 are general purpose synchronous pins, that can be used to provide HSYNC, VSYNC, DRDY or any else independent signal to a display.

The IPU has a system of internal binding counters for internal events (such as, HSYNC/VSYNC) calculation. The internal event (local start point) is synchronized with internal DI_CLK. A suitable control starts from the local start point with predefined UP and DOWN values to calculate control's changing points with half DI_CLK resolution. A full description of the counter system can be found in the IPU chapter of the i.MX 6Dual/6Quad reference manual (IMX6DQRM).

4.11.10.5.2 Asynchronous Controls

The asynchronous control is a data-oriented signal that changes its value with an output data according to additional internal flags coming with the data.

There are special physical outputs to provide asynchronous controls, as follows:

- The ipp_d0_cs and ipp_d1_cs pins are dedicated to provide chip select signals to two displays.
- The ipp_pin_11– ipp_pin_17 are general purpose asynchronous pins, that can be used to provide WR. RD, RS or any other data-oriented signal to display.

NOTE

The IPU has independent signal generators for asynchronous signals toggling. When a DI decides to put a new asynchronous data on the bus, a new internal start (local start point) is generated. The signal generators calculate predefined UP and DOWN values to change pins states with half DI_CLK resolution.

4.11.10.6 Synchronous Interfaces to Standard Active Matrix TFT LCD Panels

4.11.10.6.1 IPU Display Operating Signals

The IPU uses four control signals and data to operate a standard synchronous interface:

- IPP_DISP_CLK—Clock to display
- HSYNC—Horizontal synchronization
- VSYNC—Vertical synchronization
- DRDY—Active data

All synchronous display controls are generated on the base of an internally generated "local start point". The synchronous display controls can be placed on time axis with DI's offset, up and down parameters. The display access can be whole number of DI clock (Tdiclk) only. The IPP_DATA can not be moved relative to the local start point. The data bus of the synchronous interface is output direction only.

4.11.10.6.2 LCD Interface Functional Description

Figure 68 depicts the LCD interface timing for a generic active matrix color TFT panel. In this figure, signals are shown with negative polarity. The sequence of events for active matrix interface timing is:

- DI_CLK internal DI clock is used for calculation of other controls.

4.11.13.9 DATA and FLAG Signal Timing

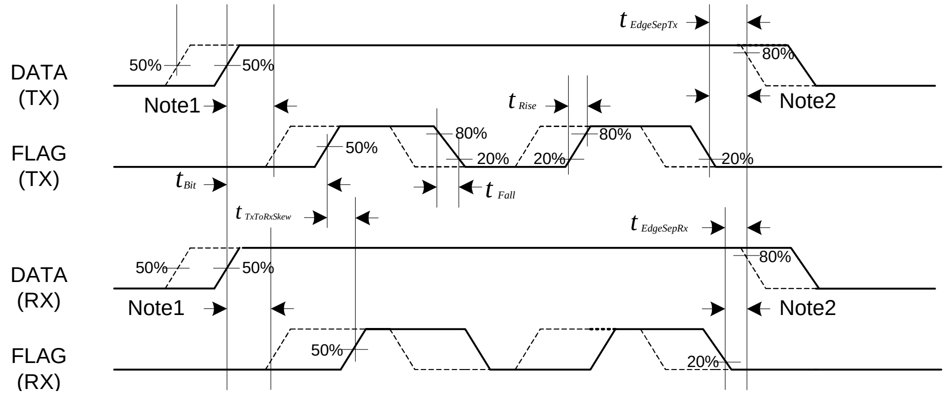

Figure 86. DATA and FLAG Signal Timing

4.11.14 MediaLB (MLB) Characteristics

4.11.14.1 MediaLB (MLB) DC Characteristics

Table 75 lists the MediaLB 3-pin interface electrical characteristics.

Table 75. MediaLB 3-Pin Interface Electrical DC Specifications

Parameter	Symbol	Test Conditions	Min	Max	Unit
Maximum input voltage	—	—	—	3.6	V
Low level input threshold	V_{IL}	—	—	0.7	V
High level input threshold	V_{IH}	See Note[1]	1.8	—	V
Low level output threshold	V_{OL}	I_{OL} = 6 mA	—	0.4	V
High level output threshold	V_{OH}	I_{OH} = –6 mA	2.0	—	V
Input leakage current	I_L	$0 < V_{in} < VDD$	—	±10	µA

1 Higher V_{IH} thresholds can be used; however, the risks associated with less noise margin in the system must be evaluated and assumed by the customer.

Table 76 lists the MediaLB 6-pin interface electrical characteristics.

Table 76. MediaLB 6-Pin Interface Electrical DC Specifications

Parameter	Symbol	Test Conditions	Min	Max	Unit
Driver Characteristics					
Differential output voltage (steady-state): $\lvert V_{O+} - V_{O-} \rvert$	V_{OD}	See Note[1]	300	500	mV
Difference in differential output voltage between (high/low) steady-states: $\lvert V_{OD, high} - V_{OD, low} \rvert$	ΔV_{OD}	—	-50	50	mV

4.11.20.2 SSI Receiver Timing with Internal Clock

Figure 97 depicts the SSI receiver internal clock timing and Table 87 lists the timing parameters for the receiver timing with the internal clock.

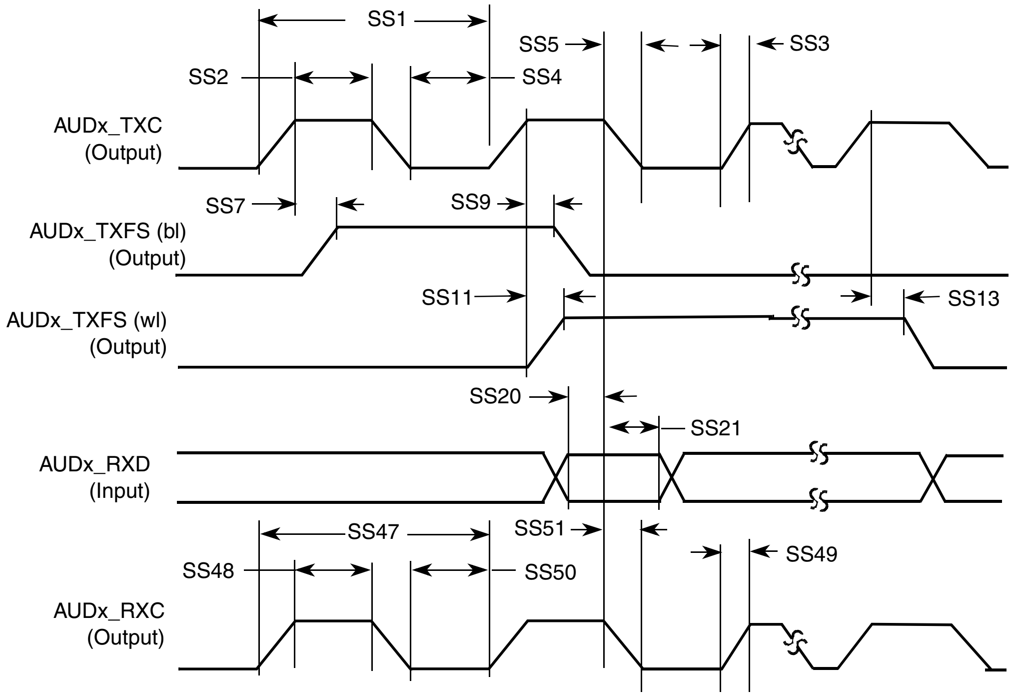

Figure 97. SSI Receiver Internal Clock Timing Diagram

Table 87. SSI Receiver Timing with Internal Clock

ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	AUDx_TXC/AUDx_RXC clock period	81.4	—	ns
SS2	AUDx_TXC/AUDx_RXC clock high period	36.0	—	ns
SS3	AUDx_TXC/AUDx_RXC clock rise time	—	6.0	ns
SS4	AUDx_TXC/AUDx_RXC clock low period	36.0	—	ns
SS5	AUDx_TXC/AUDx_RXC clock fall time	—	6.0	ns
SS7	AUDx_RXC high to AUDx_TXFS (bl) high	—	15.0	ns
SS9	AUDx_RXC high to AUDx_TXFS (bl) low	—	15.0	ns
SS11	AUDx_RXC high to AUDx_TXFS (wl) high	—	15.0	ns
SS13	AUDx_RXC high to AUDx_TXFS (wl) low	—	15.0	ns
SS20	AUDx_RXD setup time before AUDx_RXC low	10.0	—	ns
SS21	AUDx_RXD hold time after AUDx_RXC low	0.0	—	ns

4.11.20.3 SSI Transmitter Timing with External Clock

Figure 98 depicts the SSI transmitter external clock timing and Table 88 lists the timing parameters for the transmitter timing with the external clock.

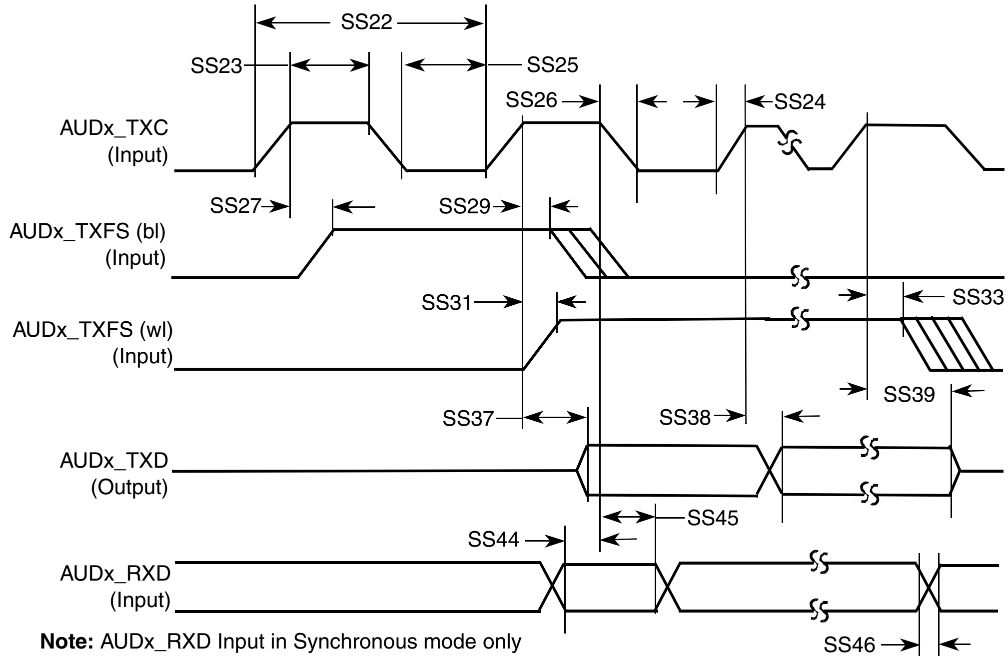

Figure 98. SSI Transmitter External Clock Timing Diagram

Table 88. SSI Transmitter Timing with External Clock

ID	Parameter	Min	Max	Unit
	External Clock Operation			
SS22	AUDx_TXC/AUDx_RXC clock period	81.4	—	ns
SS23	AUDx_TXC/AUDx_RXC clock high period	36.0	—	ns
SS24	AUDx_TXC/AUDx_RXC clock rise time	—	6.0	ns
SS25	AUDx_TXC/AUDx_RXC clock low period	36.0	—	ns
SS26	AUDx_TXC/AUDx_RXC clock fall time	—	6.0	ns
SS27	AUDx_TXC high to AUDx_TXFS (bl) high	–10.0	15.0	ns
SS29	AUDx_TXC high to AUDx_TXFS (bl) low	10.0	—	ns
SS31	AUDx_TXC high to AUDx_TXFS (wl) high	–10.0	15.0	ns
SS33	AUDx_TXC high to AUDx_TXFS (wl) low	10.0	—	ns
SS37	AUDx_TXC high to AUDx_TXD valid from high impedance	—	15.0	ns
SS38	AUDx_TXC high to AUDx_TXD high/low	—	15.0	ns
SS39	AUDx_TXC high to AUDx_TXD high impedance	—	15.0	ns

Table 88. SSI Transmitter Timing with External Clock (continued)

ID	Parameter	Min	Max	Unit
Synchronous External Clock Operation				
SS44	AUDx_RXD setup before AUDx_TXC falling	10.0	—	ns
SS45	AUDx_RXD hold after AUDx_TXC falling	2.0	—	ns
SS46	AUDx_RXD rise/fall time	—	6.0	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal AUDx_TXC/AUDx_RXC and/or the frame sync AUDx_TXFS/AUDx_RXFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- AUDx_TXC and AUDx_RXC refer to the Transmit and Receive sections of the SSI.
- The terms WL and BL refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the frame sync timing is same as that of transmit data (for example, during AC97 mode of operation).

4.11.20.4 SSI Receiver Timing with External Clock

Figure 99 depicts the SSI receiver external clock timing and Table 89 lists the timing parameters for the receiver timing with the external clock.

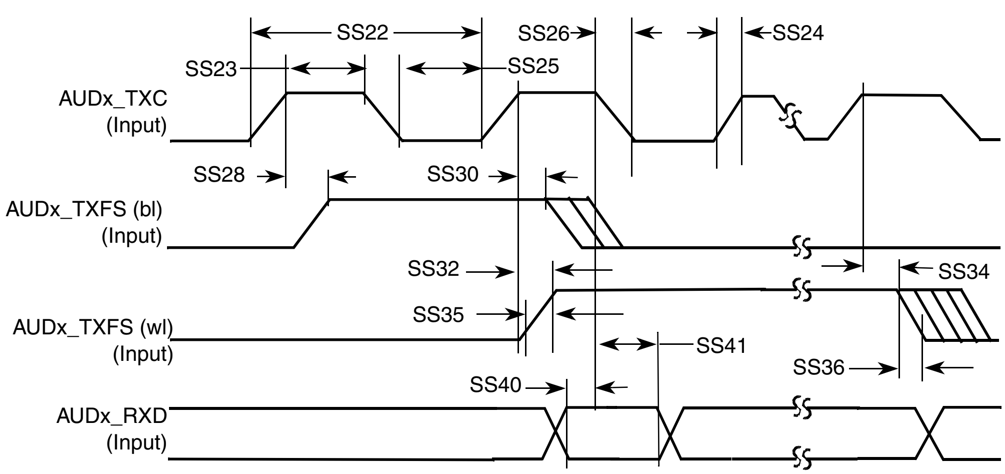

Figure 99. SSI Receiver External Clock Timing Diagram

6.2.2 21 x 21 mm Ground, Power, Sense, and Reference Contact Assignments

Table 99 shows the device connection list for ground, power, sense, and reference contact signals.

Table 99. 21 x 21 mm Supplies Contact Assignment

Supply Rail Name	Ball(s) Position(s)	Remark
CSI_REXT	D4	—
DRAM_VREF	AC2	—
DSI_REXT	G4	—
FA_ANA	A5	—
GND	A13, A25, A4, A8, AA10, AA13, AA16, AA19, AA22, AD4, D3, F8, J15, L10, M15, P15, T15, U8, W17, AA7, AD7, D6, G10, J18, L12, M18, P18, T17, V19, W18, AB24, AE1, D8, G19, J2, L15, M8, P8, T19, V8, W19, AB3, AE25, E5, G3, J8, L18, N10, R12, T8, W10, W3, AD10, B4, E6, H12, K10, L2, N15, R15, U11, W11, W7, AD13, C1, E7, H15, K12, L5, N18, R17, U12, W12, W8, AD16, C10, F5, H18, K15, L8, N8, R8, U15, W13, W9, AD19, C4, F6, H8, K18, M10, P10, T11, U17, W15, Y24, AD22, C6, F7, J12, K8, M12, P12, T12, U19, W16, Y5	—
GPANAIO	C8	—
HDMI_DDCCEC	K2	Analog ground reference for the Hot Plug detect signal
HDMI_REF	J1	—
HDMI_VP	L7	—
HDMI_VPH	M7	—
NVCC_CSI	N7	Supply of the camera sensor interface
NVCC_DRAM	R18, T18, U18, V10, V11, V12, V13, V14, V15, V16, V17, V18, V9	Supply of the DDR interface
NVCC_EIM0	K19	Supply of the EIM interface
NVCC_EIM1	L19	Supply of the EIM interface
NVCC_EIM2	M19	Supply of the EIM interface
NVCC_ENET	R19	Supply of the ENET interface
NVCC_GPIO	P7	Supply of the GPIO interface
NVCC_JTAG	J7	Supply of the JTAG tap controller interface
NVCC_LCD	P19	Supply of the LCD interface
NVCC_LVDS2P5	V7	Supply of the LVDS display interface and DDR pre-drivers. Even if the LVDS interface is not used, this supply must remain powered.
NVCC_MIPI	K7	Supply of the MIPI interface

Table 100. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function (Signal Name)	Input/Output	Value[2]
CSI_D3P	F1	NVCC_MIPI	—	—	CSI_DATA3_P	—	—
CSI0_DAT10	M1	NVCC_CSI	GPIO	ALT5	GPIO5_IO28	Input	PU (100K)
CSI0_DAT11	M3	NVCC_CSI	GPIO	ALT5	GPIO5_IO29	Input	PU (100K)
CSI0_DAT12	M2	NVCC_CSI	GPIO	ALT5	GPIO5_IO30	Input	PU (100K)
CSI0_DAT13	L1	NVCC_CSI	GPIO	ALT5	GPIO5_IO31	Input	PU (100K)
CSI0_DAT14	M4	NVCC_CSI	GPIO	ALT5	GPIO6_IO00	Input	PU (100K)
CSI0_DAT15	M5	NVCC_CSI	GPIO	ALT5	GPIO6_IO01	Input	PU (100K)
CSI0_DAT16	L4	NVCC_CSI	GPIO	ALT5	GPIO6_IO02	Input	PU (100K)
CSI0_DAT17	L3	NVCC_CSI	GPIO	ALT5	GPIO6_IO03	Input	PU (100K)
CSI0_DAT18	M6	NVCC_CSI	GPIO	ALT5	GPIO6_IO04	Input	PU (100K)
CSI0_DAT19	L6	NVCC_CSI	GPIO	ALT5	GPIO6_IO05	Input	PU (100K)
CSI0_DAT4	N1	NVCC_CSI	GPIO	ALT5	GPIO5_IO22	Input	PU (100K)
CSI0_DAT5	P2	NVCC_CSI	GPIO	ALT5	GPIO5_IO23	Input	PU (100K)
CSI0_DAT6	N4	NVCC_CSI	GPIO	ALT5	GPIO5_IO24	Input	PU (100K)
CSI0_DAT7	N3	NVCC_CSI	GPIO	ALT5	GPIO5_IO25	Input	PU (100K)
CSI0_DAT8	N6	NVCC_CSI	GPIO	ALT5	GPIO5_IO26	Input	PU (100K)
CSI0_DAT9	N5	NVCC_CSI	GPIO	ALT5	GPIO5_IO27	Input	PU (100K)
CSI0_DATA_EN	P3	NVCC_CSI	GPIO	ALT5	GPIO5_IO20	Input	PU (100K)
CSI0_MCLK	P4	NVCC_CSI	GPIO	ALT5	GPIO5_IO19	Input	PU (100K)
CSI0_PIXCLK	P1	NVCC_CSI	GPIO	ALT5	GPIO5_IO18	Input	PU (100K)
CSI0_VSYNC	N2	NVCC_CSI	GPIO	ALT5	GPIO5_IO21	Input	PU (100K)
DI0_DISP_CLK	N19	NVCC_LCD	GPIO	ALT5	GPIO4_IO16	Input	PU (100K)
DI0_PIN15	N21	NVCC_LCD	GPIO	ALT5	GPIO4_IO17	Input	PU (100K)
DI0_PIN2	N25	NVCC_LCD	GPIO	ALT5	GPIO4_IO18	Input	PU (100K)
DI0_PIN3	N20	NVCC_LCD	GPIO	ALT5	GPIO4_IO19	Input	PU (100K)
DI0_PIN4	P25	NVCC_LCD	GPIO	ALT5	GPIO4_IO20	Input	PU (100K)
DISP0_DAT0	P24	NVCC_LCD	GPIO	ALT5	GPIO4_IO21	Input	PU (100K)
DISP0_DAT1	P22	NVCC_LCD	GPIO	ALT5	GPIO4_IO22	Input	PU (100K)
DISP0_DAT10	R21	NVCC_LCD	GPIO	ALT5	GPIO4_IO31	Input	PU (100K)
DISP0_DAT11	T23	NVCC_LCD	GPIO	ALT5	GPIO5_IO05	Input	PU (100K)
DISP0_DAT12	T24	NVCC_LCD	GPIO	ALT5	GPIO5_IO06	Input	PU (100K)
DISP0_DAT13	R20	NVCC_LCD	GPIO	ALT5	GPIO5_IO07	Input	PU (100K)
DISP0_DAT14	U25	NVCC_LCD	GPIO	ALT5	GPIO5_IO08	Input	PU (100K)
DISP0_DAT15	T22	NVCC_LCD	GPIO	ALT5	GPIO5_IO09	Input	PU (100K)
DISP0_DAT16	T21	NVCC_LCD	GPIO	ALT5	GPIO5_IO10	Input	PU (100K)
DISP0_DAT17	U24	NVCC_LCD	GPIO	ALT5	GPIO5_IO11	Input	PU (100K)

Table 100. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function (Signal Name)	Input/Output	Value[2]
DISP0_DAT18	V25	NVCC_LCD	GPIO	ALT5	GPIO5_IO12	Input	PU (100K)
DISP0_DAT19	U23	NVCC_LCD	GPIO	ALT5	GPIO5_IO13	Input	PU (100K)
DISP0_DAT2	P23	NVCC_LCD	GPIO	ALT5	GPIO4_IO23	Input	PU (100K)
DISP0_DAT20	U22	NVCC_LCD	GPIO	ALT5	GPIO5_IO14	Input	PU (100K)
DISP0_DAT21	T20	NVCC_LCD	GPIO	ALT5	GPIO5_IO15	Input	PU (100K)
DISP0_DAT22	V24	NVCC_LCD	GPIO	ALT5	GPIO5_IO16	Input	PU (100K)
DISP0_DAT23	W24	NVCC_LCD	GPIO	ALT5	GPIO5_IO17	Input	PU (100K)
DISP0_DAT3	P21	NVCC_LCD	GPIO	ALT5	GPIO4_IO24	Input	PU (100K)
DISP0_DAT4	P20	NVCC_LCD	GPIO	ALT5	GPIO4_IO25	Input	PU (100K)
DISP0_DAT5	R25	NVCC_LCD	GPIO	ALT5	GPIO4_IO26	Input	PU (100K)
DISP0_DAT6	R23	NVCC_LCD	GPIO	ALT5	GPIO4_IO27	Input	PU (100K)
DISP0_DAT7	R24	NVCC_LCD	GPIO	ALT5	GPIO4_IO28	Input	PU (100K)
DISP0_DAT8	R22	NVCC_LCD	GPIO	ALT5	GPIO4_IO29	Input	PU (100K)
DISP0_DAT9	T25	NVCC_LCD	GPIO	ALT5	GPIO4_IO30	Input	PU (100K)
DRAM_A0	AC14	NVCC_DRAM	DDR	ALT0	DRAM_ADDR00	Output	0
DRAM_A1	AB14	NVCC_DRAM	DDR	ALT0	DRAM_ADDR01	Output	0
DRAM_A10	AA15	NVCC_DRAM	DDR	ALT0	DRAM_ADDR10	Output	0
DRAM_A11	AC12	NVCC_DRAM	DDR	ALT0	DRAM_ADDR11	Output	0
DRAM_A12	AD12	NVCC_DRAM	DDR	ALT0	DRAM_ADDR12	Output	0
DRAM_A13	AC17	NVCC_DRAM	DDR	ALT0	DRAM_ADDR13	Output	0
DRAM_A14	AA12	NVCC_DRAM	DDR	ALT0	DRAM_ADDR14	Output	0
DRAM_A15	Y12	NVCC_DRAM	DDR	ALT0	DRAM_ADDR15	Output	0
DRAM_A2	AA14	NVCC_DRAM	DDR	ALT0	DRAM_ADDR02	Output	0
DRAM_A3	Y14	NVCC_DRAM	DDR	ALT0	DRAM_ADDR03	Output	0
DRAM_A4	W14	NVCC_DRAM	DDR	ALT0	DRAM_ADDR04	Output	0
DRAM_A5	AE13	NVCC_DRAM	DDR	ALT0	DRAM_ADDR05	Output	0
DRAM_A6	AC13	NVCC_DRAM	DDR	ALT0	DRAM_ADDR06	Output	0
DRAM_A7	Y13	NVCC_DRAM	DDR	ALT0	DRAM_ADDR07	Output	0
DRAM_A8	AB13	NVCC_DRAM	DDR	ALT0	DRAM_ADDR08	Output	0
DRAM_A9	AE12	NVCC_DRAM	DDR	ALT0	DRAM_ADDR09	Output	0
DRAM_CAS	AE16	NVCC_DRAM	DDR	ALT0	DRAM_CAS_B	Output	0
DRAM_CS0	Y16	NVCC_DRAM	DDR	ALT0	DRAM_CS0_B	Output	0
DRAM_CS1	AD17	NVCC_DRAM	DDR	ALT0	DRAM_CS1_B	Output	0
DRAM_D0	AD2	NVCC_DRAM	DDR	ALT0	DRAM_DATA00	Input	PU (100K)
DRAM_D1	AE2	NVCC_DRAM	DDR	ALT0	DRAM_DATA01	Input	PU (100K)
DRAM_D10	AA6	NVCC_DRAM	DDR	ALT0	DRAM_DATA10	Input	PU (100K)

Table 102. 21 x 21 mm, 0.8 mm Pitch Ball Map (continued)

	E	F	G	H	J	K	L
1	CSI_D2M	CSI_D3P	DSI_D0P	DSI_D1P	HDMI_REF	HDMI_HPD	CSI0_DAT13
2	CSI_D2P	CSI_D3M	DSI_D0M	DSI_D1M	GND	HDMI_DDCCEC	GND
3	CSI_D0P	CSI_CLK0P	GND	DSI_CLK0M	HDMI_D1M	HDMI_D2M	CSI0_DAT17
4	CSI_D0M	CSI_CLK0M	DSI_REXT	DSI_CLK0P	HDMI_D1P	HDMI_D2P	CSI0_DAT16
5	GND	GND	JTAG_TDI	JTAG_TCK	HDMI_CLKM	HDMI_D0M	GND
6	GND	GND	JTAG_TDO	JTAG_MOD	HDMI_CLKP	HDMI_D0P	CSI0_DAT19
7	GND	GND	PCIE_VPH	PCIE_VP	NVCC_JTAG	NVCC_MIPI	HDMI_VP
8	NVCC_PLL_OUT	GND	PCIE_VPTX	GND	GND	GND	GND
9	USB_OTG_VBUS	VDDUSB_CAP	VDD_SNVS_CAP	VDDHIGH_IN	VDDHIGH_IN	VDDARM23_IN	VDDARM23_IN
10	USB_H1_DP	USB_H1_DN	GND	VDDHIGH_CAP	VDDHIGH_CAP	GND	GND
11	TAMPER	PMIC_STBY_REQ	VDD_SNVS_IN	VDDARM23_CAP	VDDARM23_CAP	VDDARM23_CAP	VDDARM23_CAP
12	TEST_MODE	BOOT_MODE1	SATA_VPH	GND	GND	GND	GND
13	SD3_DAT6	SD3_DAT7	SATA_VP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP
14	SD3_DAT0	SD3_DAT1	NVCC_SD3	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN
15	NANDF_WP_B	NANDF_CS0	NVCC_NANDF	GND	GND	GND	GND
16	SD4_CLK	NANDF_D2	NVCC_SD1	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN
17	NANDF_D6	SD4_DAT2	NVCC_SD2	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP
18	SD4_DAT4	SD1_DAT3	NVCC_RGMII	GND	GND	GND	GND
19	SD1_DAT2	SD2_CMD	GND	EIM_A25	EIM_D29	NVCC_EIM0	NVCC_EIM1
20	SD2_DAT1	RGMII_TD1	EIM_D20	EIM_D21	EIM_D30	EIM_RW	EIM_DA0
21	RGMII_TD2	EIM_D17	EIM_D19	EIM_D31	EIM_A23	EIM_EB0	EIM_DA2
22	EIM_EB2	EIM_D24	EIM_D25	EIM_A20	EIM_A18	EIM_LBA	EIM_DA4
23	EIM_D22	EIM_EB3	EIM_D28	EIM_A21	EIM_CS1	EIM_EB1	EIM_DA5
24	EIM_D26	EIM_A22	EIM_A17	EIM_CS0	EIM_OE	EIM_DA3	EIM_DA8
25	EIM_D27	EIM_A24	EIM_A19	EIM_A16	EIM_DA1	EIM_DA6	EIM_DA7

7 Revision History

Table 103 provides a revision history for this data sheet.

Table 103. i.MX 6Dual/6Quad Data Sheet Document Revision History

Rev. Number	Date	Substantive Change(s)
4	07/2015	• Added footnote to Table 1, "Example Orderable Part Numbers," on page 3: If a 24 MHz input clock is used (required for USB), the maximum SoC speed is limited to 996 MHz. • Section 1.2, "Features" changed Five UARTs, from *up to 4.0 Mbps*, to *up to 5.0 Mbps.* • Table 6, "Operating Ranges," on page 21: Row: VDD_HIGH internal regulator, changed minimum parameter value from 2.8 to 2.7V. • Table 6, "Operating Ranges," on page 21: Removed footnote: *VDDSOC and VDDPU output voltages must be set according to this rule: VDDARM-VDDSOC/PU<50mV.* This was a duplicate footnote, renumbered footnotes accordingly. • Table 6, "Operating Ranges," on page 21: Changed value: *Standby/DSM Mode, VDD_SOC_IN, minimum voltage, from 0.9V to 1.05V.* • Table 8, "Maximum Supply Currents," on page 25, Differentiated VDD_ARM_IN, VDD_ARM23_IN, and VDD_SOC_IN by frequency and by Power Virus/CoreMark maximum current. • Table 21, "XTALI and RTC_XTALI DC Parameters," on page 38, Added rows: *Input capacitance*; *Startup current*; and *DC input current* and their values. • Table 40, "EIM Bus Timing Parameters," on page 53, Changed WE4–WE17 minimum and maximum parameter values from, *0.5 t (k+1)/2-1.25*, to *0.5 x t x (k+1)-1.25.* • Table 41, "EIM Asynchronous Timing Parameters Relative to Chip Select," on page 60 Added to end of formulas in the minimum, typical, and maximum parameter values for WE31–WE42 and WE45–WE46, $\times t$. For example from *3-CSN*, to *3-CSN*$\times t$. Also added maximum value to MAXDTI of 10. • Table 43, "DDR3/DDR3L Write Cycle," on page 63, Changed minimum parameter value of DDR17 from 240 to 125; and of DDR18 from 240 to 150. • Figure 27, "LPDDR2 Command and Address Timing Diagram," on page 64, LP2 signal cycle reduced. • Table 46, "LPDDR2 Write Cycle," on page 65, Changed LP21 minimum and maximum parameter value from -0.25/+0.25 to 0.8/1.2. • Figure 41, "ECSPI Master Mode Timing Diagram," on page 76, Added footnote: *Note: ECSPIx_MOSI is always driven (not tri-stated) between actual data transmissions. This limits the ECSPI to be connected between a single master and a single slave.* • Figure 42, "ECSPI Slave Mode Timing Diagram," on page 77, Added footnote: *Note: ECSPIx_MISO is always driven (not tri-stated) between actual data transmissions. This limits the ECSPI to be connected between a single master and a single slave.* • Figure 65, "Gated Clock Mode Timing Diagram," on page 98, Corrected IPU2_CSIx_HSYNC trace drawing. • Section 4.11.23, "USB PHY Parameters" Specified *Battery Charging Specification* applies to portable devices only.