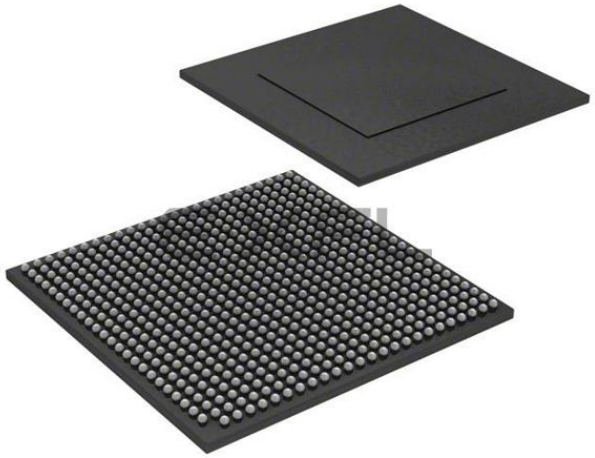

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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | ARM® Cortex®-A9 |
| Number of Cores/Bus Width | 4 Core, 32-Bit |
| Speed | 852MHz |
| Co-Processors/DSP | Multimedia; NEON™ SIMD |
| RAM Controllers | LPDDR2, LVDDR3, DDR3 |
| Graphics Acceleration | Yes |
| Display & Interface Controllers | Keypad, LCD |
| Ethernet | 10/100/1000Mbps (1) |
| SATA | SATA 3Gbps (1) |
| USB | USB 2.0 + PHY (4) |
| Voltage - I/O | 1.8V, 2.5V, 2.8V, 3.3V |
| Operating Temperature | -40°C ~ 125°C (TJ) |
| Security Features | ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection |
| Package / Case | 624-FBGA, FCBGA |
| Supplier Device Package | 624-FCBGA (21x21) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6q6avt08ac |

### 4.7.1 General Purpose I/O AC Parameters

The I/O AC parameters for GPIO in slow and fast modes are presented in the Table 27 and Table 28, respectively. Note that the fast or slow I/O behavior is determined by the appropriate control bits in the IOMUXC control registers.

**Table 27. General Purpose I/O AC Parameters 1.8 V Mode**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output Pad Transition Times, rise/fall (Max Drive, ipp_dse=111) | tr, tf | 15 pF Cload, slow slew rate<br>15 pF Cload, fast slew rate | — | — | 2.72/2.79<br>1.51/1.54 | ns |
| Output Pad Transition Times, rise/fall (High Drive, ipp_dse=101) | tr, tf | 15 pF Cload, slow slew rate<br>15 pF Cload, fast slew rate | — | — | 3.20/3.36<br>1.96/2.07 | |
| Output Pad Transition Times, rise/fall (Medium Drive, ipp_dse=100) | tr, tf | 15 pF Cload, slow slew rate<br>15 pF Cload, fast slew rate | — | — | 3.64/3.88<br>2.27/2.53 | |
| Output Pad Transition Times, rise/fall (Low Drive. ipp_dse=011) | tr, tf | 15 pF Cload, slow slew rate<br>15 pF Cload, fast slew rate | — | — | 4.32/4.50<br>3.16/3.17 | |
| Input Transition Times[1] | trm | — | — | — | 25 | ns |

1 Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

**Table 28. General Purpose I/O AC Parameters 3.3 V Mode**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output Pad Transition Times, rise/fall (Max Drive, ipp_dse=101) | tr, tf | 15 pF Cload, slow slew rate<br>15 pF Cload, fast slew rate | — | — | 1.70/1.79<br>1.06/1.15 | ns |
| Output Pad Transition Times, rise/fall (High Drive, ipp_dse=011) | tr, tf | 15 pF Cload, slow slew rate<br>15 pF Cload, fast slew rate | — | — | 2.35/2.43<br>1.74/1.77 | |
| Output Pad Transition Times, rise/fall (Medium Drive, ipp_dse=010) | tr, tf | 15 pF Cload, slow slew rate<br>15 pF Cload, fast slew rate | — | — | 3.13/3.29<br>2.46/2.60 | |
| Output Pad Transition Times, rise/fall (Low Drive. ipp_dse=001) | tr, tf | 15 pF Cload, slow slew rate<br>15 pF Cload, fast slew rate | — | — | 5.14/5.57<br>4.77/5.15 | |
| Input Transition Times[1] | trm | — | — | — | 25 | ns |

1 Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

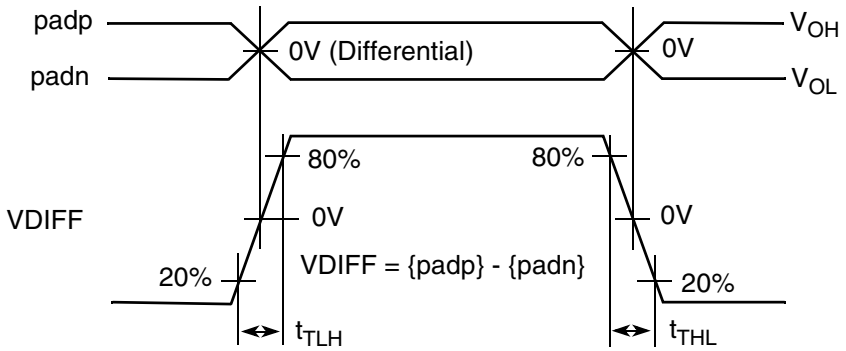


**Figure 7. Differential MLB Driver Transition Time Waveform**

A 4-stage pipeline is used in the MLB 6-pin implementation to facilitate design, maximize throughput, and allow for reasonable PCB trace lengths. Each cycle is one ipp_clk_in* (internal clock from MLB PLL) clock period. Cycles 2, 3, and 4 are MLB PHY related. Cycle 2 includes clock-to-output delay of Signal/Data sampling flip-flop and Transmitter, Cycle 3 includes clock-to-output delay of Signal/Data clocked receiver, Cycle 4 includes clock-to-output delay of Signal/Data sampling flip-flop.

MLB 6-pin pipeline diagram is shown in Figure 8.

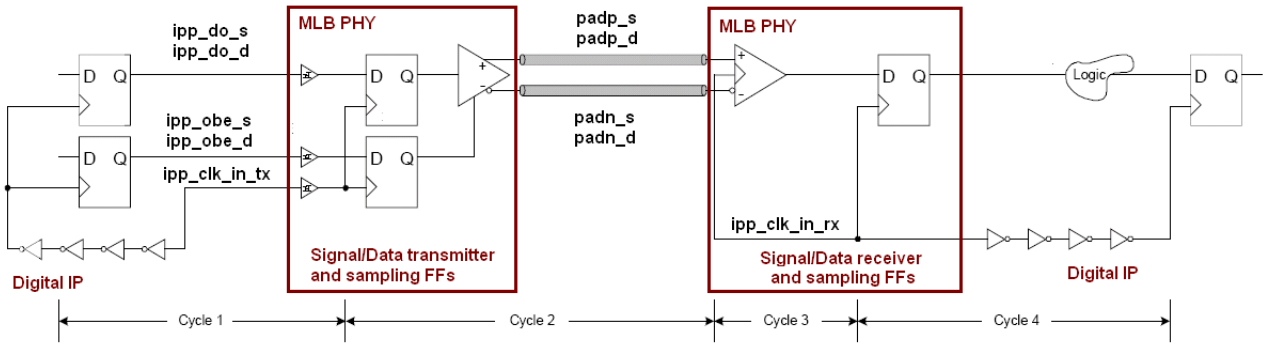


**Figure 8. MLB 6-Pin Pipeline Diagram**

Table 32 shows the AC parameters for MLB I/O.

**Table 32. I/O AC Parameters of MLB PHY**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Differential pulse skew[1] | $t_{SKD}$ | Rload = 50 Ω between padP and padN | — | — | 0.1 | ns |
| Transition Low to High Time[2] | $t_{TLH}$ | | — | — | 1 | |
| Transition High to Low Time | $t_{THL}$ | | — | — | 1 | |
| MLB external clock Operating Frequency | fclk_ext | — | — | — | 102.4 | MHz |
| MLB PLL clock Operating Frequency | fclk_pll | — | — | — | 307.2 | MHz |

1 $t_{SKD} = | t_{PHLD} - t_{PLHD} |$, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.

2 Measurement levels are 20-80% from output voltage.

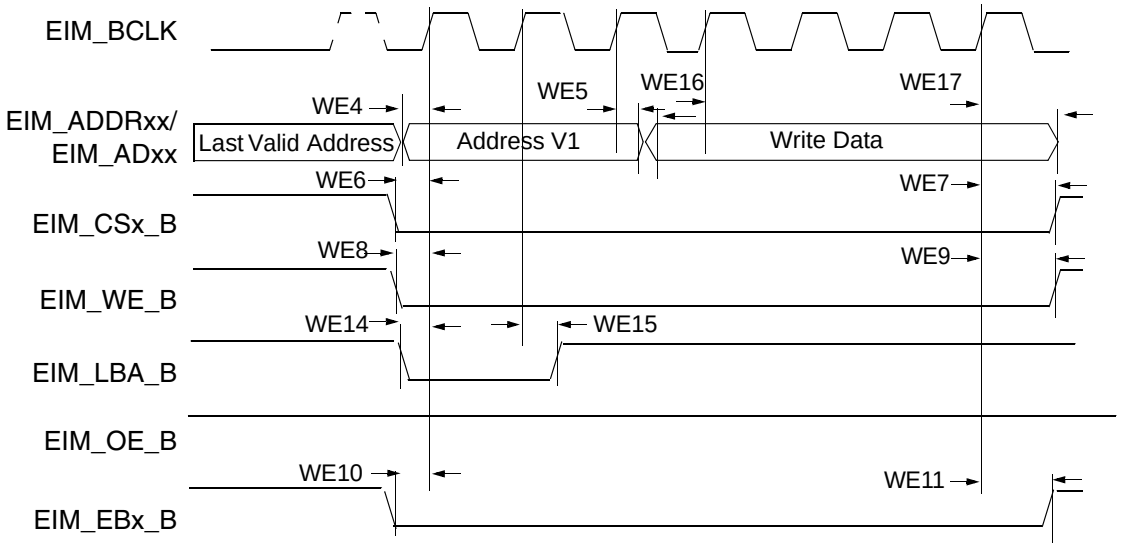


**Figure 16. Muxed Address/Data (A/D) Mode, Synchronous Write Access, WSC=6,ADVA=0, ADVN=1, and ADH=1**

### NOTE

In 32-bit muxed address/data (A/D) mode the 16 MSBs are driven on the data bus.

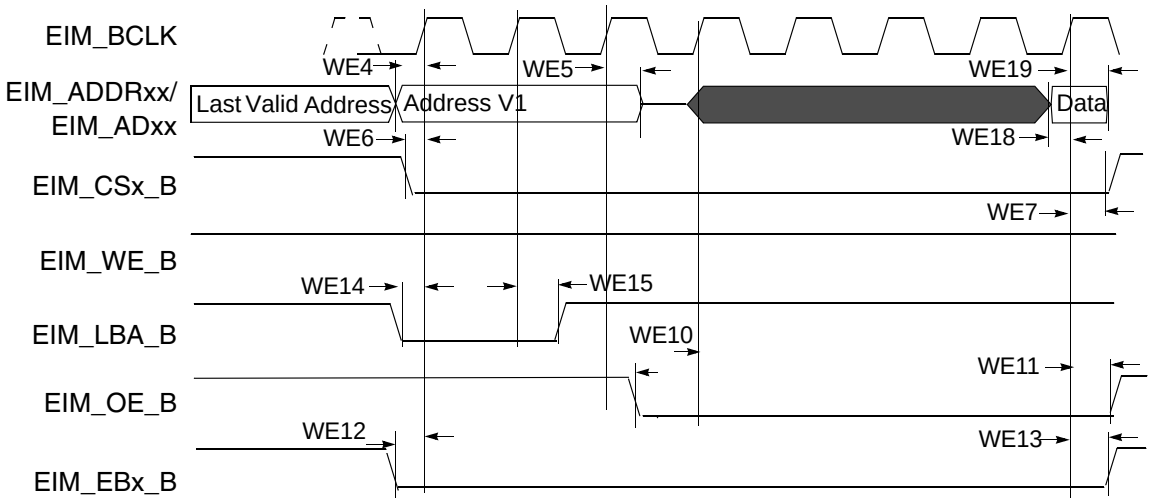


**Figure 17. 16-Bit Muxed A/D Mode, Synchronous Read Access, WSC=7, RADVN=1, ADH=1, OEA=0**

**Table 42. DDR3/DDR3L Timing Parameter (continued)**

| ID | Parameter[1,2] | Symbol | CK = 532 MHz | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| DDR4 | DRAM_CSx_B, DRAM_RAS_B, DRAM_CAS_B, DRAM_SDCKEx, DRAM_SDWE_B, DRAM_ODTx setup time | tIS | 500 | — | ps |
| DDR5 | DRAM_CSx_B, DRAM_RAS_B, DRAM_CAS_B, DRAM_SDCKEx, DRAM_SDWE_B, DRAM_ODTx hold time | tIH | 400 | — | ps |
| DDR6 | Address output setup time | tIS | 500 | — | ps |
| DDR7 | Address output hold time | tIH | 400 | — | ps |

1 All measurements are in reference to Vref level.

2 Measurements were done using balanced load and 25 Ω resistor from outputs to DRAM_VREF.

Figure 25 shows the DDR3/DDR3L write timing diagram. The timing parameters for this diagram appear in Table 43.

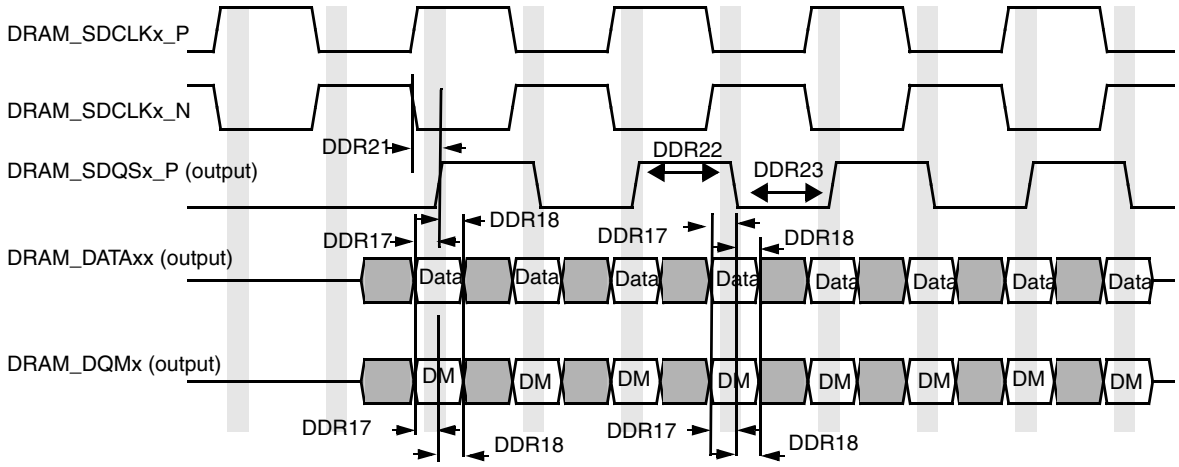


**Figure 25. DDR3/DDR3L Write Cycle**

**Table 43. DDR3/DDR3L Write Cycle**

| ID | Parameter[1,2,3] | Symbol | CK = 532 MHz | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| DDR17 | DRAM_DATAxx and DRAM_DQMx setup time to DRAM_SDQSx_P (differential strobe) | tDS | 125[4] | — | ps |
| DDR18 | DRAM_DATAxx and DRAM_DQMx hold time to DRAM_SDQSx_P (differential strobe) | tDH | 150[4] | — | ps |
| DDR21 | DRAM_SDQSx_P latching rising transitions to associated clock edges | tDQSS | -0.25 | +0.25 | tCK |
| DDR22 | DRAM_SDQSx_P high level width | tDQSH | 0.45 | 0.55 | tCK |
| DDR23 | DRAM_SDQSx_P low level width | tDQSL | 0.45 | 0.55 | tCK |

1 To receive the reported setup and hold values, write calibration should be performed to locate the DRAM_SDQSx_P in the middle of DRAM_DATAxx window.

2 All measurements are in reference to Vref level.

3 Measurements were taken using balanced load and 25 Ω resistor from outputs to DRAM_VREF

### 4.10.1 Asynchronous Mode AC Timing (ONFI 1.0 Compatible)

Asynchronous mode AC timings are provided as multiplications of the clock cycle and fixed delay. The Maximum I/O speed of GPMI in Asynchronous mode is about 50 MB/s. Figure 30 through Figure 33 depict the relative timing between GPMI signals at the module level for different operations under Asynchronous mode. Table 48 describes the timing parameters (NF1–NF17) that are shown in the figures.

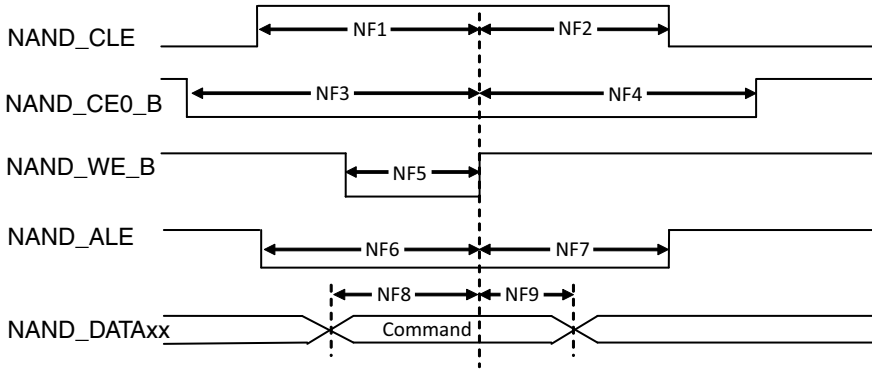


**Figure 30. Command Latch Cycle Timing Diagram**

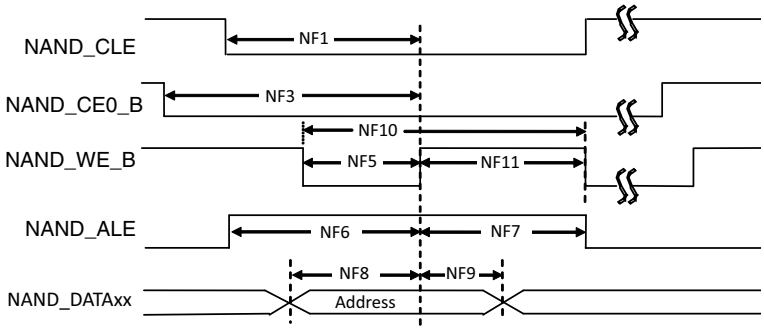


**Figure 31. Address Latch Cycle Timing Diagram**

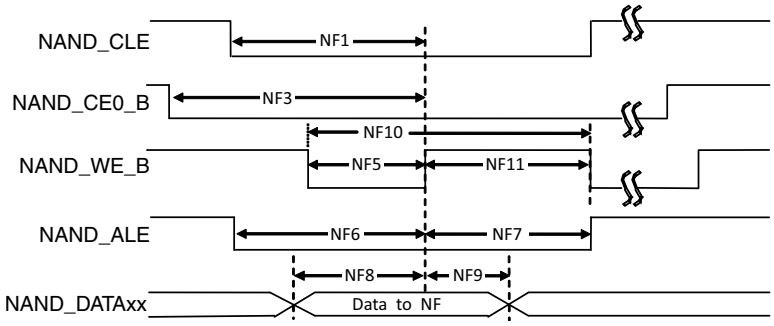


**Figure 32. Write Data Latch Cycle Timing Diagram**

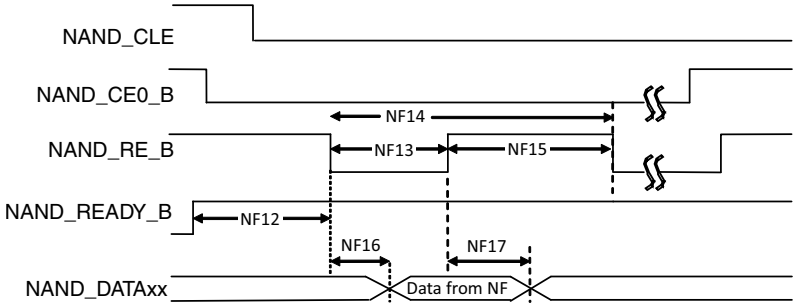


**Figure 33. Read Data Latch Cycle Timing Diagram (Non-EDO Mode)**

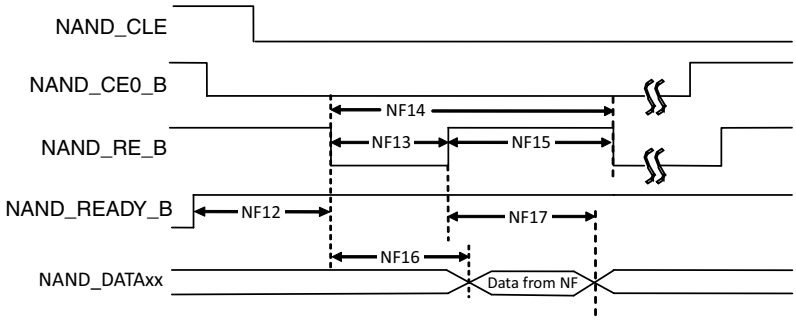


**Figure 34. Read Data Latch Cycle Timing Diagram (EDO Mode)**

**Table 48. Asynchronous Mode Timing Parameters[1]**

| ID | Parameter | Symbol | Timing T = GPMI Clock Cycle | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| NF1 | NAND_CLE setup time | tCLS | (AS + DS) × T - 0.12 [see [2,3]] | | ns |
| NF2 | NAND_CLE hold time | tCLH | DH × T - 0.72 [see [2]] | | ns |
| NF3 | NAND_CEx_B setup time | tCS | (AS + DS + 1) × T [see [3,2]] | | ns |
| NF4 | NAND_CEx_B hold time | tCH | (DH+1) × T - 1 [see [2]] | | ns |
| NF5 | NAND_WE_B pulse width | tWP | DS × T [see [2]] | | ns |
| NF6 | NAND_ALE setup time | tALS | (AS + DS) × T - 0.49 [see [3,2]] | | ns |
| NF7 | NAND_ALE hold time | tALH | (DH × T - 0.42 [see [2]] | | ns |
| NF8 | Data setup time | tDS | DS × T - 0.26 [see [2]] | | ns |
| NF9 | Data hold time | tDH | DH × T - 1.37 [see [2]] | | ns |
| NF10 | Write cycle time | tWC | (DS + DH) × T [see [2]] | | ns |
| NF11 | NAND_WE_B hold time | tWH | DH × T [see [2]] | | ns |
| NF12 | Ready to NAND_RE_B low | tRR[4] | (AS + 2) × T [see [3,2]] | — | ns |
| NF13 | NAND_RE_B pulse width | tRP | DS × T [see [2]] | | ns |
| NF14 | READ cycle time | tRC | (DS + DH) × T [see [2]] | | ns |
| NF15 | NAND_RE_B high hold time | tREH | DH × T [see [2]] | | ns |

## 4.10.3 Samsung Toggle Mode AC Timing

### 4.10.3.1 Command and Address Timing

Samsung Toggle mode command and address timing is the same as ONFI 1.0 compatible Async mode AC timing. See Section 4.10.1, “Asynchronous Mode AC Timing (ONFI 1.0 Compatible)” for details.

### 4.10.3.2 Read and Write Timing

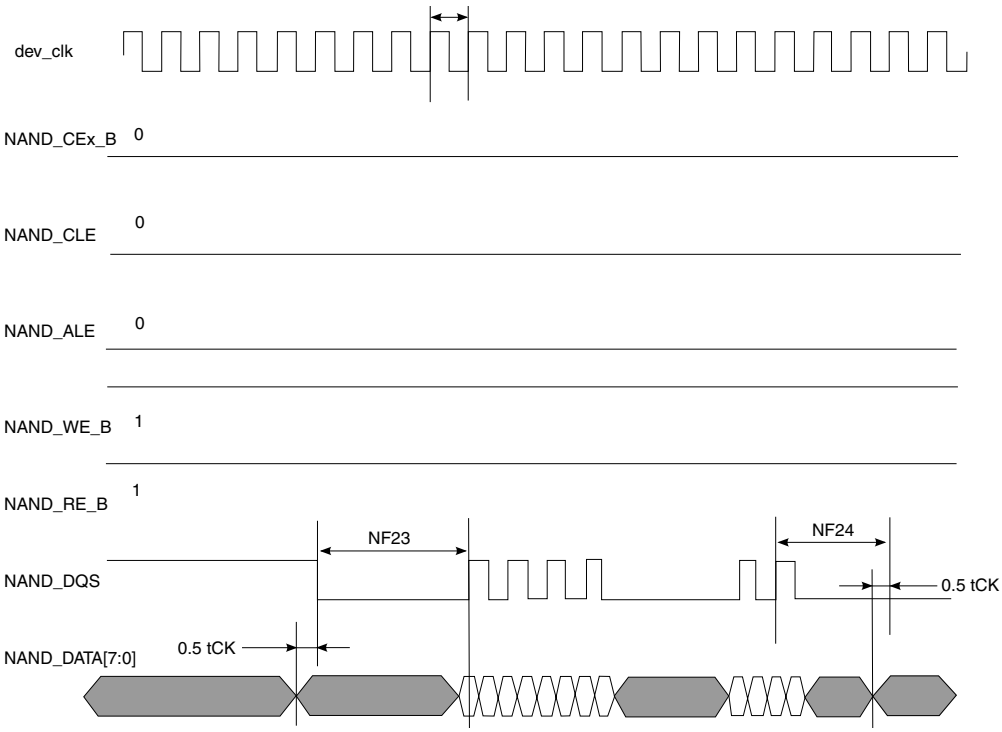


**Figure 39. Samsung Toggle Mode Data Write Timing**

#### 4.11.4.4 Bus Operation Condition for 3.3 V and 1.8 V Signaling

Signalling level of SD/eMMC4.3 and eMMC4.4/4.41 modes is 3.3 V. Signalling level of SDR104/SDR50 mode is 1.8 V. The DC parameters for the NVCC_SD1, NVCC_SD2, and NVCC_SD3 supplies are identical to those shown in Table 22, "GPIO I/O DC Parameters," on page 39.

### 4.11.5 Ethernet Controller (ENET) AC Electrical Specifications

#### 4.11.5.1 ENET MII Mode Timing

This subsection describes MII receive, transmit, asynchronous inputs, and serial management signal timings.

##### 4.11.5.1.1 MII Receive Signal Timing (ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER, and ENET_RX_CLK)

The receiver functions correctly up to an ENET_RX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. Additionally, the processor clock frequency must exceed twice the ENET_RX_CLK frequency.

Figure 48 shows MII receive signal timings. Table 57 describes the timing parameters (M1–M4) shown in the figure.

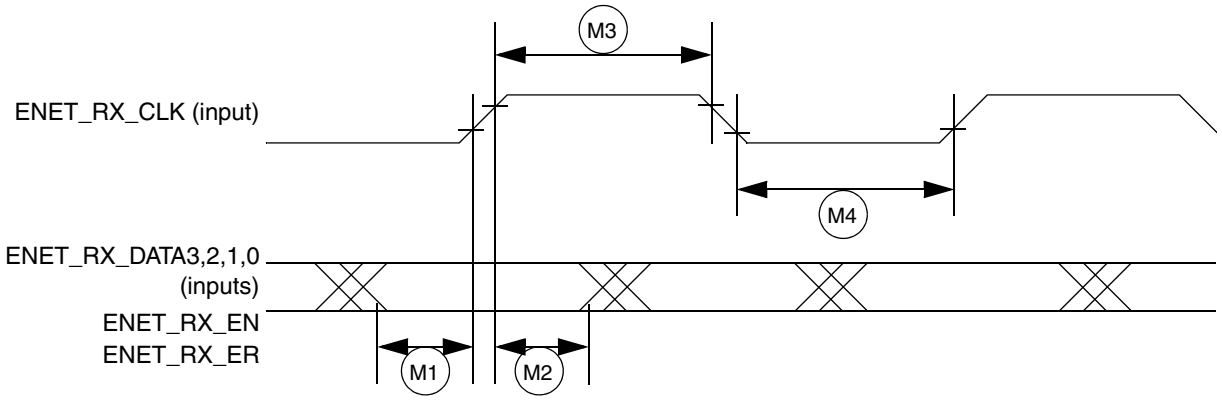


**Figure 48. MII Receive Signal Timing Diagram**

**Table 57. MII Receive Signal Timing**

| ID | Characteristic[1] | Min | Max | Unit |
|---|---|---|---|---|
| M1 | ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER to ENET_RX_CLK setup | 5 | — | ns |
| M2 | ENET_RX_CLK to ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER hold | 5 | — | ns |
| M3 | ENET_RX_CLK pulse width high | 35% | 65% | ENET_RX_CLK period |
| M4 | ENET_RX_CLK pulse width low | 35% | 65% | ENET_RX_CLK period |

[1] ENET_RX_EN, ENET_RX_CLK, and ENET0_RXD0 have the same timing in 10 Mbps 7-wire interface mode.

**Table 63. Electrical Characteristics (continued)**

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_T$ | Termination resistance | — | 45 | 50 | 55 | Ω |
| **TMDS drivers DC specifications** | | | | | | |
| $V_{OFF}$ | Single-ended standby voltage | RT = 50 Ω<br>For measurement conditions and definitions, see the first two figures above.<br>Compliance point TP1 as defined in the HDMI specification, version 1.3a, section 4.2.4. | avddtmds ± 10 mV | | | mV |
| $V_{SWING}$ | Single-ended output swing voltage | | 400 | — | 600 | mV |
| $V_H$ | Single-ended output high voltage<br>For definition, see the second figure above. | If attached sink supports TMDSCLK < or = 165 MHz | avddtmds ± 10 mV | | | mV |
| | | If attached sink supports TMDSCLK > 165 MHz | avddtmds – 200 mV | — | avddtmds + 10 mV | mV |
| $V_L$ | Single-ended output low voltage<br>For definition, see the second figure above. | If attached sink supports TMDSCLK < or = 165 MHz | avddtmds – 600 mV | — | avddtmds – 400mV | mV |
| | | If attached sink supports TMDSCLK > 165 MHz | avddtmds – 700 mV | — | avddtmds – 400 mV | mV |
| $R_{TERM}$ | Differential source termination load (inside HDMI 3D Tx PHY)<br>Although the HDMI 3D Tx PHY includes differential source termination, the user-defined value is set for each single line (for illustration, see the third figure above).<br>**Note:** $R_{TERM}$ can also be configured to be open and not present on TMDS channels. | — | 50 | — | 200 | Ω |
| **Hot plug detect specifications** | | | | | | |
| $HPD^{VH}$ | Hot plug detect high range | — | 2.0 | — | 5.3 | V |
| $VHPD_{VL}$ | Hot plug detect low range | — | 0 | — | 0.8 | V |
| $HPD_Z$ | Hot plug detect input impedance | — | 10 | — | — | kΩ |
| $HPD_t$ | Hot plug detect time delay | — | — | — | 100 | µs |

## 4.11.8 Switching Characteristics

Table 64 describes switching characteristics for the HDMI 3D Tx PHY. Figure 59 to Figure 63 illustrate various parameters specified in table.

**NOTE**

All dynamic parameters related to the TMDS line drivers' performance imply the use of assembly guidelines.

**Table 65. I²C Module Timing Parameters (continued)**

| ID | Parameter | Standard Mode | | Fast Mode | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| IC9 | Bus free time between a STOP and START condition | 4.7 | — | 1.3 | — | µs |
| IC10 | Rise time of both I2Cx_SDA and I2Cx_SCL signals | — | 1000 | $20 + 0.1C_b$[4] | 300 | ns |
| IC11 | Fall time of both I2Cx_SDA and I2Cx_SCL signals | — | 300 | $20 + 0.1C_b$[4] | 300 | ns |
| IC12 | Capacitive load for each bus line ($C_b$) | — | 400 | — | 400 | pF |

1 A device must internally provide a hold time of at least 300 ns for I2Cx_SDA signal to bridge the undefined region of the falling edge of I2Cx_SCL.

2 The maximum hold time has only to be met if the device does not stretch the LOW period (ID no IC5) of the I2Cx_SCL signal.

3 A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement of Set-up time (ID No IC7) of 250 ns must be met. This automatically is the case if the device does not stretch the LOW period of the I2Cx_SCL signal. If such a device does stretch the LOW period of the I2Cx_SCL signal, it must output the next data bit to the I2Cx_SDA line max_rise_time (IC9) + data_setup_time (IC7) = 1000 + 250 = 1250 ns (according to the Standard-mode I2C-bus specification) before the I2Cx_SCL line is released.

4 $C_b$ = total capacitance of one bus line in pF.

## 4.11.10 Image Processing Unit (IPU) Module Parameters

The purpose of the IPU is to provide comprehensive support for the flow of data from an image sensor and/or to a display device. This support covers all aspects of these activities:

- Connectivity to relevant devices—cameras, displays, graphics accelerators, and TV encoders.
- Related image processing and manipulation: sensor image signal processing, display processing, image conversions, and other related functions.
- Synchronization and control capabilities, such as avoidance of tearing artifacts.

**Table 68. Video Signal Cross-Reference (continued)**

| i.MX 6Dual/6Quad | LCD | | | | | | | Comment[1,2] |
|---|---|---|---|---|---|---|---|---|
| Port Name (x = 0, 1) | RGB, Signal Name (General) | RGB/TV Signal Allocation (Example) | | | | | | |
| | | 16-bit RGB | 18-bit RGB | 24 Bit RGB | 8-bit YCrCb[3] | 16-bit YCrCb | 20-bit YCrCb | |
| IPUx_DISPx_DAT07 | DAT[7] | G[2] | G[1] | B[7] | Y/C[7] | C[7] | C[7] | — |
| IPUx_DISPx_DAT08 | DAT[8] | G[3] | G[2] | G[0] | — | Y[0] | C[8] | — |
| IPUx_DISPx_DAT09 | DAT[9] | G[4] | G[3] | G[1] | — | Y[1] | C[9] | — |
| IPUx_DISPx_DAT10 | DAT[10] | G[5] | G[4] | G[2] | — | Y[2] | Y[0] | — |
| IPUx_DISPx_DAT11 | DAT[11] | R[0] | G[5] | G[3] | — | Y[3] | Y[1] | — |
| IPUx_DISPx_DAT12 | DAT[12] | R[1] | R[0] | G[4] | — | Y[4] | Y[2] | — |
| IPUx_DISPx_DAT13 | DAT[13] | R[2] | R[1] | G[5] | — | Y[5] | Y[3] | — |
| IPUx_DISPx_DAT14 | DAT[14] | R[3] | R[2] | G[6] | — | Y[6] | Y[4] | — |
| IPUx_DISPx_DAT15 | DAT[15] | R[4] | R[3] | G[7] | — | Y[7] | Y[5] | — |
| IPUx_DISPx_DAT16 | DAT[16] | — | R[4] | R[0] | — | — | Y[6] | — |
| IPUx_DISPx_DAT17 | DAT[17] | — | R[5] | R[1] | — | — | Y[7] | — |
| IPUx_DISPx_DAT18 | DAT[18] | — | — | R[2] | — | — | Y[8] | — |
| IPUx_DISPx_DAT19 | DAT[19] | — | — | R[3] | — | — | Y[9] | — |
| IPUx_DISPx_DAT20 | DAT[20] | — | — | R[4] | — | — | — | — |
| IPUx_DISPx_DAT21 | DAT[21] | — | — | R[5] | — | — | — | — |
| IPUx_DISPx_DAT22 | DAT[22] | — | — | R[6] | — | — | — | — |
| IPUx_DISPx_DAT23 | DAT[23] | — | — | R[7] | — | — | — | — |
| IPUx_DIx_DISP_CLK | PixCLK | | | | | | | — |
| IPUx_DIx_PIN01 | — | | | | | | | May be required for anti-tearing |
| IPUx_DIx_PIN02 | HSYNC | | | | | | | — |
| IPUx_DIx_PIN03 | VSYNC | | | | | | | VSYNC out |
| IPUx_DIx_PIN04 | — | | | | | | | Additional frame/row synchronous signals with programmable timing |
| IPUx_DIx_PIN05 | — | | | | | | | |
| IPUx_DIx_PIN06 | — | | | | | | | |
| IPUx_DIx_PIN07 | — | | | | | | | |
| IPUx_DIx_PIN08 | — | | | | | | | |

### 4.11.14.2 MediaLB (MLB) Controller AC Timing Electrical Specifications

This section describes the timing electrical information of the MediaLB module. Figure 87 show the timing of MediaLB 3-pin interface, and Table 77 and Table 78 lists the MediaLB 3-pin interface timing characteristics.

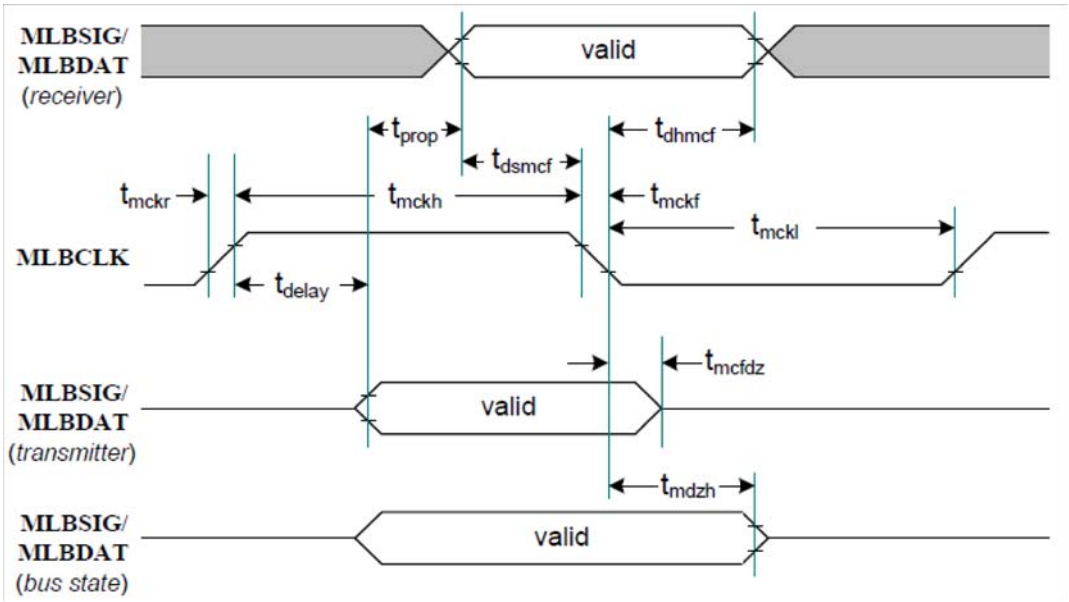


**Figure 87. MediaLB 3-Pin Timing**

Ground = 0.0 V; Load Capacitance = 60 pF; MediaLB speed = 256/512 Fs; Fs = 48 kHz; all timing parameters specified from the valid voltage threshold as listed below; unless otherwise noted.

**Table 77. MLB 256/512 Fs Timing Parameters**

| Parameter | Symbol | Min | Max | Unit | Comment |
|---|---|---|---|---|---|
| MLB_CLK operating frequency[1] | $f_{mck}$ | 11.264 | 25.6 | MHz | 256xFs at 44.0 kHz<br>512xFs at 50.0 kHz |
| MLB_CLK rise time | $t_{mckr}$ | — | 3 | ns | $V_{IL}$ TO $V_{IH}$ |
| MLB_CLK fall time | $t_{mckf}$ | — | 3 | ns | $V_{IH}$ TO $V_{IL}$ |
| MLB_CLK low time[2] | $t_{mckl}$ | 30<br>14 | — | ns | 256xFs<br>512xFs |
| MLB_CLK high time | $t_{mckh}$ | 30<br>14 | — | ns | 256xFs<br>512xFs |
| MLB_SIG/MLB_DATA receiver input valid to MLB_CLK falling | $t_{dsmcf}$ | 1 | — | ns | — |
| MLB_SIG/MLB_DATA receiver input hold from MLB_CLK low | $t_{dhmcf}$ | $t_{mdzh}$ | — | ns | — |
| MLB_SIG/MLB_DATA output high impedance from MLB_CLK low | $t_{mcfdz}$ | 0 | $t_{mckl}$ | ns | (see [3]) |

### 4.11.15.1 PCIE_REXT Reference Resistor Connection

The impedance calibration process requires connection of reference resistor 200 Ω. 1% precision resistor on PCIE_REXT pads to ground. It is used for termination impedance calibration.

## 4.11.16 Pulse Width Modulator (PWM) Timing Parameters

This section describes the electrical information of the PWM. The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMO) external pin.

Figure 89 depicts the timing of the PWM, and Table 80 lists the PWM timing parameters.

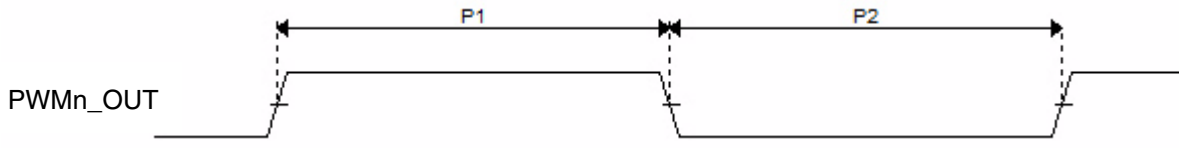


**Figure 89. PWM Timing**

**Table 80. PWM Output Timing Parameters**

| ID | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| — | PWM Module Clock Frequency | 0 | ipg_clk | MHz |
| P1 | PWM output pulse width high | 15 | — | ns |
| P2 | PWM output pulse width low | 15 | — | ns |

## 4.11.17 SATA PHY Parameters

This section describes SATA PHY electrical specifications.

### 4.11.17.1 Transmitter and Receiver Characteristics

The SATA PHY meets or exceeds the electrical compliance requirements defined in the SATA specifications.

**NOTE**

The tables in the following sections indicate any exceptions to the SATA specification or aspects of the SATA PHY that exceed the standard, as well as provide information about parameters not defined in the standard.

The following subsections provide values obtained from a combination of simulations and silicon characterization.

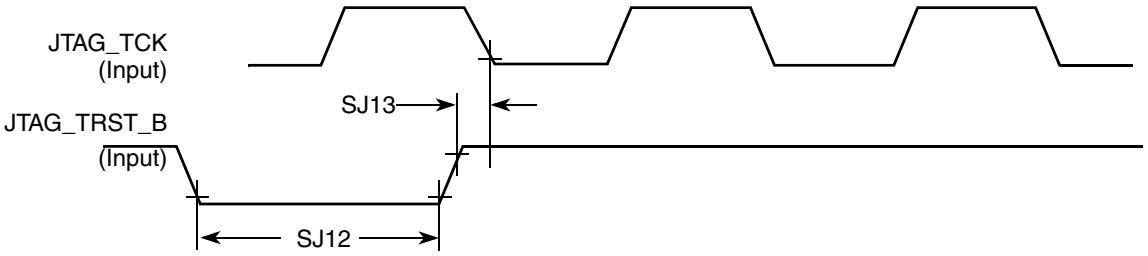


**Figure 93. JTAG_TRST_B Timing Diagram**

**Table 83. JTAG Timing**

| ID | Parameter[1,2] | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| SJ0 | JTAG_TCK frequency of operation $1/(3xT_{DC})$[1] | 0.001 | 22 | MHz |
| SJ1 | JTAG_TCK cycle time in crystal mode | 45 | — | ns |
| SJ2 | JTAG_TCK clock pulse width measured at $V_M$[2] | 22.5 | — | ns |
| SJ3 | JTAG_TCK rise and fall times | — | 3 | ns |
| SJ4 | Boundary scan input data set-up time | 5 | — | ns |
| SJ5 | Boundary scan input data hold time | 24 | — | ns |
| SJ6 | JTAG_TCK low to output data valid | — | 40 | ns |
| SJ7 | JTAG_TCK low to output high impedance | — | 40 | ns |
| SJ8 | JTAG_TMS, JTAG_TDI data set-up time | 5 | — | ns |
| SJ9 | JTAG_TMS, JTAG_TDI data hold time | 25 | — | ns |
| SJ10 | JTAG_TCK low to JTAG_TDO data valid | — | 44 | ns |
| SJ11 | JTAG_TCK low to JTAG_TDO high impedance | — | 44 | ns |
| SJ12 | JTAG_TRST_B assert time | 100 | — | ns |
| SJ13 | JTAG_TRST_B set-up time to JTAG_TCK low | 40 | — | ns |

1 $T_{DC}$ = target frequency of SJC
2 $V_M$ = mid-point voltage

## 4.11.19 SPDIF Timing Parameters

The Sony/Philips Digital Interconnect Format (SPDIF) data is sent using the bi-phase marking code. When encoding, the SPDIF data signal is modulated by a clock that is twice the bit rate of the data signal.

Table 84 and Figure 94 and Figure 95 show SPDIF timing parameters for the Sony/Philips Digital Interconnect Format (SPDIF), including the timing of the modulating Rx clock (SPDIF_SR_CLK) for SPDIF in Rx mode and the timing of the modulating Tx clock (SPDIF_ST_CLK) for SPDIF in Tx mode.

**Table 84. SPDIF Timing Parameters**

| Parameter | Symbol | Timing Parameter Range | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| SPDIF_IN Skew: asynchronous inputs, no specs apply | — | — | 0.7 | ns |
| SPDIF_OUT output (Load = 50pf)<br>• Skew<br>• Transition rising<br>• Transition falling | <br>—<br>—<br>— | <br>—<br>—<br>— | <br>1.5<br>24.2<br>31.3 | ns |
| SPDIF_OUT output (Load = 30pf)<br>• Skew<br>• Transition rising<br>• Transition falling | <br>—<br>—<br>— | <br>—<br>—<br>— | <br>1.5<br>13.6<br>18.0 | ns |
| Modulating Rx clock (SPDIF_SR_CLK) period | srckp | 40.0 | — | ns |
| SPDIF_SR_CLK high period | srckph | 16.0 | — | ns |
| SPDIF_SR_CLK low period | srckpl | 16.0 | — | ns |
| Modulating Tx clock (SPDIF_ST_CLK) period | stclkp | 40.0 | — | ns |
| SPDIF_ST_CLK high period | stclkph | 16.0 | — | ns |
| SPDIF_ST_CLK low period | stclkpl | 16.0 | — | ns |

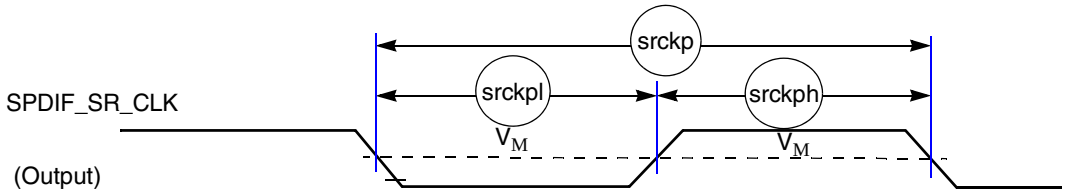


**Figure 94. SPDIF_SR_CLK Timing Diagram**

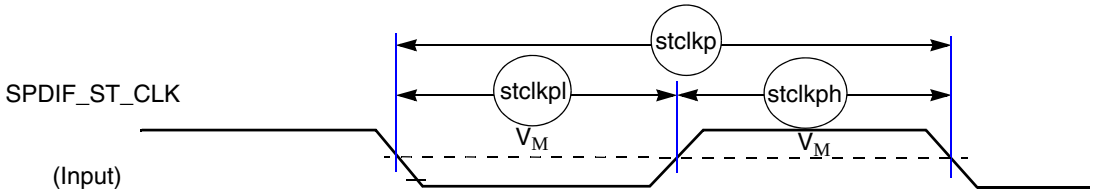


**Figure 95. SPDIF_ST_CLK Timing Diagram**

**Table 87. SSI Receiver Timing with Internal Clock (continued)**

| ID | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| **Oversampling Clock Operation** | | | | |
| SS47 | Oversampling clock period | 15.04 | — | ns |
| SS48 | Oversampling clock high period | 6.0 | — | ns |
| SS49 | Oversampling clock rise time | — | 3.0 | ns |
| SS50 | Oversampling clock low period | 6.0 | — | ns |
| SS51 | Oversampling clock fall time | — | 3.0 | ns |

**NOTE**

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal AUDx_TXC/AUDx_RXC and/or the frame sync AUDx_TXFS/AUDx_RXFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- AUDx_TXC and AUDx_RXC refer to the Transmit and Receive sections of the SSI.
- The terms, WL and BL, refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the frame sync timing is same as that of transmit data (for example, during AC97 mode of operation).

### 4.11.20.3 SSI Transmitter Timing with External Clock

Figure 98 depicts the SSI transmitter external clock timing and Table 88 lists the timing parameters for the transmitter timing with the external clock.

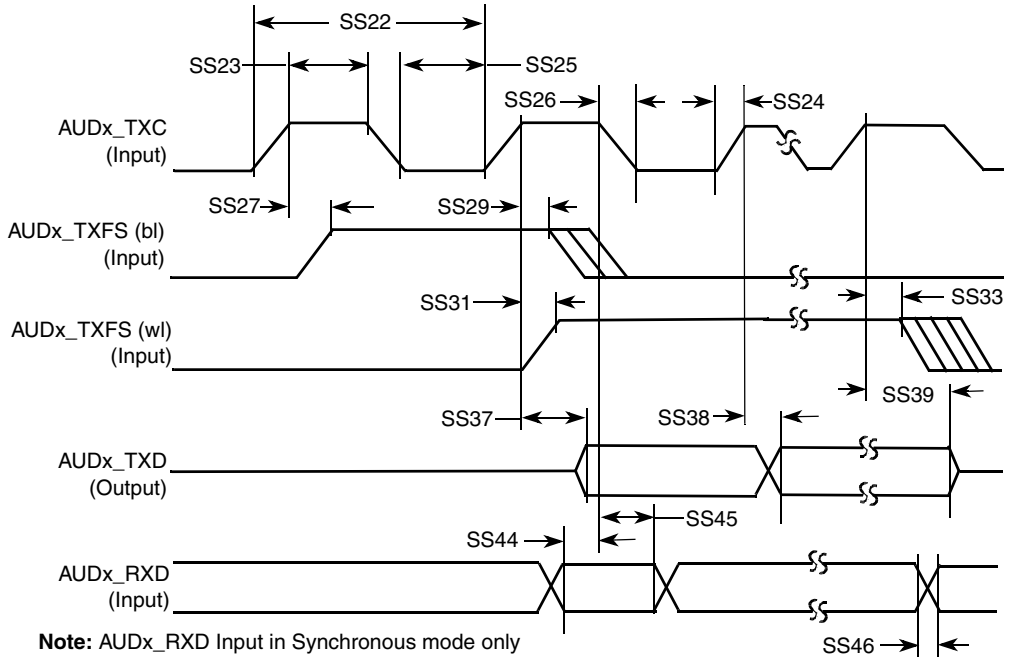


**Figure 98. SSI Transmitter External Clock Timing Diagram**

**Table 88. SSI Transmitter Timing with External Clock**

| ID | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| **External Clock Operation** | | | | |
| SS22 | AUDx_TXC/AUDx_RXC clock period | 81.4 | — | ns |
| SS23 | AUDx_TXC/AUDx_RXC clock high period | 36.0 | — | ns |
| SS24 | AUDx_TXC/AUDx_RXC clock rise time | — | 6.0 | ns |
| SS25 | AUDx_TXC/AUDx_RXC clock low period | 36.0 | — | ns |
| SS26 | AUDx_TXC/AUDx_RXC clock fall time | — | 6.0 | ns |
| SS27 | AUDx_TXC high to AUDx_TXFS (bl) high | –10.0 | 15.0 | ns |
| SS29 | AUDx_TXC high to AUDx_TXFS (bl) low | 10.0 | — | ns |
| SS31 | AUDx_TXC high to AUDx_TXFS (wl) high | –10.0 | 15.0 | ns |
| SS33 | AUDx_TXC high to AUDx_TXFS (wl) low | 10.0 | — | ns |
| SS37 | AUDx_TXC high to AUDx_TXD valid from high impedance | — | 15.0 | ns |
| SS38 | AUDx_TXC high to AUDx_TXD high/low | — | 15.0 | ns |
| SS39 | AUDx_TXC high to AUDx_TXD high impedance | — | 15.0 | ns |

**Table 98. Interfaces Allocation During Boot (continued)**

| Interface | IP Instance | Allocated Pads During Boot | Comment |
|---|---|---|---|
| NAND Flash | GPMI | NANDF_CLE, NANDF_ALE, NANDF_WP_B, SD4_CMD, SD4_CLK, NANDF_RB0, SD4_DAT0, NANDF_CS0, NANDF_CS1, NANDF_CS2, NANDF_CS3, NANDF_D[7:0] | 8 bit<br>Only CS0 is supported |
| SD/MMC | USDHC-1 | SD1_CLK, SD1_CMD,SD1_DAT0, SD1_DAT1, SD1_DAT2, SD1_DAT3, NANDF_D0, NANDF_D1, NANDF_D2, NANDF_D3, KEY_COL1 | 1, 4, or 8 bit |
| SD/MMC | USDHC-2 | SD2_CLK, SD2_CMD, SD2_DAT0, SD2_DAT1, SD2_DAT2, SD2_DAT3, NANDF_D4, NANDF_D5, NANDF_D6, NANDF_D7, KEY_ROW1 | 1, 4, or 8 bit |
| SD/MMC | USDHC-3 | SD3_CLK, SD3_CMD, SD3_DAT0, SD3_DAT1, SD3_DAT2, SD3_DAT3, SD3_DAT4, SD3_DAT5, SD3_DAT6, SD3_DAT7, GPIO_18 | 1, 4, or 8 bit |
| SD/MMC | USDHC-4 | SD4_CLK, SD4_CMD, SD4_DAT0, SD4_DAT1, SD4_DAT2, SD4_DAT3, SD4_DAT4, SD4_DAT5, SD4_DAT6, SD4_DAT7, NANDF_CS1 | 1, 4, or 8 bit |
| I2C | I2C-1 | EIM_D28, EIM_D21 | — |
| I2C | I2C-2 | EIM_D16, EIM_EB2 | — |
| I2C | I2C-3 | EIM_D18, EIM_D17 | — |
| SATA | SATA_PHY | SATA_TXM, SATA_TXP, SATA_RXP, SATA_RXM, SATA_REXT | — |
| USB | USB-OTG PHY | USB_OTG_DP<br>USB_OTG_DN<br>USB_OTG_VBUS | — |

### 6.2.2 21 x 21 mm Ground, Power, Sense, and Reference Contact Assignments

Table 99 shows the device connection list for ground, power, sense, and reference contact signals.

**Table 99. 21 x 21 mm Supplies Contact Assignment**

| Supply Rail Name | Ball(s) Position(s) | Remark |
|---|---|---|
| CSI_REXT | D4 | — |
| DRAM_VREF | AC2 | — |
| DSI_REXT | G4 | — |
| FA_ANA | A5 | — |
| GND | A13, A25, A4, A8, AA10, AA13, AA16, AA19, AA22, AD4, D3, F8, J15, L10, M15, P15, T15, U8, W17, AA7, AD7, D6, G10, J18, L12, M18, P18, T17, V19, W18, AB24, AE1, D8, G19, J2, L15, M8, P8, T19, V8, W19, AB3, AE25, E5, G3, J8, L18, N10, R12, T8, W10, W3, AD10, B4, E6, H12, K10, L2, N15, R15, U11, W11, W7, AD13, C1, E7, H15, K12, L5, N18, R17, U12, W12, W8, AD16, C10, F5, H18, K15, L8, N8, R8, U15, W13, W9, AD19, C4, F6, H8, K18, M10, P10, T11, U17, W15, Y24, AD22, C6, F7, J12, K8, M12, P12, T12, U19, W16, Y5 | — |
| GPANAIO | C8 | — |
| HDMI_DDCCEC | K2 | Analog ground reference for the Hot Plug detect signal |
| HDMI_REF | J1 | — |
| HDMI_VP | L7 | — |
| HDMI_VPH | M7 | — |
| NVCC_CSI | N7 | Supply of the camera sensor interface |
| NVCC_DRAM | R18, T18, U18, V10, V11, V12, V13, V14, V15, V16, V17, V18, V9 | Supply of the DDR interface |
| NVCC_EIM0 | K19 | Supply of the EIM interface |
| NVCC_EIM1 | L19 | Supply of the EIM interface |
| NVCC_EIM2 | M19 | Supply of the EIM interface |
| NVCC_ENET | R19 | Supply of the ENET interface |
| NVCC_GPIO | P7 | Supply of the GPIO interface |
| NVCC_JTAG | J7 | Supply of the JTAG tap controller interface |
| NVCC_LCD | P19 | Supply of the LCD interface |
| NVCC_LVDS2P5 | V7 | Supply of the LVDS display interface and DDR pre-drivers. Even if the LVDS interface is not used, this supply must remain powered. |
| NVCC_MIPI | K7 | Supply of the MIPI interface |

**Table 100. 21 x 21 mm Functional Contact Assignments (continued)**

| Ball Name | Ball | Power Group | Ball Type | Out of Reset Condition[1] | | | |
|---|---|---|---|---|---|---|---|
| | | | | Default Mode (Reset Mode) | Default Function (Signal Name) | Input/Output | Value[2] |
| GPIO_8 | R5 | NVCC_GPIO | GPIO | ALT5 | GPIO1_IO08 | Input | PU (100K) |
| GPIO_9 | T2 | NVCC_GPIO | GPIO | ALT5 | GPIO1_IO09 | Input | PU (100K) |
| HDMI_CLKM | J5 | HDMI_VPH | — | — | HDMI_TX_CLK_N | — | — |
| HDMI_CLKP | J6 | HDMI_VPH | — | — | HDMI_TX_CLK_P | — | — |
| HDMI_D0M | K5 | HDMI_VPH | — | — | HDMI_TX_DATA0_N | — | — |
| HDMI_D0P | K6 | HDMI_VPH | — | — | HDMI_TX_DATA0_P | — | — |
| HDMI_D1M | J3 | HDMI_VPH | — | — | HDMI_TX_DATA1_N | — | — |
| HDMI_D1P | J4 | HDMI_VPH | — | — | HDMI_TX_DATA1_P | — | — |
| HDMI_D2M | K3 | HDMI_VPH | — | — | HDMI_TX_DATA2_N | — | — |
| HDMI_D2P | K4 | HDMI_VPH | — | — | HDMI_TX_DATA2_P | — | — |
| HDMI_HPD | K1 | HDMI_VPH | — | — | HDMI_TX_HPD | — | — |
| JTAG_MOD | H6 | NVCC_JTAG | GPIO | ALT0 | JTAG_MODE | Input | PU (100K) |
| JTAG_TCK | H5 | NVCC_JTAG | GPIO | ALT0 | JTAG_TCK | Input | PU (47K) |
| JTAG_TDI | G5 | NVCC_JTAG | GPIO | ALT0 | JTAG_TDI | Input | PU (47K) |
| JTAG_TDO | G6 | NVCC_JTAG | GPIO | ALT0 | JTAG_TDO | Output | Keeper |
| JTAG_TMS | C3 | NVCC_JTAG | GPIO | ALT0 | JTAG_TMS | Input | PU (47K) |
| JTAG_TRSTB | C2 | NVCC_JTAG | GPIO | ALT0 | JTAG_TRST_B | Input | PU (47K) |
| KEY_COL0 | W5 | NVCC_GPIO | GPIO | ALT5 | GPIO4_IO06 | Input | PU (100K) |
| KEY_COL1 | U7 | NVCC_GPIO | GPIO | ALT5 | GPIO4_IO08 | Input | PU (100K) |
| KEY_COL2 | W6 | NVCC_GPIO | GPIO | ALT5 | GPIO4_IO10 | Input | PU (100K) |
| KEY_COL3 | U5 | NVCC_GPIO | GPIO | ALT5 | GPIO4_IO12 | Input | PU (100K) |
| KEY_COL4 | T6 | NVCC_GPIO | GPIO | ALT5 | GPIO4_IO14 | Input | PU (100K) |
| KEY_ROW0 | V6 | NVCC_GPIO | GPIO | ALT5 | GPIO4_IO07 | Input | PU (100K) |
| KEY_ROW1 | U6 | NVCC_GPIO | GPIO | ALT5 | GPIO4_IO09 | Input | PU (100K) |
| KEY_ROW2 | W4 | NVCC_GPIO | GPIO | ALT5 | GPIO4_IO11 | Input | PU (100K) |
| KEY_ROW3 | T7 | NVCC_GPIO | GPIO | ALT5 | GPIO4_IO13 | Input | PU (100K) |
| KEY_ROW4 | V5 | NVCC_GPIO | GPIO | ALT5 | GPIO4_IO15 | Input | PD (100K) |
| LVDS0_CLK_N | V4 | NVCC_LVDS_2P5 | LVDS | — | LVDS0_CLK_N | — | — |
| LVDS0_CLK_P | V3 | NVCC_LVDS_2P5 | LVDS | ALT0 | LVDS0_CLK_P | Input | Keeper |
| LVDS0_TX0_N | U2 | NVCC_LVDS_2P5 | LVDS | — | LVDS0_TX0_N | — | — |
| LVDS0_TX0_P | U1 | NVCC_LVDS_2P5 | LVDS | ALT0 | LVDS0_TX0_P | Input | Keeper |
| LVDS0_TX1_N | U4 | NVCC_LVDS_2P5 | LVDS | — | LVDS0_TX1_N | — | — |
| LVDS0_TX1_P | U3 | NVCC_LVDS_2P5 | LVDS | ALT0 | LVDS0_TX1_P | Input | Keeper |
| LVDS0_TX2_N | V2 | NVCC_LVDS_2P5 | LVDS | — | LVDS0_TX2_N | — | — |
| LVDS0_TX2_P | V1 | NVCC_LVDS_2P5 | LVDS | ALT0 | LVDS0_TX2_P | Input | Keeper |
| LVDS0_TX3_N | W2 | NVCC_LVDS_2P5 | LVDS | — | LVDS0_TX3_N | — | — |