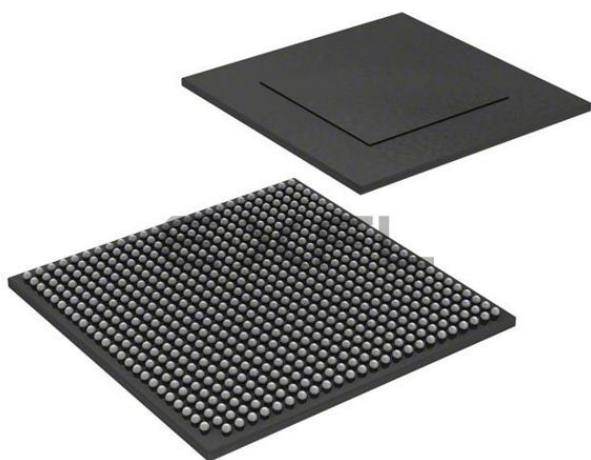




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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Active
Core Processor	ARM® Cortex® -A9
Number of Cores/Bus Width	4 Core, 32-Bit
Speed	852MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (1)
SATA	SATA 3Gbps (1)
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-40°C ~ 125°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	624-FBGA, FCBGA
Supplier Device Package	624-FCBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6q6avt08ad

1.1 Ordering Information

Table 1 shows examples of orderable part numbers covered by this data sheet. This table does not include all possible orderable part numbers. The latest part numbers are available on freescale.com/imx6series. If your desired part number is not listed in the table, or you have questions about available parts, see freescale.com/imx6series or contact your Freescale representative.

Table 1. Example Orderable Part Numbers

Part Number	Quad/Dual CPU	Options	Speed ¹ Grade	Temperature Grade	Package
MCIMX6Q6AVT10AC	i.MX 6Quad	With VPU, GPU	1 GHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6Q6AVT10AD	i.MX 6Quad	With VPU, GPU	1 GHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6Q4AVT10AC	i.MX 6Quad	With GPU, no VPU	1 GHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6Q4AVT10AD	i.MX 6Quad	With GPU, no VPU	1 GHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6Q6AVT08AC	i.MX 6Quad	With VPU, GPU	852 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6Q6AVT08AD	i.MX 6Quad	With VPU, GPU	852 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6Q4AVT08AC	i.MX 6Quad	With GPU, no VPU	852 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6Q4AVT08AD	i.MX 6Quad	With GPU, no VPU	852 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6D6AVT10AC	i.MX 6Dual	With VPU, GPU	1 GHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6D6AVT10AD	i.MX 6Dual	With VPU, GPU	1 GHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6D4AVT10AC	i.MX 6Dual	With GPU, no VPU	1 GHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6D4AVT10AD	i.MX 6Dual	With GPU, no VPU	1 GHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6D6AVT08AC	i.MX 6Dual	With VPU, GPU	852 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6D6AVT08AD	i.MX 6Dual	With VPU, GPU	852 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6D4AVT08AC	i.MX 6Dual	With GPU, no VPU	852 MHz	Automotive ¹	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6D4AVT08AD	i.MX 6Dual	With GPU, no VPU	852 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)

¹ If a 24 MHz input clock is used (required for USB), the maximum SoC speed is limited to 996 MHz.

Introduction

- Displays—Total five interfaces available. Total raw pixel rate of all interfaces is up to 450 Mpixels/sec, 24 bpp. Up to four interfaces may be active in parallel.
 - One Parallel 24-bit display port, up to 225 Mpixels/sec (for example, WUXGA at 60 Hz or dual HD1080 and WXGA at 60 Hz)
 - LVDS serial ports—One port up to 165 Mpixels/sec or two ports up to 85 MP/sec (for example, WUXGA at 60 Hz) each
 - HDMI 1.4 port
 - MIPI/DSI, two lanes at 1 Gbps
- Camera sensors:
 - Parallel Camera port (up to 20 bit and up to 240 MHz peak)
 - MIPI CSI-2 serial camera port, supporting up to 1000 Mbps/lane in 1/2/3-lane mode and up to 800 Mbps/lane in 4-lane mode. The CSI-2 Receiver core can manage one clock lane and up to four data lanes. Each i.MX 6Dual/6Quad processor has four lanes.
- Expansion cards:
 - Four MMC/SD/SDIO card ports all supporting:
 - 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR-104 mode (104 MB/s max)
 - 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max)
- USB:
 - One High Speed (HS) USB 2.0 OTG (Up to 480 Mbps), with integrated HS USB PHY
 - Three USB 2.0 (480 Mbps) hosts:
 - One HS host with integrated High Speed PHY
 - Two HS hosts with integrated HS-IC USB (High Speed Inter-Chip USB) PHY
- Expansion PCI Express port (PCIe) v2.0 one lane
 - PCI Express (Gen 2.0) dual mode complex, supporting Root complex operations and Endpoint operations. Uses x1 PHY configuration.
- Miscellaneous IPs and interfaces:
 - SSI block capable of supporting audio sample frequencies up to 192 kHz stereo inputs and outputs with I²S mode
 - ESAI is capable of supporting audio sample frequencies up to 260kHz in I2S mode with 7.1 multi channel outputs
 - Five UARTs, up to 5.0 Mbps each:
 - Providing RS232 interface
 - Supporting 9-bit RS485 multidrop mode
 - One of the five UARTs (UART1) supports 8-wire while others four supports 4-wire. This is due to the SoC IOMUX limitation, since all UART IPs are identical.
 - Five eCSPI (Enhanced CSPI)
 - Three I2C, supporting 400 kbps

4.1.9 PCIe 2.0 Maximum Power Consumption

Table 12 provides PCIe PHY currents for certain operating modes.

Table 12. PCIe PHY Current Drain

Mode	Test Conditions	Supply	Max Current	Unit
P0: Normal Operation	5G Operations	PCIE_VP (1.1 V)	40	mA
		PCIE_VPTX (1.1 V)	20	
		PCIE_VPH (2.5 V)	21	
	2.5G Operations	PCIE_VP (1.1 V)	27	
		PCIE_VPTX (1.1 V)	20	
		PCIE_VPH (2.5 V)	20	
P0s: Low Recovery Time Latency, Power Saving State	5G Operations	PCIE_VP (1.1 V)	30	mA
		PCIE_VPTX (1.1 V)	2.4	
		PCIE_VPH (2.5 V)	18	
	2.5G Operations	PCIE_VP (1.1 V)	20	
		PCIE_VPTX (1.1 V)	2.4	
		PCIE_VPH (2.5 V)	18	
P1: Longer Recovery Time Latency, Lower Power State	—	PCIE_VP (1.1 V)	12	mA
		PCIE_VPTX (1.1 V)	2.4	
		PCIE_VPH (2.5 V)	12	
Power Down	—	PCIE_VP (1.1 V)	1.3	mA
		PCIE_VPTX (1.1 V)	0.18	
		PCIE_VPH (2.5 V)	0.36	

4.9.3 External Interface Module (EIM)

The following subsections provide information on the EIM. Maximum operating frequency for EIM data transfer is 104 MHz. Timing parameters in this section that are given as a function of register settings or clock periods are valid for the entire range of allowed frequencies (0–104 MHz).

4.9.3.1 EIM Interface Pads Allocation

EIM supports 32-bit, 16-bit and 8-bit devices operating in address/data separate or multiplexed modes. [Table 39](#) provides EIM interface pads allocation in different modes.

Table 39. EIM Internal Module Multiplexing¹

Setup	Non Multiplexed Address/Data Mode							Multiplexed Address/Data mode	
	8 Bit				16 Bit		32 Bit	16 Bit	32 Bit
	MUM = 0, DSZ = 100	MUM = 0, DSZ = 101	MUM = 0, DSZ = 110	MUM = 0, DSZ = 111	MUM = 0, DSZ = 001	MUM = 0, DSZ = 010	MUM = 0, DSZ = 011	MUM = 1, DSZ = 001	MUM = 1, DSZ = 011
EIM_ADDR [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]
EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_DATA [09:00]
EIM_DATA [07:00], EIM_EB0_B	EIM_DATA [07:00]	—	—	—	EIM_DATA [07:00]	—	EIM_DATA [07:00]	EIM_AD [07:00]	EIM_AD [07:00]
EIM_DATA [15:08], EIM_EB1_B	—	EIM_DATA [15:08]	—	—	EIM_DATA [15:08]	—	EIM_DATA [15:08]	EIM_AD [15:08]	EIM_AD [15:08]
EIM_DATA [23:16], EIM_EB2_B	—	—	EIM_DATA [23:16]	—	—	EIM_DATA [23:16]	EIM_DATA [23:16]	—	EIM_DATA [07:00]
EIM_DATA [31:24], EIM_EB3_B	—	—	—	EIM_DATA [31:24]	—	EIM_DATA [31:24]	EIM_DATA [31:24]	—	EIM_DATA [15:08]

¹ For more information on configuration ports mentioned in this table, see the i.MX 6Dual/6Quad reference manual (IMX6DQRM).

Table 42. DDR3/DDR3L Timing Parameter (continued)

ID	Parameter ^{1,2}	Symbol	CK = 532 MHz		Unit
			Min	Max	
DDR4	DRAM_CSx_B, DRAM_RAS_B, DRAM_CAS_B, DRAM_SDCKEx, DRAM_SDWE_B, DRAM_ODTx setup time	t _{IS}	500	—	ps
DDR5	DRAM_CSx_B, DRAM_RAS_B, DRAM_CAS_B, DRAM_SDCKEx, DRAM_SDWE_B, DRAM_ODTx hold time	t _{IH}	400	—	ps
DDR6	Address output setup time	t _{IS}	500	—	ps
DDR7	Address output hold time	t _{IH}	400	—	ps

¹ All measurements are in reference to V_{ref} level.

² Measurements were done using balanced load and 25 Ω resistor from outputs to DRAM_VREF.

Figure 25 shows the DDR3/DDR3L write timing diagram. The timing parameters for this diagram appear in Table 43.

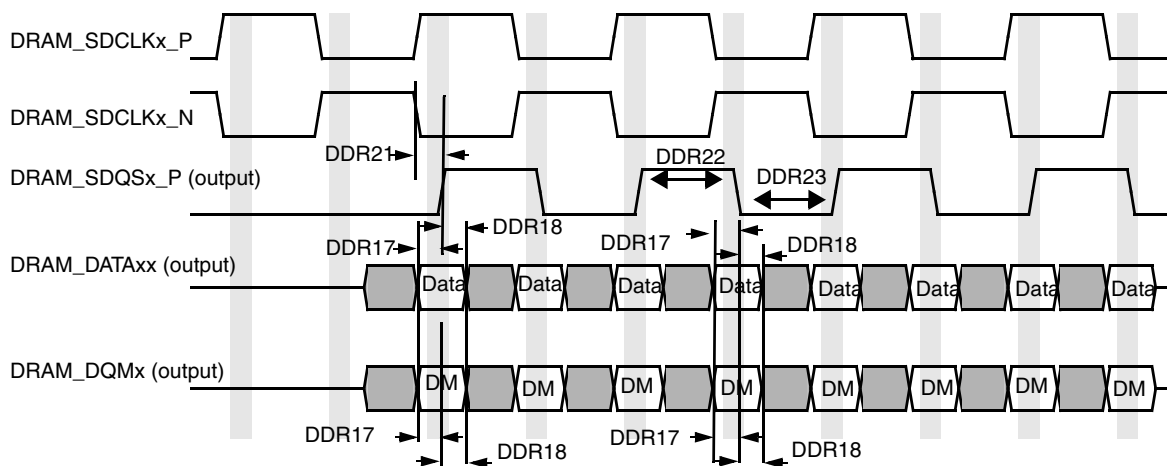


Figure 25. DDR3/DDR3L Write Cycle

Table 43. DDR3/DDR3L Write Cycle

ID	Parameter ^{1,2,3}	Symbol	CK = 532 MHz		Unit
			Min	Max	
DDR17	DRAM_DATAxx and DRAM_DQMx setup time to DRAM_SDQSx_P (differential strobe)	t _{DS}	125 ⁴	—	ps
DDR18	DRAM_DATAxx and DRAM_DQMx hold time to DRAM_SDQSx_P (differential strobe)	t _{DH}	150 ⁴	—	ps
DDR21	DRAM_SDQSx_P latching rising transitions to associated clock edges	t _{DQSS}	-0.25	+0.25	tCK
DDR22	DRAM_SDQSx_P high level width	t _{DQSH}	0.45	0.55	tCK
DDR23	DRAM_SDQSx_P low level width	t _{DQSL}	0.45	0.55	tCK

¹ To receive the reported setup and hold values, write calibration should be performed to locate the DRAM_SDQSx_P in the middle of DRAM_DATAxx window.

² All measurements are in reference to V_{ref} level.

³ Measurements were taken using balanced load and 25 Ω resistor from outputs to DRAM_VREF

Table 45. LPDDR2 Timing Parameter

ID	Parameter ^{1,2}	Symbol	CK = 532 MHz		Unit
			Min	Max	
LP1	DRAM_SDCLKx_P clock high-level width	tCH	0.45	0.55	tCK
LP2	DRAM_SDCLKx_P clock low-level width	tCL	0.45	0.55	tCK
LP3	DRAM_CSx_B, DRAM_ADDRxx setup time	tIS	270	—	ps
LP4	DRAM_CSx_B, DRAM_ADDRxx hold time	tIH	270	—	ps
LP3	DRAM_ADDRxx setup time	tIS	230	—	ps
LP4	DRAM_ADDRxx hold time	tIH	230	—	ps

¹ All measurements are in reference to Vref level.

² Measurements were completed using balanced load and a 25 Ω resistor from outputs to DRAM_VREF.

Figure 28 shows the LPDDR2 write timing diagram. The timing parameters for this diagram appear in Table 46.

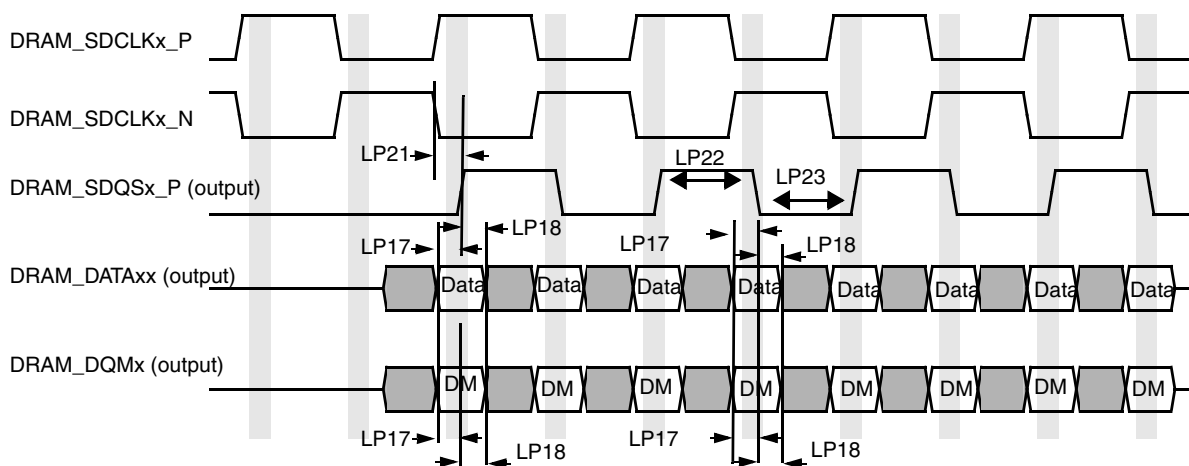


Figure 28. LPDDR2 Write Cycle

Table 46. LPDDR2 Write Cycle

ID	Parameter ^{1,2,3}	Symbol	CK = 532 MHz		Unit
			Min	Max	
LP17	DRAM_DATAxx and DRAM_DQMx setup time to DRAM_SDQSx_P (differential strobe)	tds	235	—	ps
LP18	DRAM_DATAxx and DRAM_DQMx hold time to DRAM_SDQSx_P (differential strobe)	tdH	235	—	ps
LP21	DRAM_SDQSx_P latching rising transitions to associated clock edges	tdQSS	0.75	1.25	tCK
LP22	DRAM_SDQSx_P high level width	tdQSH	0.4	—	tCK
LP23	DRAM_SDQSx_P low level width	tdQSL	0.4	—	tCK

Table 48. Asynchronous Mode Timing Parameters¹ (continued)

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min	Max	
NF16	Data setup on read	tDSR	—	$(DS \times T - 0.67)/18.38$ [see ^{5,6}]	ns
NF17	Data hold on read	tDHR	0.82/11.83 [see ^{5,6}]	—	ns

¹ The GPMI asynchronous mode output timing can be controlled by the module's internal registers HW_GPMI_TIMING0_ADDRESS_SETUP, HW_GPMI_TIMING0_DATA_SETUP, and HW_GPMI_TIMING0_DATA_HOLD. This AC timing depends on these registers settings. In the table, AS/DS/DH represents each of these settings.

² AS minimum value can be 0, while DS/DH minimum value is 1.

³ T = GPMI clock period -0.075ns (half of maximum p-p jitter).

⁴ NF12 is met automatically by the design.

⁵ Non-EDO mode.

⁶ EDO mode, GPMI clock $\approx$ 100 MHz
(AS=DS=DH=1, GPMI_CTL1 [RDN_DELAY] = 8, GPMI_CTL1 [HALF_PERIOD] = 0).

In EDO mode (Figure 34), NF16/NF17 are different from the definition in non-EDO mode (Figure 33). They are called tREA/tRHOH (NAND_RE_B access time/NAND_RE_B HIGH to output hold). The typical value for them are 16 ns (max for tREA)/15 ns (min for tRHOH) at 50 MB/s EDO mode. In EDO mode, GPMI will sample NAND_DATAxx at rising edge of delayed NAND_RE_B provided by an internal DPLL. The delay value can be controlled by GPMI_CTRL1.RDN_DELAY (see the GPMI chapter of the i.MX 6Dual/6Quad reference manual (IMX6DQRM)). The typical value of this control register is 0x8 at 50 MT/s EDO mode. However, if the board delay is large enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

Electrical Characteristics

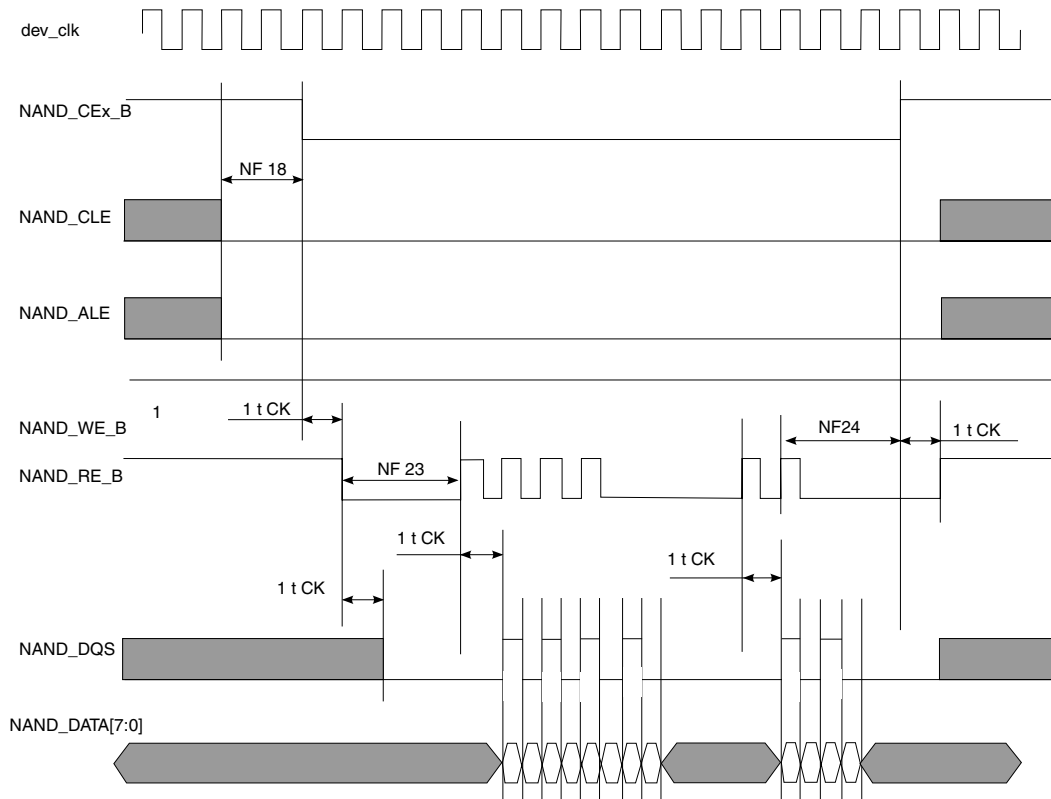


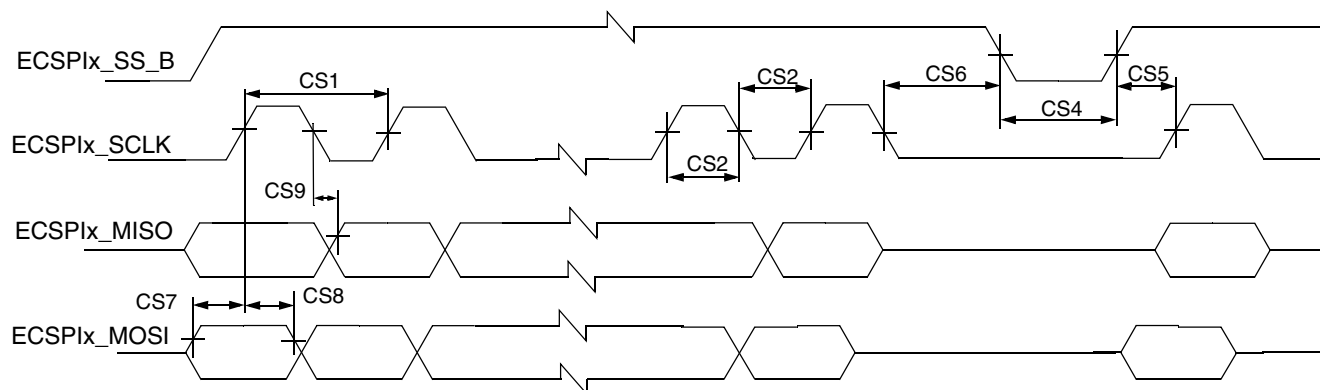
Figure 40. Samsung Toggle Mode Data Read Timing

Table 50. Samsung Toggle Mode Timing Parameters¹

ID	Parameter	Symbol	Timing T = GPML Clock Cycle		Unit
			Min	Max	
NF1	NAND_CLE setup time	tCLS	$(AS + DS) \times T - 0.12$ [see ^{2,3}]		—
NF2	NAND_CLE hold time	tCLH	$DH \times T - 0.72$ [see ²]		—
NF3	NAND_CEx_B setup time	tCS	$(AS + DS) \times T - 0.58$ [see ^{3,2}]		—
NF4	NAND_CEx_B hold time	tCH	$DH \times T - 1$ [see ²]		—
NF5	NAND_WE_B pulse width	tWP	$DS \times T$ [see ²]		—
NF6	NAND_ALE setup time	tALS	$(AS + DS) \times T - 0.49$ [see ^{3,2}]		—
NF7	NAND_ALE hold time	tALH	$DH \times T - 0.42$ [see ²]		—
NF8	Command/address NAND_DATAxx setup time	tCAS	$DS \times T - 0.26$ [see ²]		—
NF9	Command/address NAND_DATAxx hold time	tCAH	$DH \times T - 1.37$ [see ²]		—
NF18	NAND_CEx_B access time	tCE	$CE_DELAY \times T$ [see ^{4,2}]	—	ns
NF22	clock period	tCK	—	—	ns
NF23	preamble delay	tPRE	$PRE_DELAY \times T$ [see ^{5,2}]	—	ns
NF24	postamble delay	tPOST	$POST_DELAY \times T + 0.43$ [see ²]	—	ns

4.11.2.2 ECSPi Slave Mode Timing

Figure 42 depicts the timing of ECSPi in slave mode and Table 52 lists the ECSPi slave mode timing characteristics.



Note: ECSPi_MISO is always driven (not tri-stated) between actual data transmissions. This limits the ECSPi to be connected between a single master and a single slave.

Figure 42. ECSPi Slave Mode Timing Diagram

Table 52. ECSPi Slave Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	ECSPi_SCLK Cycle Time–Read • Slow group ¹ • Fast group ² ECSPi_SCLK Cycle Time–Write	t_{clk}	55 40 15	—	ns
CS2	ECSPi_SCLK High or Low Time–Read • Slow group ¹ • Fast group ² ECSPi_SCLK High or Low Time–Write	t_{sw}	26 20 7	—	ns
CS4	ECSPi_SSx pulse width	t_{CSLH}	Half ECSPi_SCLK period	—	ns
CS5	ECSPi_SSx Lead Time (CS setup time)	t_{SCS}	5	—	ns
CS6	ECSPi_SSx Lag Time (CS hold time)	t_{HCS}	5	—	ns
CS7	ECSPi_MOSI Setup Time	t_{Smosi}	4	—	ns
CS8	ECSPi_MOSI Hold Time	t_{Hmosi}	4	—	ns
CS9	ECSPi_MISO Propagation Delay ($C_{LOAD} = 20$ pF) • Slow group ¹ • Fast group ²	t_{PDmiso}	4	25 17	ns

¹ ECSPi slow includes:

ECSPi1/DISP0_DAT22, ECSPi1/KEY_COL1, ECSPi1/CSI0_DAT6, ECSPi2/EIM_OE, ECSPi2/DISP0_DAT17, ECSPi2/CSI0_DAT10, ECSPi3/DISP0_DAT2

² ECSPi fast includes:

ECSPi1/EIM_D17, ECSPi4/EIM_D22, ECSPi5/SD2_DAT0, ECSPi5/SD1_DAT0

4.11.4 Ultra High Speed SD/SDIO/MMC Host Interface (uSDHC) AC Timing

This section describes the electrical information of the uSDHC, which includes SD/eMMC4.3 (Single Data Rate) timing and eMMC4.4/4.1 (Dual Data Rate) timing.

4.11.4.1 SD/eMMC4.3 (Single Data Rate) AC Timing

Figure 45 depicts the timing of SD/eMMC4.3, and Table 54 lists the SD/eMMC4.3 timing characteristics.

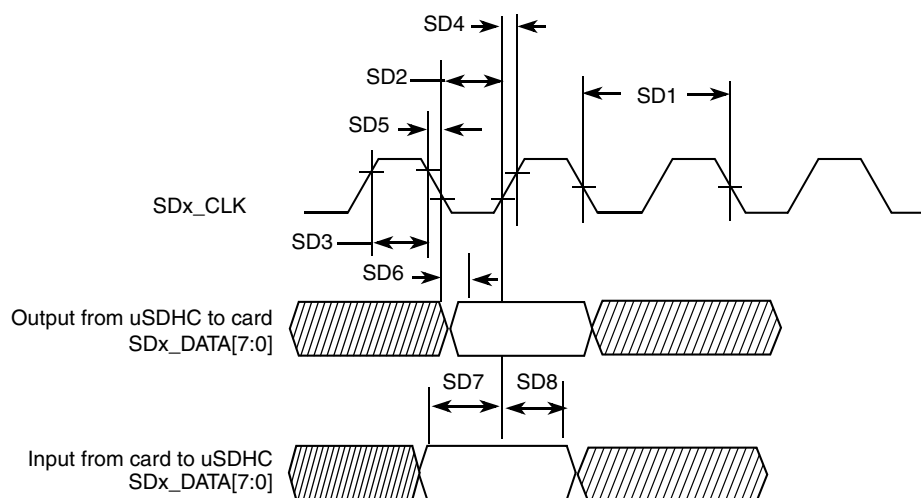


Figure 45. SD/eMMC4.3 Timing

Table 54. SD/eMMC4.3 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (Low Speed)	f_{PP}^1	0	400	kHz
	Clock Frequency (SD/SDIO Full Speed/High Speed)	f_{PP}^2	0	25/50	MHz
	Clock Frequency (MMC Full Speed/High Speed)	f_{PP}^3	0	20/52	MHz
	Clock Frequency (Identification Mode)	f_{OD}	100	400	kHz
SD2	Clock Low Time	t_{WL}	7	—	ns
SD3	Clock High Time	t_{WH}	7	—	ns
SD4	Clock Rise Time	t_{TLH}	—	3	ns
SD5	Clock Fall Time	t_{THL}	—	3	ns
eSDHC Output/Card Inputs SD_CMD, SD_DATAx (Reference to SDx_CLK)					
SD6	eSDHC Output Delay	t_{OD}	-6.6	3.6	ns

Power-up time for the HDMI 3D Tx PHY while operating with the fastest input reference clock supported (340 MHz) is 133 μ s.

4.11.7.2 Electrical Characteristics

The table below provides electrical characteristics for the HDMI 3D Tx PHY. The following three figures illustrate various definitions and measurement conditions specified in the table below.

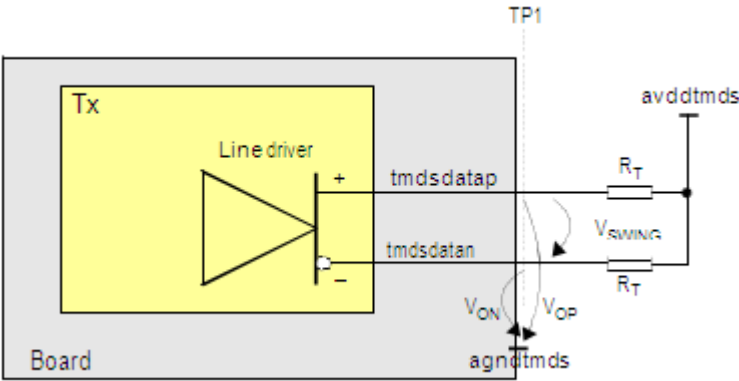


Figure 56. Driver Measuring Conditions

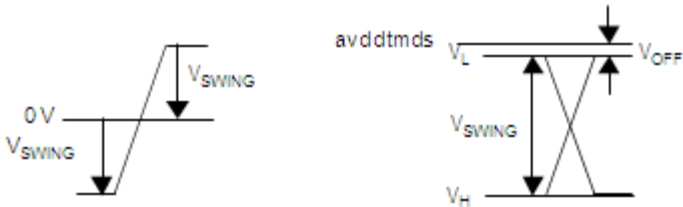


Figure 57. Driver Definitions

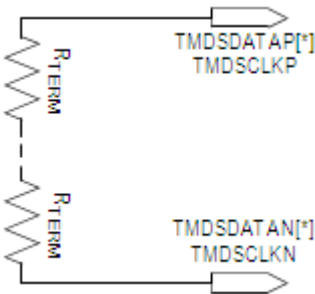


Figure 58. Source Termination

Table 63. Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Operating conditions for HDMI						
avddtmds	Termination supply voltage	—	3.15	3.3	3.45	V

³ Display interface clock up time where CEIL(X) rounds the elements of X to the nearest integers towards infinity.

$$T_{dicu} = \frac{1}{2} \left(T_{diclk} \times \text{ceil} \left[\frac{2 \times \text{DISP_CLK_UP}}{\text{DI_CLK_PERIOD}} \right] \right)$$

4.11.11 LVDS Display Bridge (LDB) Module Parameters

The LVDS interface complies with TIA/EIA 644-A standard. For more details, see TIA/EIA STANDARD 644-A, “Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits.”

Table 71. LVDS Display Bridge (LDB) Electrical Specification

Parameter	Symbol	Test Condition	Min	Max	Units
Differential Voltage Output Voltage	V _{OD}	100 Ω Differential load	250	450	mV
Output Voltage High	V _{oh}	100 Ω differential load (0 V Diff—Output High Voltage static)	1.25	1.6	V
Output Voltage Low	V _{ol}	100 Ω differential load (0 V Diff—Output Low Voltage static)	0.9	1.25	V
Offset Static Voltage	V _{OS}	Two 49.9 Ω resistors in series between N-P terminal, with output in either Zero or One state, the voltage measured between the 2 resistors.	1.15	1.375	V
VOS Differential	V _{OSDIFF}	Difference in V _{OS} between a One and a Zero state	-50	50	mV
Output short-circuited to GND	ISA ISB	With the output common shorted to GND	-24	24	mA
VT Full Load Test	VTLoad	100 Ω Differential load with a 3.74 kΩ load between GND and I/O supply voltage	247	454	mV

4.11.12 MIPI D-PHY Timing Parameters

This section describes MIPI D-PHY electrical specifications, compliant with MIPI CSI-2 version 1.0, D-PHY specification Rev. 1.0 (for MIPI sensor port x4 lanes) and MIPI DSI Version 1.01, and D-PHY specification Rev. 1.0 (and also DPI version 2.0, DBI version 2.0, DSC version 1.0a at protocol layer) (for MIPI display port x2 lanes).

4.11.12.1 Electrical and Timing Information

Table 72. Electrical and Timing Information

Symbol	Parameters	Test Conditions	Min	Typ	Max	Unit
Input DC Specifications—Apply to DSI_CLK_P/_N and DSI_DATA_P/_N Inputs						
V _I	Input signal voltage range	Transient voltage range is limited from -300 mV to 1600 mV	-50	—	1350	mV

4.11.13.3 Receiver Real-Time Data Flow

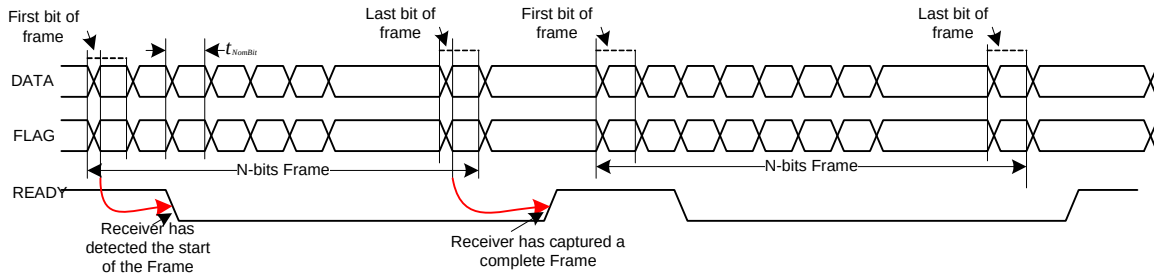


Figure 81. Receiver Real-Time Data Flow READY Signal Timing

4.11.13.4 Synchronized Data Flow Transmission with Wake

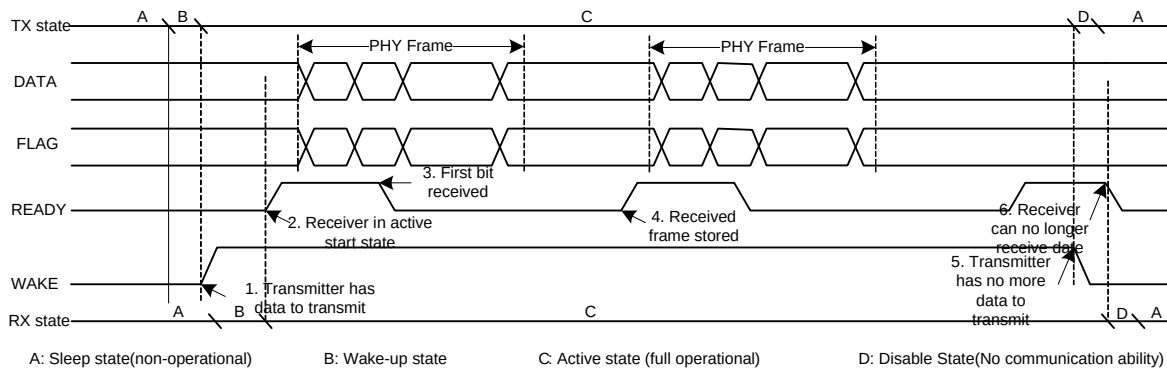


Figure 82. Synchronized Data Flow Transmission with WAKE

4.11.13.5 Stream Transmission Mode Frame Transfer

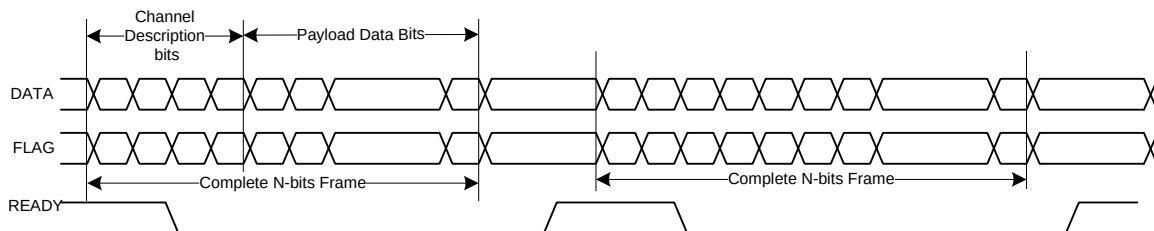


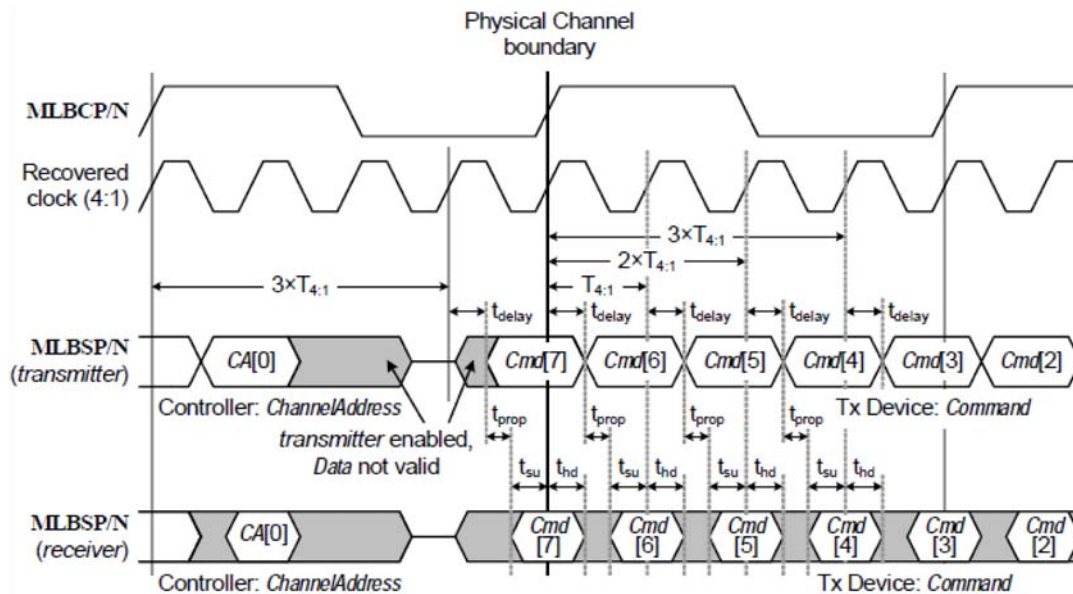
Figure 83. Stream Transmission Mode Frame Transfer (Synchronized Data Flow)

Table 79. MLB 6-Pin Interface Timing Parameters

Parameter	Symbol	Min	Max	Unit	Comment
Cycle-to-cycle system jitter	t_{jitter}	—	600	ps	—
Transmitter MLB_SIG_P/_N (MLB_DATA_P/_N) output valid from transition of MLB_CLK_P/_N (low-to-high) ¹	t_{delay}	0.6	1.3	ns	—
Disable turnaround time from transition of MLB_CLK_P/_N (low-to-high)	t_{phz}	0.6	3.5	ns	—
Enable turnaround time from transition of MLB_CLK_P/_N (low-to-high)	t_{plz}	0.6	5.6	ns	—
MLB_SIG_P/_N (MLB_DATA_P/_N) valid to transition of MLB_CLK_P/_N (low-to-high)	t_{su}	0.05	—	ns	—
MLB_SIG_P/_N (MLB_DATA_P/_N) hold from transition of MLB_CLK_P/_N (low-to-high) ²	t_{hd}	0.6	—	ns	—

¹ t_{delay} , t_{phz} , t_{plz} , t_{su} , and t_{hd} may also be referenced from a low-to-high transition of the recovered clock for 2:1 and 4:1 recovered-to-external clock ratios.

² The transmitting device must ensure valid data on MLB_SIG_P/_N (MLB_DATA_P/_N) for at least $t_{\text{hd}(\text{min})}$ following the rising edge of MLBCLKP/N; receivers must latch MLB_SIG_P/_N (MLB_DATA_P/_N) data within $t_{\text{hd}(\text{min})}$ of the rising edge of MLB_CLK_P/_N.


Figure 88. MLB 6-Pin Delay, Setup, and Hold Times

4.11.15 PCIe PHY Parameters

The PCIe interface complies with PCIe specification Gen2 x1 lane and supports the PCI Express 1.1/2.0 standard.

4.11.15.1 PCIE_REXT Reference Resistor Connection

The impedance calibration process requires connection of reference resistor 200 Ω . 1% precision resistor on PCIE_REXT pads to ground. It is used for termination impedance calibration.

4.11.16 Pulse Width Modulator (PWM) Timing Parameters

This section describes the electrical information of the PWM. The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMO) external pin.

Figure 89 depicts the timing of the PWM, and Table 80 lists the PWM timing parameters.

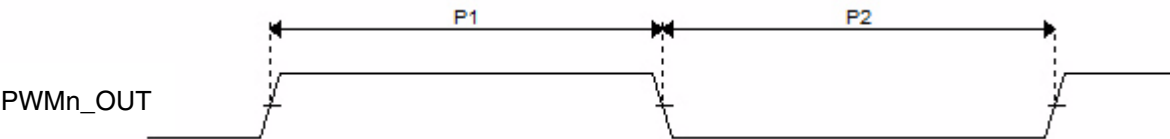


Figure 89. PWM Timing

Table 80. PWM Output Timing Parameters

ID	Parameter	Min	Max	Unit
—	PWM Module Clock Frequency	0	ipg_clk	MHz
P1	PWM output pulse width high	15	—	ns
P2	PWM output pulse width low	15	—	ns

4.11.17 SATA PHY Parameters

This section describes SATA PHY electrical specifications.

4.11.17.1 Transmitter and Receiver Characteristics

The SATA PHY meets or exceeds the electrical compliance requirements defined in the SATA specifications.

NOTE

The tables in the following sections indicate any exceptions to the SATA specification or aspects of the SATA PHY that exceed the standard, as well as provide information about parameters not defined in the standard.

The following subsections provide values obtained from a combination of simulations and silicon characterization.

Table 84. SPDIF Timing Parameters

Parameter	Symbol	Timing Parameter Range		Unit
		Min	Max	
SPDIF_IN Skew: asynchronous inputs, no specs apply	—	—	0.7	ns
SPDIF_OUT output (Load = 50pf)				
• Skew	—	—	1.5	ns
• Transition rising	—	—	24.2	
• Transition falling	—	—	31.3	
SPDIF_OUT output (Load = 30pf)				
• Skew	—	—	1.5	ns
• Transition rising	—	—	13.6	
• Transition falling	—	—	18.0	
Modulating Rx clock (SPDIF_SR_CLK) period	srckp	40.0	—	ns
SPDIF_SR_CLK high period	srckph	16.0	—	ns
SPDIF_SR_CLK low period	srckpl	16.0	—	ns
Modulating Tx clock (SPDIF_ST_CLK) period	stckp	40.0	—	ns
SPDIF_ST_CLK high period	stckph	16.0	—	ns
SPDIF_ST_CLK low period	stckpl	16.0	—	ns

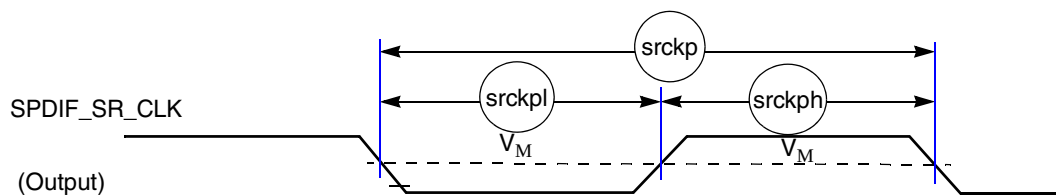


Figure 94. SPDIF_SR_CLK Timing Diagram

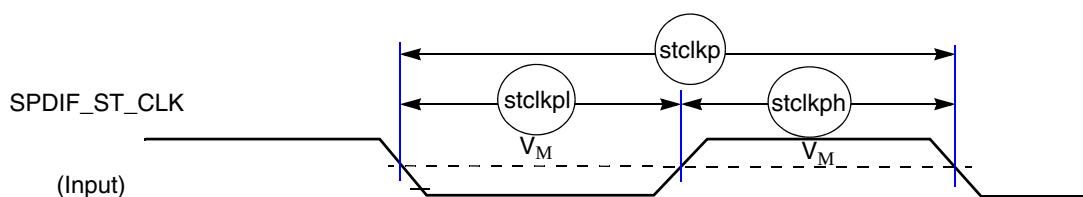


Figure 95. SPDIF_ST_CLK Timing Diagram

4.11.20 SSI Timing Parameters

This section describes the timing parameters of the SSI module. The connectivity of the serial synchronous interfaces are summarized in [Table 85](#).

Table 85. AUDMUX Port Allocation

Port	Signal Nomenclature	Type and Access
AUDMUX port 1	SSI 1	Internal
AUDMUX port 2	SSI 2	Internal
AUDMUX port 3	AUD3	External – AUD3 I/O
AUDMUX port 4	AUD4	External – EIM or CSPI1 I/O through IOMUXC
AUDMUX port 5	AUD5	External – EIM or SD1 I/O through IOMUXC
AUDMUX port 6	AUD6	External – EIM or DISP2 through IOMUXC
AUDMUX port 7	SSI 3	Internal

NOTE

The terms WL and BL used in the timing diagrams and tables refer to Word Length (WL) and Bit Length (BL).

4.11.20.1 SSI Transmitter Timing with Internal Clock

[Figure 96](#) depicts the SSI transmitter internal clock timing and [Table 86](#) lists the timing parameters for the SSI transmitter internal clock.

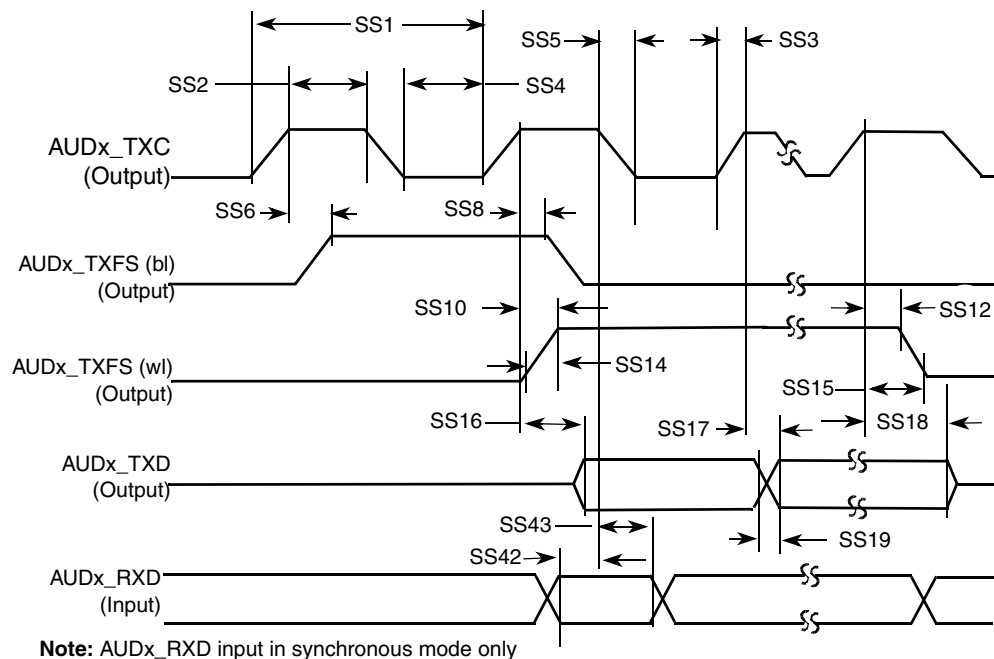


Figure 96. SSI Transmitter Internal Clock Timing Diagram

Table 87. SSI Receiver Timing with Internal Clock (continued)

ID	Parameter	Min	Max	Unit
Oversampling Clock Operation				
SS47	Oversampling clock period	15.04	—	ns
SS48	Oversampling clock high period	6.0	—	ns
SS49	Oversampling clock rise time	—	3.0	ns
SS50	Oversampling clock low period	6.0	—	ns
SS51	Oversampling clock fall time	—	3.0	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal AUDx_TXC/AUDx_RXC and/or the frame sync AUDx_TXFS/AUDx_RXFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- AUDx_TXC and AUDx_RXC refer to the Transmit and Receive sections of the SSI.
- The terms, WL and BL, refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the frame sync timing is same as that of transmit data (for example, during AC97 mode of operation).

Table 100. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition ¹			
				Default Mode (Reset Mode)	Default Function (Signal Name)	Input/Output	Value ²
CSI_D3P	F1	NVCC_MIPI	—	—	CSI_DATA3_P	—	—
CSI0_DAT10	M1	NVCC_CSI	GPIO	ALT5	GPIO5_IO28	Input	PU (100K)
CSI0_DAT11	M3	NVCC_CSI	GPIO	ALT5	GPIO5_IO29	Input	PU (100K)
CSI0_DAT12	M2	NVCC_CSI	GPIO	ALT5	GPIO5_IO30	Input	PU (100K)
CSI0_DAT13	L1	NVCC_CSI	GPIO	ALT5	GPIO5_IO31	Input	PU (100K)
CSI0_DAT14	M4	NVCC_CSI	GPIO	ALT5	GPIO6_IO00	Input	PU (100K)
CSI0_DAT15	M5	NVCC_CSI	GPIO	ALT5	GPIO6_IO01	Input	PU (100K)
CSI0_DAT16	L4	NVCC_CSI	GPIO	ALT5	GPIO6_IO02	Input	PU (100K)
CSI0_DAT17	L3	NVCC_CSI	GPIO	ALT5	GPIO6_IO03	Input	PU (100K)
CSI0_DAT18	M6	NVCC_CSI	GPIO	ALT5	GPIO6_IO04	Input	PU (100K)
CSI0_DAT19	L6	NVCC_CSI	GPIO	ALT5	GPIO6_IO05	Input	PU (100K)
CSI0_DAT4	N1	NVCC_CSI	GPIO	ALT5	GPIO5_IO22	Input	PU (100K)
CSI0_DAT5	P2	NVCC_CSI	GPIO	ALT5	GPIO5_IO23	Input	PU (100K)
CSI0_DAT6	N4	NVCC_CSI	GPIO	ALT5	GPIO5_IO24	Input	PU (100K)
CSI0_DAT7	N3	NVCC_CSI	GPIO	ALT5	GPIO5_IO25	Input	PU (100K)
CSI0_DAT8	N6	NVCC_CSI	GPIO	ALT5	GPIO5_IO26	Input	PU (100K)
CSI0_DAT9	N5	NVCC_CSI	GPIO	ALT5	GPIO5_IO27	Input	PU (100K)
CSI0_DATA_EN	P3	NVCC_CSI	GPIO	ALT5	GPIO5_IO20	Input	PU (100K)
CSI0_MCLK	P4	NVCC_CSI	GPIO	ALT5	GPIO5_IO19	Input	PU (100K)
CSI0_PIXCLK	P1	NVCC_CSI	GPIO	ALT5	GPIO5_IO18	Input	PU (100K)
CSI0_VSYNC	N2	NVCC_CSI	GPIO	ALT5	GPIO5_IO21	Input	PU (100K)
DI0_DISP_CLK	N19	NVCC_LCD	GPIO	ALT5	GPIO4_IO16	Input	PU (100K)
DI0_PIN15	N21	NVCC_LCD	GPIO	ALT5	GPIO4_IO17	Input	PU (100K)
DI0_PIN2	N25	NVCC_LCD	GPIO	ALT5	GPIO4_IO18	Input	PU (100K)
DI0_PIN3	N20	NVCC_LCD	GPIO	ALT5	GPIO4_IO19	Input	PU (100K)
DI0_PIN4	P25	NVCC_LCD	GPIO	ALT5	GPIO4_IO20	Input	PU (100K)
DISP0_DAT0	P24	NVCC_LCD	GPIO	ALT5	GPIO4_IO21	Input	PU (100K)
DISP0_DAT1	P22	NVCC_LCD	GPIO	ALT5	GPIO4_IO22	Input	PU (100K)
DISP0_DAT10	R21	NVCC_LCD	GPIO	ALT5	GPIO4_IO31	Input	PU (100K)
DISP0_DAT11	T23	NVCC_LCD	GPIO	ALT5	GPIO5_IO05	Input	PU (100K)
DISP0_DAT12	T24	NVCC_LCD	GPIO	ALT5	GPIO5_IO06	Input	PU (100K)
DISP0_DAT13	R20	NVCC_LCD	GPIO	ALT5	GPIO5_IO07	Input	PU (100K)
DISP0_DAT14	U25	NVCC_LCD	GPIO	ALT5	GPIO5_IO08	Input	PU (100K)
DISP0_DAT15	T22	NVCC_LCD	GPIO	ALT5	GPIO5_IO09	Input	PU (100K)
DISP0_DAT16	T21	NVCC_LCD	GPIO	ALT5	GPIO5_IO10	Input	PU (100K)
DISP0_DAT17	U24	NVCC_LCD	GPIO	ALT5	GPIO5_IO11	Input	PU (100K)

Table 100. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition ¹			
				Default Mode (Reset Mode)	Default Function (Signal Name)	Input/Output	Value ²
EIM_DA10	M22	NVCC_EIM2	GPIO	ALT0	EIM_AD10	Input	PU (100K)
EIM_DA11	M20	NVCC_EIM2	GPIO	ALT0	EIM_AD11	Input	PU (100K)
EIM_DA12	M24	NVCC_EIM2	GPIO	ALT0	EIM_AD12	Input	PU (100K)
EIM_DA13	M23	NVCC_EIM2	GPIO	ALT0	EIM_AD13	Input	PU (100K)
EIM_DA14	N23	NVCC_EIM2	GPIO	ALT0	EIM_AD14	Input	PU (100K)
EIM_DA15	N24	NVCC_EIM2	GPIO	ALT0	EIM_AD15	Input	PU (100K)
EIM_EB0	K21	NVCC_EIM2	GPIO	ALT0	EIM_EB0_B	Output	1
EIM_EB1	K23	NVCC_EIM2	GPIO	ALT0	EIM_EB1_B	Output	1
EIM_EB2	E22	NVCC_EIM0	GPIO	ALT5	GPIO2_IO30	Input	PU (100K)
EIM_EB3	F23	NVCC_EIM0	GPIO	ALT5	GPIO2_IO31	Input	PU (100K)
EIM_LBA	K22	NVCC_EIM1	GPIO	ALT0	EIM_LBA_B	Output	1
EIM_OE	J24	NVCC_EIM1	GPIO	ALT0	EIM_OE	Output	1
EIM_RW	K20	NVCC_EIM1	GPIO	ALT0	EIM_RW	Output	1
EIM_WAIT	M25	NVCC_EIM2	GPIO	ALT0	EIM_WAIT	Input	PU (100K)
ENET_CRS_DV	U21	NVCC_ENET	GPIO	ALT5	GPIO1_IO25	Input	PU (100K)
ENET_MDC	V20	NVCC_ENET	GPIO	ALT5	GPIO1_IO31	Input	PU (100K)
ENET_MDIO	V23	NVCC_ENET	GPIO	ALT5	GPIO1_IO22	Input	PU (100K)
ENET_REF_CLK ³	V22	NVCC_ENET	GPIO	ALT5	GPIO1_IO23	Input	PU (100K)
ENET_RX_ER	W23	NVCC_ENET	GPIO	ALT5	GPIO1_IO24	Input	PU (100K)
ENET_RXD0	W21	NVCC_ENET	GPIO	ALT5	GPIO1_IO27	Input	PU (100K)
ENET_RXD1	W22	NVCC_ENET	GPIO	ALT5	GPIO1_IO26	Input	PU (100K)
ENET_TX_EN	V21	NVCC_ENET	GPIO	ALT5	GPIO1_IO28	Input	PU (100K)
ENET_TXD0	U20	NVCC_ENET	GPIO	ALT5	GPIO1_IO30	Input	PU (100K)
ENET_TXD1	W20	NVCC_ENET	GPIO	ALT5	GPIO1_IO29	Input	PU (100K)
GPIO_0	T5	NVCC_GPIO	GPIO	ALT5	GPIO1_IO00	Input	PD (100K)
GPIO_1	T4	NVCC_GPIO	GPIO	ALT5	GPIO1_IO01	Input	PU (100K)
GPIO_16	R2	NVCC_GPIO	GPIO	ALT5	GPIO7_IO11	Input	PU (100K)
GPIO_17	R1	NVCC_GPIO	GPIO	ALT5	GPIO7_IO12	Input	PU (100K)
GPIO_18	P6	NVCC_GPIO	GPIO	ALT5	GPIO7_IO13	Input	PU (100K)
GPIO_19	P5	NVCC_GPIO	GPIO	ALT5	GPIO4_IO05	Input	PU (100K)
GPIO_2	T1	NVCC_GPIO	GPIO	ALT5	GPIO1_IO02	Input	PU (100K)
GPIO_3	R7	NVCC_GPIO	GPIO	ALT5	GPIO1_IO03	Input	PU (100K)
GPIO_4	R6	NVCC_GPIO	GPIO	ALT5	GPIO1_IO04	Input	PU (100K)
GPIO_5	R4	NVCC_GPIO	GPIO	ALT5	GPIO1_IO05	Input	PU (100K)
GPIO_6	T3	NVCC_GPIO	GPIO	ALT5	GPIO1_IO06	Input	PU (100K)
GPIO_7	R3	NVCC_GPIO	GPIO	ALT5	GPIO1_IO07	Input	PU (100K)