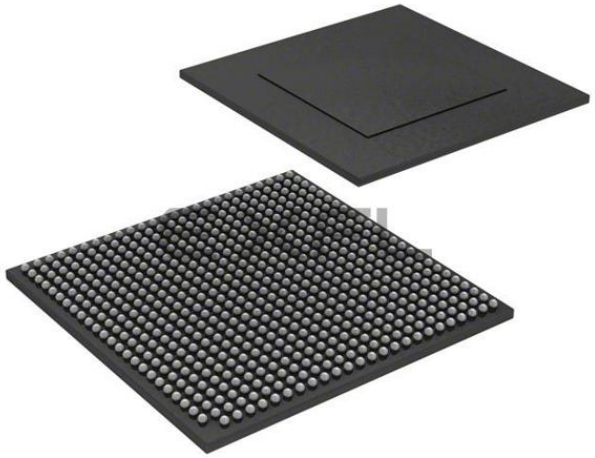

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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | ARM® Cortex®-A9 |
| Number of Cores/Bus Width | 4 Core, 32-Bit |
| Speed | 1.0GHz |
| Co-Processors/DSP | Multimedia; NEON™ SIMD |
| RAM Controllers | LPDDR2, LVDDR3, DDR3 |
| Graphics Acceleration | Yes |
| Display & Interface Controllers | Keypad, LCD |
| Ethernet | 10/100/1000Mbps (1) |
| SATA | SATA 3Gbps (1) |
| USB | USB 2.0 + PHY (4) |
| Voltage - I/O | 1.8V, 2.5V, 2.8V, 3.3V |
| Operating Temperature | -40°C ~ 125°C (TJ) |
| Security Features | ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection |
| Package / Case | 624-FBGA, FCBGA |
| Supplier Device Package | 624-FCBGA (21x21) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6q6avt10acr |

## 1.1 Ordering Information

Table 1shows examples of orderable part numbers covered by this data sheet. This table does not include all possible orderable part numbers. The latest part numbers are available on freescale.com/imx6series. If your desired part number is not listed in the table, or you have questions about available parts, see freescale.com/imx6series or contact your Freescale representative.

**Table 1. Example Orderable Part Numbers**

| Part Number | Quad/Dual CPU | Options | Speed[1] Grade | Temperature Grade | Package |
|---|---|---|---|---|---|
| MCIMX6Q6AVT10AC | i.MX 6Quad | With VPU, GPU | 1 GHz | Automotive | 21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded) |
| MCIMX6Q6AVT10AD | i.MX 6Quad | With VPU, GPU | 1 GHz | Automotive | 21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded) |
| MCIMX6Q4AVT10AC | i.MX 6Quad | With GPU, no VPU | 1 GHz | Automotive | 21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded) |
| MCIMX6Q4AVT10AD | i.MX 6Quad | With GPU, no VPU | 1 GHz | Automotive | 21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded) |
| MCIMX6Q6AVT08AC | i.MX 6Quad | With VPU, GPU | 852 MHz | Automotive | 21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded) |
| MCIMX6Q6AVT08AD | i.MX 6Quad | With VPU, GPU | 852 MHz | Automotive | 21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded) |
| MCIMX6Q4AVT08AC | i.MX 6Quad | With GPU, no VPU | 852 MHz | Automotive | 21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded) |
| MCIMX6Q4AVT08AD | i.MX 6Quad | With GPU, no VPU | 852 MHz | Automotive | 21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded) |
| MCIMX6D6AVT10AC | i.MX 6Dual | With VPU, GPU | 1 GHz | Automotive | 21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded) |
| MCIMX6D6AVT10AD | i.MX 6Dual | With VPU, GPU | 1 GHz | Automotive | 21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded) |
| MCIMX6D4AVT10AC | i.MX 6Dual | With GPU, no VPU | 1 GHz | Automotive | 21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded) |
| MCIMX6D4AVT10AD | i.MX 6Dual | With GPU, no VPU | 1 GHz | Automotive | 21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded) |
| MCIMX6D6AVT08AC | i.MX 6Dual | With VPU, GPU | 852 MHz | Automotive | 21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded) |
| MCIMX6D6AVT08AD | i.MX 6Dual | With VPU, GPU | 852 MHz | Automotive | 21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded) |
| MCIMX6D4AVT08AC | i.MX 6Dual | With GPU, no VPU | 852 MHz | Automotive1 | 21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded) |
| MCIMX6D4AVT08AD | i.MX 6Dual | With GPU, no VPU | 852 MHz | Automotive | 21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded) |

[1] If a 24 MHz input clock is used (required for USB), the maximum SoC speed is limited to 996 MHz.

## 1.2 Features

The i.MX 6Dual/6Quad processors are based on ARM Cortex-A9 MPCore platform, which has the following features:

- ARM Cortex-A9 MPCore 4xCPU processor (with TrustZone®)
- The core configuration is symmetric, where each core includes:
  - 32 KByte L1 Instruction Cache
  - 32 KByte L1 Data Cache
  - Private Timer and Watchdog
  - Cortex-A9 NEON MPE (Media Processing Engine) Co-processor

The ARM Cortex-A9 MPCore complex includes:

- General Interrupt Controller (GIC) with 128 interrupt support
- Global Timer
- Snoop Control Unit (SCU)
- 1 MB unified I/D L2 cache, shared by two/four cores
- Two Master AXI (64-bit) bus interfaces output of L2 cache
- Frequency of the core (including Neon and L1 cache) as per Table 6.
- NEON MPE coprocessor
  - SIMD Media Processing Architecture
  - NEON register file with 32x64-bit general-purpose registers
  - NEON Integer execute pipeline (ALU, Shift, MAC)
  - NEON dual, single-precision floating point execute pipeline (FADD, FMUL)
  - NEON load/store and permute pipeline

The SoC-level memory system consists of the following additional components:

  - Boot ROM, including HAB (96 KB)
  - Internal multimedia / shared, fast access RAM (OCRAM, 256 KB)
  - Secure/non-secure RAM (16 KB)
- External memory interfaces:
  - 16-bit, 32-bit, and 64-bit DDR3-1066, LVDDR3-1066, and 1/2 LPDDR2-1066 channels, supporting DDR interleaving mode, for 2x32 LPDDR2-1066
  - 8-bit NAND-Flash, including support for Raw MLC/SLC, 2 KB, 4 KB, and 8 KB page size, BA-NAND, PBA-NAND, LBA-NAND, OneNAND™ and others. BCH ECC up to 40 bit.
  - 16/32-bit NOR Flash. All EIMv2 pins are muxed on other interfaces.
  - 16/32-bit PSRAM, Cellular RAM

Each i.MX 6Dual/6Quad processor enables the following interfaces to external devices (some of them are muxed and not available simultaneously):

- Hard Disk Drives—SATA II, 3.0 Gbps

**Table 2. i.MX 6Dual/6Quad Modules List (continued)**

| Block Mnemonic | Block Name | Subsystem | Brief Description |
|---|---|---|---|
| EPIT-1<br>EPIT-2 | Enhanced Periodic Interrupt Timer | Timer Peripherals | Each EPIT is a 32-bit “set and forget” timer that starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler for division of input clock frequency to get the required time setting for the interrupts to occur, and counter value can be programmed on the fly. |
| ESAI | Enhanced Serial Audio Interface | Connectivity Peripherals | The Enhanced Serial Audio Interface (ESAI) provides a full-duplex serial port for serial communication with a variety of serial devices, including industry-standard codecs, SPDIF transceivers, and other processors. The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. All serial transfers are synchronized to a clock. Additional synchronization signals are used to delineate the word frames. The normal mode of operation is used to transfer data at a periodic rate, one word per period. The network mode is also intended for periodic transfers; however, it supports up to 32 words (time slots) per period. This mode can be used to build time division multiplexed (TDM) networks. In contrast, the on-demand mode is intended for non-periodic transfers of data and to transfer data serially at high speed when the data becomes available.<br>The ESAI has 12 pins for data and clocking connection to external devices. |
| FlexCAN-1<br>FlexCAN-2 | Flexible Controller Area Network | Connectivity Peripherals | The CAN protocol was primarily, but not only, designed to be used as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the Electromagnetic interference (EMI) environment of a vehicle, cost-effectiveness and required bandwidth. The FlexCAN module is a full implementation of the CAN protocol specification, Version 2.0 B, which supports both standard and extended message frames. |
| GPIO-1<br>GPIO-2<br>GPIO-3<br>GPIO-4<br>GPIO-5<br>GPIO-6<br>GPIO-7 | General Purpose I/O Modules | System Control Peripherals | Used for general purpose input/output to external devices. Each GPIO module supports 32 bits of I/O. |
| GPMI | General Purpose Media Interface | Connectivity Peripherals | The GPMI module supports up to 8x NAND devices. 40-bit ECC encryption/decryption for NAND Flash controller (GPMI2). The GPMI supports separate DMA channels per NAND device. |
| GPT | General Purpose Timer | Timer Peripherals | Each GPT is a 32-bit “free-running” or “set and forget” mode timer with programmable prescaler and compare and capture register. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in “set and forget” mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock. |

### 4.1.3 Operating Ranges

Table 6 provides the operating ranges of the i.MX 6Dual/6Quad processors.

**Table 6. Operating Ranges**

| Parameter Description | Symbol | Min | Typ | Max[1] | Unit | Comment[2] |
|---|---|---|---|---|---|---|
| Run mode: LDO enabled | VDD_ARM_IN VDD_ARM23_IN[3] | 1.35[4] | — | 1.5 | V | LDO Output Set Point (VDD_ARM_CAP[5]) of 1.225 V minimum for operation up to 852 MHz or 996 MHz (depending on the device speed grade). |
| | | 1.275[4] | — | 1.5 | V | LDO Output Set Point (VDD_ARM_CAP[5]) of 1.150 V minimum for operation up to 792 MHz. |
| | | 1.05[4] | — | 1.5 | V | LDO Output Set Point (VDD_ARM_CAP[5]) of 0.925 V minimum for operation up to 396 MHz. |
| | VDD_SOC_IN[6] | 1.350[4] | — | 1.5 | V | 264 MHz < VPU ≤ 352 MHz; VDDSOC and VDDPU LDO outputs (VDD_SOC_CAP and VDD_PU_CAP) require 1.225 V minimum. |
| | | 1.275[4,7] | — | 1.5 | V | VPU ≤ 264 MHz; VDDSOC and VDDPU LDO outputs (VDD_SOC_CAP and VDD_PU_CAP) require 1.15 V minimum. |
| Run mode: LDO bypassed[8] | VDD_ARM_IN VDD_ARM23_IN[3] | 1.225 | — | 1.3 | V | LDO bypassed for operation up to 852 MHz or 996 MHz (depending on the device speed grade). |
| | | 1.150 | — | 1.3 | V | LDO bypassed for operation up to 792 MHz. |
| | | 0.925 | — | 1.3 | V | LDO bypassed for operation up to 396 MHz. |
| | VDD_SOC_IN[6] | 1.225 | — | 1.3 | V | 264 MHz < VPU ≤ 352 MHz |
| | | 1.15 | — | 1.3 | V | VPU ≤ 264 MHz |
| Standby/DSM mode | VDD_ARM_IN VDD_ARM23_IN[3] | 0.9 | — | 1.3 | V | See Table 9, "Stop Mode Current and Power Consumption," on page 26. |
| | VDD_SOC_IN | 0.9 | — | 1.3 | V | |
| VDD_HIGH internal regulator | VDD_HIGH_IN[9] | 2.7 | — | 3.3 | V | Must match the range of voltages that the rechargeable backup battery supports. |
| Backup battery supply range | VDD_SNVS_IN[9] | 2.8 | — | 3.3 | V | Should be supplied from the same supply as VDD_HIGH_IN, if the system does not require keeping real time and other data on OFF state. |
| USB supply voltages | USB_OTG_VBUS | 4.4 | — | 5.25 | V | — |
| | USB_H1_VBUS | 4.4 | — | 5.25 | V | — |
| DDR I/O supply | NVCC_DRAM | 1.14 | 1.2 | 1.3 | V | LPDDR2 |
| | | 1.425 | 1.5 | 1.575 | V | DDR3 |
| | | 1.283 | 1.35 | 1.45 | V | DDR3_L |
| Supply for RGMII I/O power group[10] | NVCC_RGMII | 1.15 | — | 2.625 | V | • 1.15 V – 1.30 V in HSIC 1.2 V mode<br>• 1.43 V – 1.58 V in RGMII 1.5 V mode<br>• 1.70 V – 1.90 V in RGMII 1.8 V mode<br>• 2.25 V – 2.625 V in RGMII 2.5 V mode |

**Table 9. Stop Mode Current and Power Consumption (continued)**

| Mode | Test Conditions | Supply | Typical[1] | Unit |
|---|---|---|---|---|
| STOP_ON | • ARM LDO set to 0.9 V<br>• SoC and PU LDOs set to 1.225 V<br>• HIGH LDO set to 2.5 V<br>• PLLs disabled<br>• DDR is in self refresh | VDD_ARM_IN (1.4 V) | 7.5 | mA |
| | | VDD_SOC_IN (1.4 V) | 22 | mA |
| | | VDD_HIGH_IN (3.0 V) | 3.7 | mA |
| | | Total | 52 | mW |
| STOP_OFF | • ARM LDO set to 0.9 V<br>• SoC LDO set to 1.225 V<br>• PU LDO is power gated<br>• HIGH LDO set to 2.5 V<br>• PLLs disabled<br>• DDR is in self refresh | VDD_ARM_IN (1.4 V) | 7.5 | mA |
| | | VDD_SOC_IN (1.4 V) | 13.5 | mA |
| | | VDD_HIGH_IN (3.0 V) | 3.7 | mA |
| | | Total | 41 | mW |
| STANDBY | • ARM and PU LDOs are power gated<br>• SoC LDO is in bypass<br>• HIGH LDO is set to 2.5 V<br>• PLLs are disabled<br>• Low voltage<br>• Well Bias ON<br>• Crystal oscillator is enabled | VDD_ARM_IN (0.9 V) | 0.1 | mA |
| | | VDD_SOC_IN (0.9 V) | 13 | mA |
| | | VDD_HIGH_IN (3.0 V) | 3.7 | mA |
| | | Total | 22 | mW |
| Deep Sleep Mode (DSM) | • ARM and PU LDOs are power gated<br>• SoC LDO is in bypass<br>• HIGH LDO is set to 2.5 V<br>• PLLs are disabled<br>• Low voltage<br>• Well Bias ON<br>• Crystal oscillator and bandgap are disabled | VDD_ARM_IN (0.9 V) | 0.1 | mA |
| | | VDD_SOC_IN (0.9 V) | 2 | mA |
| | | VDD_HIGH_IN (3.0 V) | 0.5 | mA |
| | | Total | 3.4 | mW |
| SNVS Only | • VDD_SNVS_IN powered<br>• All other supplies off<br>• SRTC running | VDD_SNVS_IN (2.8V) | 41 | µA |
| | | Total | 115 | µW |

1 The typical values shown here are for information only and are not guaranteed. These values are average values measured on a worst-case wafer at 25°C.

## 4.6 I/O DC Parameters

This section includes the DC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2 and DDR3/DDR3L modes
- LVDS I/O
- MLB I/O

**NOTE**

The term ‘OVDD’ in this section refers to the associated supply rail of an input or output.

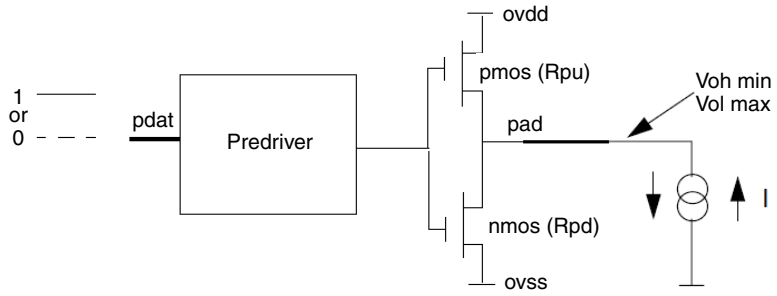


**Figure 3. Circuit for Parameters Voh and Vol for I/O Cells**

### 4.6.1 XTALI and RTC_XTALI (Clock Inputs) DC Parameters

Table 21 shows the DC parameters for the clock inputs.

**Table 21. XTALI and RTC_XTALI DC Parameters**

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| XTALI high-level DC input voltage | Vih | — | 0.8 x NVCC_PLL_OUT | — | NVCC_PLL_ OUT | V |
| XTALI low-level DC input voltage | Vil | — | 0 | — | 0.2 | V |
| RTC_XTALI high-level DC input voltage | Vih | — | 0.8 | — | 1.1 | V |
| RTC_XTALI low-level DC input voltage | Vil | — | 0 | — | 0.2 | V |
| Input capacitance | $C_{IN}$ | Simulated data | — | 5 | — | pF |
| Startup current | $I_{XTALI\_STARTUP}$ | Power-on startup for 0.15msec with a driven 32KHz RTC clock @ 1.1V. This current draw is present even if an external clock source directly drives XTALI | — | — | 600 | uA |
| DC input current | $I_{XTALI\_DC}$ | — | — | — | 2.5 | uA |

### 4.7.2 DDR I/O AC Parameters

The LPDDR2 interface mode fully complies with JESD209-2B LPDDR2 JEDEC standard release June, 2009. The DDR3/DDR3L interface mode fully complies with JESD79-3D DDR3 JEDEC standard release April, 2008.

Table 29 shows the AC parameters for DDR I/O operating in LPDDR2 mode.

**Table 29. DDR I/O LPDDR2 Mode AC Parameters[1]**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| AC input logic high | Vih(ac) | — | Vref + 0.22 | — | OVDD | V |
| AC input logic low | Vil(ac) | — | 0 | — | Vref – 0.22 | V |
| AC differential input high voltage[2] | Vidh(ac) | — | 0.44 | — | — | V |
| AC differential input low voltage | Vidl(ac) | — | — | — | 0.44 | V |
| Input AC differential cross point voltage[3] | Vix(ac) | Relative to Vref | -0.12 | — | 0.12 | V |
| Over/undershoot peak | Vpeak | — | — | — | 0.35 | V |
| Over/undershoot area (above OVDD or below OVSS) | Varea | 533 MHz | — | — | 0.3 | V-ns |
| Single output slew rate, measured between Vol(ac) and Voh(ac) | tsr | 50 Ω to Vref.<br>5 pF load.<br>Drive impedance = 4 0 Ω ±30% | 1.5 | — | 3.5 | V/ns |
| | | 50 Ω to Vref.<br>5pF load.<br>Drive impedance = 60 Ω ±30% | 1 | — | 2.5 | |
| Skew between pad rise/fall asymmetry + skew caused by SSN | $t_{SKD}$ | clk = 533 MHz | — | — | 0.1 | ns |

1 Note that the JEDEC LPDDR2 specification (JESD209_2B) supersedes any specification in this document.

2 Vid(ac) specifies the input differential voltage |Vtr – Vcp| required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac) – Vil(ac).

3 The typical value of Vix(ac) is expected to be about 0.5 × OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

Table 30 shows the AC parameters for DDR I/O operating in DDR3/DDR3L mode.

**Table 30. DDR I/O DDR3/DDR3L Mode AC Parameters[1]**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| AC input logic high | Vih(ac) | — | Vref + 0.175 | — | OVDD | V |
| AC input logic low | Vil(ac) | — | 0 | — | Vref – 0.175 | V |
| AC differential input voltage[2] | Vid(ac) | — | 0.35 | — | — | V |
| Input AC differential cross point voltage[3] | Vix(ac) | Relative to Vref | Vref – 0.15 | — | Vref + 0.15 | V |
| Over/undershoot peak | Vpeak | — | — | — | 0.4 | V |
| Over/undershoot area (above OVDD or below OVSS) | Varea | 533 MHz | — | — | 0.5 | V-ns |

**Table 40. EIM Bus Timing Parameters (continued)**

| ID | Parameter | Min[1] | Max[1] | Unit |
|---|---|---|---|---|
| WE4 | Clock rise to address valid | -0.5 × t × (k+1) - 1.25 | -0.5 × t × (k+1) + 2.25 | ns |
| WE5 | Clock rise to address invalid | 0.5 × t × (k+1) - 1.25 | 0.5 × t × (k+1) + 2.25 | ns |
| WE6 | Clock rise to EIM_CSx_B valid | -0.5 × t × (k+1) - 1.25 | -0.5 × t × (k+1) + 2.25 | ns |
| WE7 | Clock rise to EIM_CSx_B invalid | 0.5 × t × (k+1) - 1.25 | 0.5 × t × (k+1) + 2.25 | ns |
| WE8 | Clock rise to EIM_WE_B valid | -0.5 × t × (k+1) - 1.25 | -0.5 × t × (k+1) + 2.25 | ns |
| WE9 | Clock rise to EIM_WE_B invalid | 0.5 × t × (k+1) - 1.25 | 0.5 × t × (k+1) + 2.25 | ns |
| WE10 | Clock rise to EIM_OE_B valid | -0.5 × t × (k+1) - 1.25 | -0.5 × t × (k+1) + 2.25 | ns |
| WE11 | Clock rise to EIM_OE_B invalid | 0.5 × t × (k+1) - 1.25 | 0.5 × t × (k+1) + 2.25 | ns |
| WE12 | Clock rise to EIM_EBx_B valid | -0.5 × t × (k+1) - 1.25 | -0.5 × t × (k+1) + 2.25 | ns |
| WE13 | Clock rise to EIM_EBx_B invalid | 0.5 × t × (k+1) - 1.25 | 0.5 × t × (k+1) + 2.25 | ns |
| WE14 | Clock rise to EIM_LBA_B valid | -0.5 × t × (k+1) - 1.25 | -0.5 × t × (k+1) + 2.25 | ns |
| WE15 | Clock rise to EIM_LBA_B invalid | 0.5 × t × (k+1) - 1.25 | 0.5 × t × (k+1) + 2.25 | ns |
| WE16 | Clock rise to output data valid | -0.5 × t × (k+1) - 1.25 | -0.5 × t × (k+1) + 2.25 | ns |
| WE17 | Clock rise to output data invalid | 0.5 × t × (k+1) - 1.25 | 0.5 × t × (k+1) + 2.25 | ns |
| WE18 | Input data setup time to clock rise | 2.3 | — | ns |
| WE19 | Input data hold time from clock rise | 2 | — | ns |
| WE20 | EIM_WAIT_B setup time to clock rise | 2 | — | ns |
| WE21 | EIM_WAIT_B hold time from clock rise | 2 | — | ns |

1 k represents register setting BCD value.

2 t is clock period (1/Freq). For 104 MHz, t = 9.165 ns.

2 In this table:
- t means clock period from axi_clk frequency.
- CSA means register setting for WCSA when in write operations or RCSA when in read operations.
- CSN means register setting for WCSN when in write operations or RCSN when in read operations.
- ADVN means register setting for WADVN when in write operations or RADVN when in read operations.
- ADVA means register setting for WADVA when in write operations or RADVA when in read operations.

## 4.9.4 DDR SDRAM Specific Parameters (DDR3/DDR3L and LPDDR2)

### 4.9.4.1 DDR3/DDR3L Parameters

Figure 24 shows the DDR3/DDR3L basic timing diagram. The timing parameters for this diagram appear in Table 42.

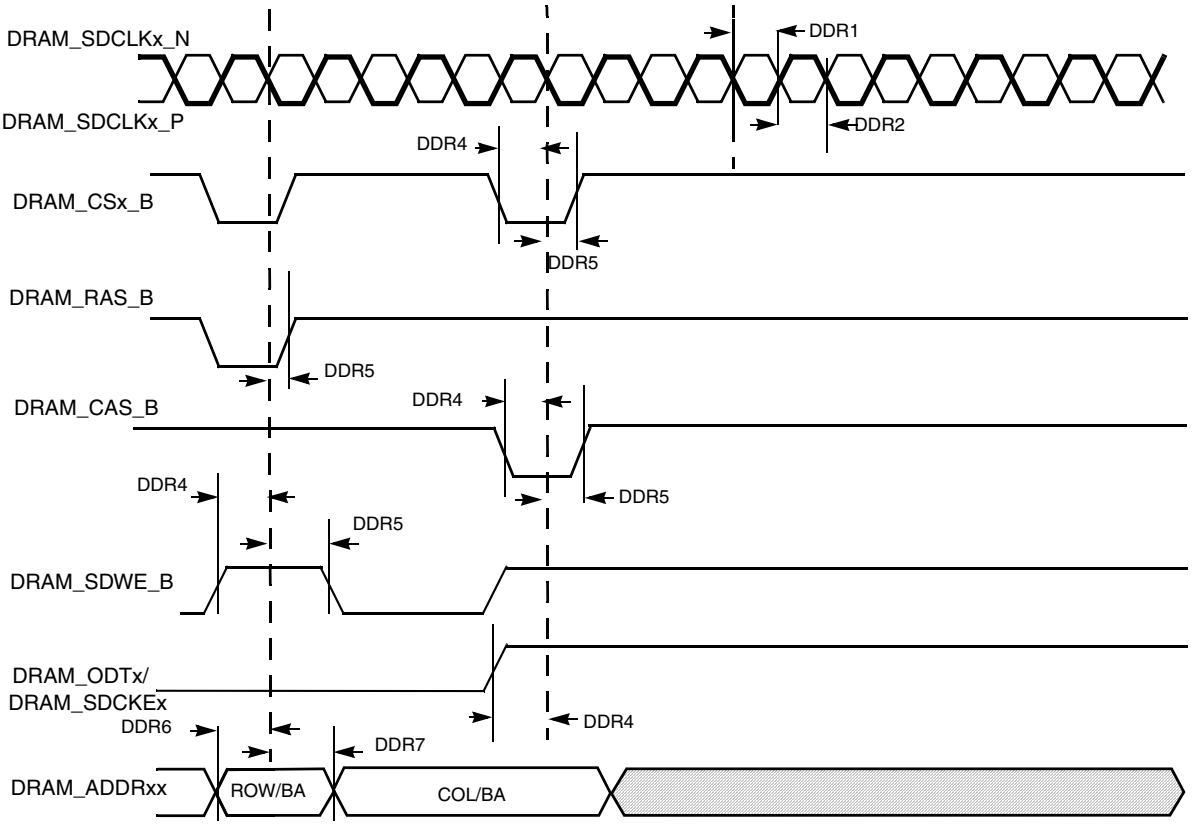


**Figure 24. DDR3/DDR3L Command and Address Timing Diagram**

**Table 42. DDR3/DDR3L Timing Parameter**

| ID | Parameter[1,2] | Symbol | CK = 532 MHz | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| DDR1 | DRAM_SDCLKx_P clock high-level width | $t_{CH}$ | 0.47 | 0.53 | $t_{CK}$ |
| DDR2 | DRAM_SDCLKx_P clock low-level width | $t_{CL}$ | 0.47 | 0.53 | $t_{CK}$ |

**Table 42. DDR3/DDR3L Timing Parameter (continued)**

| ID | Parameter[1,2] | Symbol | CK = 532 MHz | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| DDR4 | DRAM_CSx_B, DRAM_RAS_B, DRAM_CAS_B, DRAM_SDCKEx, DRAM_SDWE_B, DRAM_ODTx setup time | tIS | 500 | — | ps |
| DDR5 | DRAM_CSx_B, DRAM_RAS_B, DRAM_CAS_B, DRAM_SDCKEx, DRAM_SDWE_B, DRAM_ODTx hold time | tIH | 400 | — | ps |
| DDR6 | Address output setup time | tIS | 500 | — | ps |
| DDR7 | Address output hold time | tIH | 400 | — | ps |

1 All measurements are in reference to Vref level.

2 Measurements were done using balanced load and 25 Ω resistor from outputs to DRAM_VREF.

Figure 25 shows the DDR3/DDR3L write timing diagram. The timing parameters for this diagram appear in Table 43.

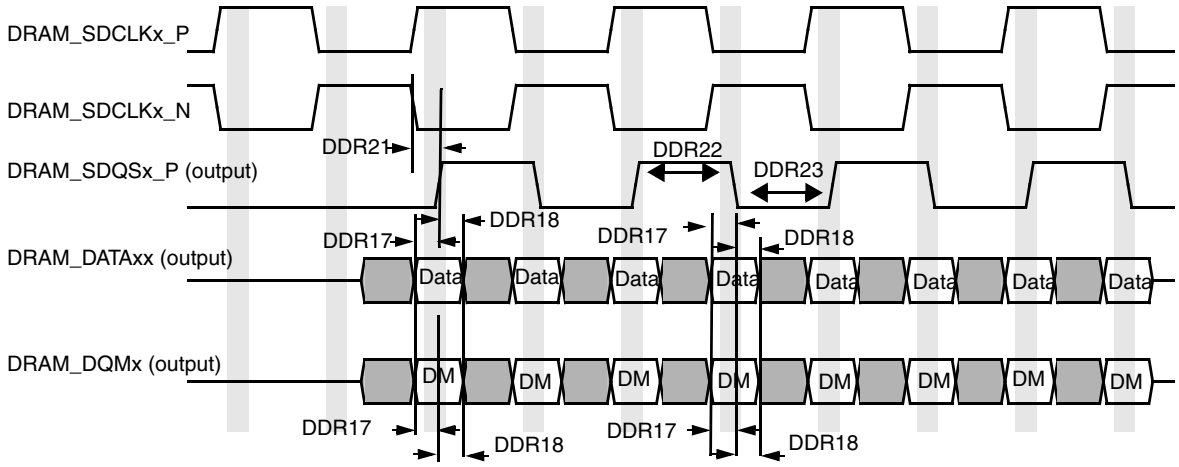


**Figure 25. DDR3/DDR3L Write Cycle**

**Table 43. DDR3/DDR3L Write Cycle**

| ID | Parameter[1,2,3] | Symbol | CK = 532 MHz | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| DDR17 | DRAM_DATAxx and DRAM_DQMx setup time to DRAM_SDQSx_P (differential strobe) | tDS | 125[4] | — | ps |
| DDR18 | DRAM_DATAxx and DRAM_DQMx hold time to DRAM_SDQSx_P (differential strobe) | tDH | 150[4] | — | ps |
| DDR21 | DRAM_SDQSx_P latching rising transitions to associated clock edges | tDQSS | -0.25 | +0.25 | tCK |
| DDR22 | DRAM_SDQSx_P high level width | tDQSH | 0.45 | 0.55 | tCK |
| DDR23 | DRAM_SDQSx_P low level width | tDQSL | 0.45 | 0.55 | tCK |

1 To receive the reported setup and hold values, write calibration should be performed to locate the DRAM_SDQSx_P in the middle of DRAM_DATAxx window.

2 All measurements are in reference to Vref level.

3 Measurements were taken using balanced load and 25 Ω resistor from outputs to DRAM_VREF

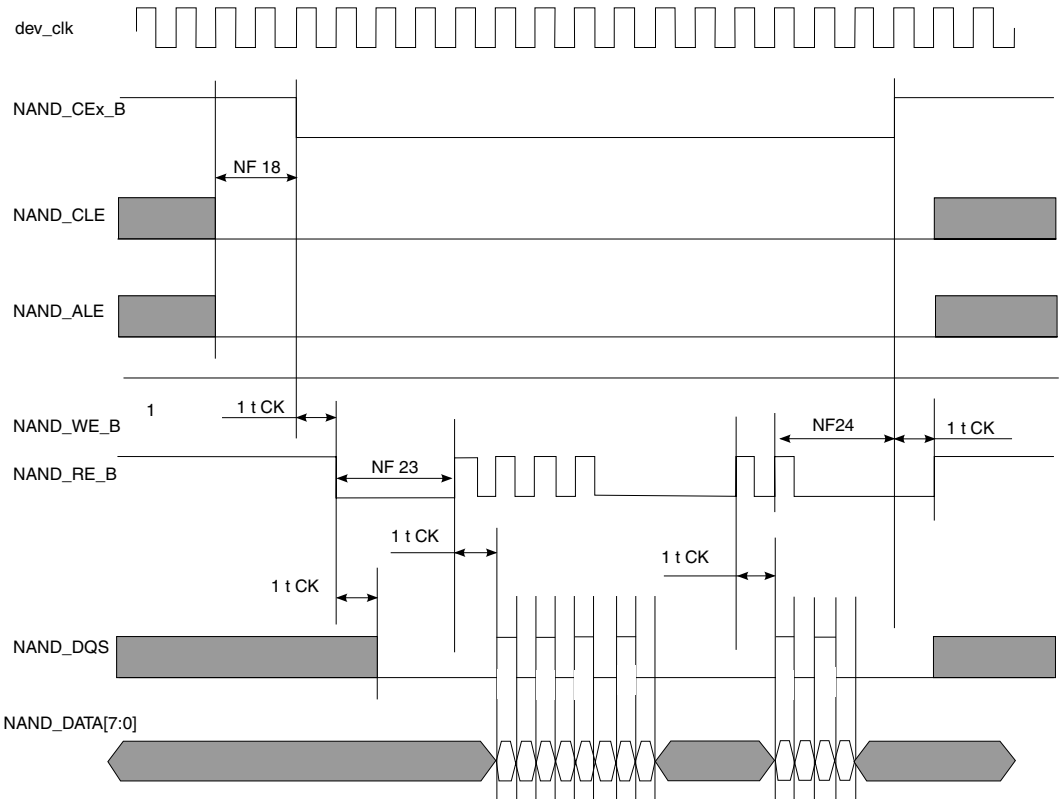


**Figure 40. Samsung Toggle Mode Data Read Timing**

**Table 50. Samsung Toggle Mode Timing Parameters[1]**

| ID | Parameter | Symbol | Timing T = GPMI Clock Cycle | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| NF1 | NAND_CLE setup time | tCLS | (AS + DS) × T - 0.12 [see 2,3] | | — |
| NF2 | NAND_CLE hold time | tCLH | DH × T - 0.72 [see 2] | | — |
| NF3 | NAND_CEx_B setup time | tCS | (AS + DS) × T - 0.58 [see 3,2] | | — |
| NF4 | NAND_CEx_B hold time | tCH | DH × T - 1 [see 2] | | — |
| NF5 | NAND_WE_B pulse width | tWP | DS × T [see 2] | | — |
| NF6 | NAND_ALE setup time | tALS | (AS + DS) × T - 0.49 [see 3,2] | | — |
| NF7 | NAND_ALE hold time | tALH | DH × T - 0.42 [see 2] | | — |
| NF8 | Command/address NAND_DATAxx setup time | tCAS | DS × T - 0.26 [see 2] | | — |
| NF9 | Command/address NAND_DATAxx hold time | tCAH | DH × T - 1.37 [see 2] | | — |
| NF18 | NAND_CEx_B access time | tCE | CE_DELAY × T [see 4,2] | — | ns |
| NF22 | clock period | tCK | — | — | ns |
| NF23 | preamble delay | tPRE | PRE_DELAY × T [see 5,2] | — | ns |
| NF24 | postamble delay | tPOST | POST_DELAY × T +0.43 [see 2] | — | ns |

**Table 54. SD/eMMC4.3 Interface Timing Specification (continued)**

| ID | Parameter | Symbols | Min | Max | Unit |
|---|---|---|---|---|---|
| **eSDHC Input/Card Outputs SD_CMD, SD_DATAx (Reference to SDx_CLK)** | | | | | |
| SD7 | eSDHC Input Setup Time | $t_{ISU}$ | 2.5 | — | ns |
| SD8 | eSDHC Input Hold Time[4] | $t_{IH}$ | 1.5 | — | ns |

1 In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

2 In normal (full) speed mode for SD/SDIO card, clock frequency can be any value between 0—25 MHz. In high-speed mode, clock frequency can be any value between 0—50 MHz.

3 In normal (full) speed mode for MMC card, clock frequency can be any value between 0—20 MHz. In high-speed mode, clock frequency can be any value between 0—52 MHz.

4 To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

### 4.11.4.2 eMMC4.4/4.41 (Dual Data Rate) eSDHCv3 AC Timing

Figure 46 depicts the timing of eMMC4.4/4.41. Table 55 lists the eMMC4.4/4.41 timing characteristics. Be aware that only SDx_DATAx is sampled on both edges of the clock (not applicable to SD_CMD).

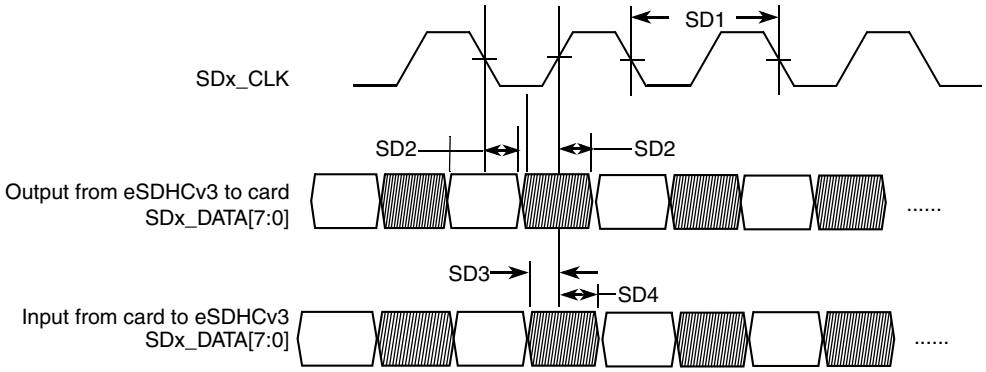


**Figure 46. eMMC4.4/4.41 Timing**

**Table 55. eMMC4.4/4.41 Interface Timing Specification**

| ID | Parameter | Symbols | Min | Max | Unit |
|---|---|---|---|---|---|
| **Card Input Clock** | | | | | |
| SD1 | Clock Frequency (EMMC4.4 DDR) | $f_{PP}$ | 0 | 52 | MHz |
| SD1 | Clock Frequency (SD3.0 DDR) | $f_{PP}$ | 0 | 50 | MHz |
| **uSDHC Output / Card Inputs SD_CMD, SD_DATAx (Reference to SD_CLK)** | | | | | |
| SD2 | uSDHC Output Delay | $t_{OD}$ | 2.5 | 7.1 | ns |
| **uSDHC Input / Card Outputs SD_CMD, SD_DATAx (Reference to SD_CLK)** | | | | | |
| SD3 | uSDHC Input Setup Time | $t_{ISU}$ | 2.6 | — | ns |
| SD4 | uSDHC Input Hold Time | $t_{IH}$ | 1.5 | — | ns |

### 4.11.5.2 RMII Mode Timing

In RMII mode, ENET_CLK is used as the REF_CLK, which is a 50 MHz ± 50 ppm continuous reference clock. ENET_RX_EN is used as the ENET_RX_EN in RMII. Other signals under RMII mode include ENET_TX_EN, ENET0_TXD[1:0], ENET_RXD[1:0] and ENET_RX_ER.

Figure 52 shows RMII mode timings. Table 61 describes the timing parameters (M16–M21) shown in the figure.

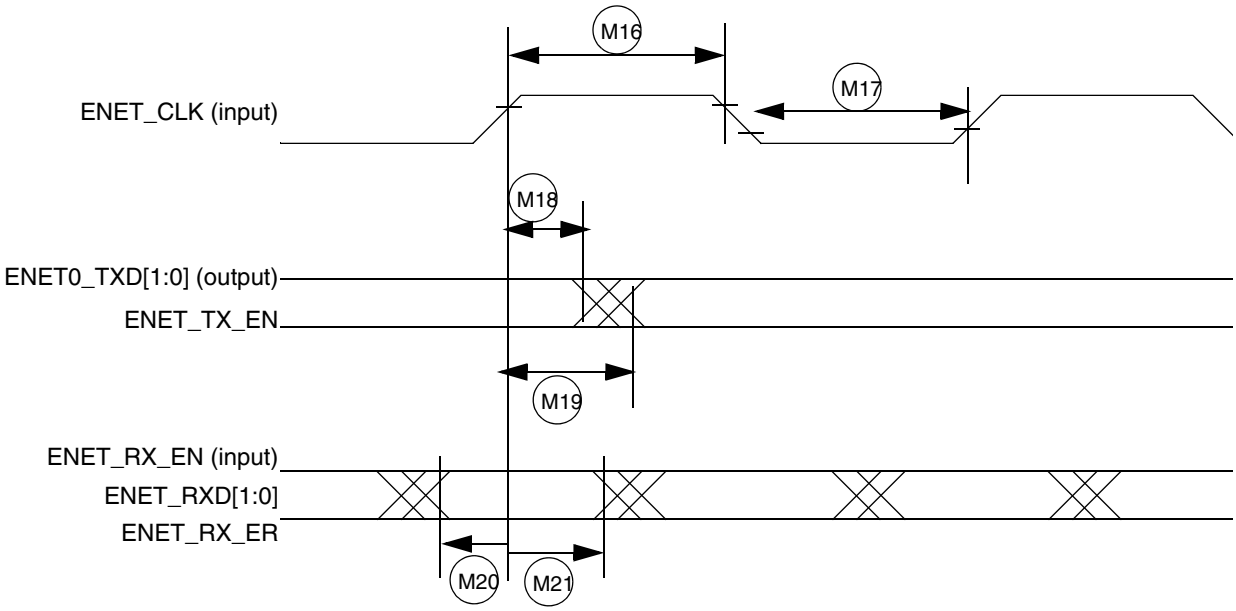


**Figure 52. RMII Mode Signal Timing Diagram**

**Table 61. RMII Signal Timing**

| ID | Characteristic | Min | Max | Unit |
|---|---|---|---|---|
| M16 | ENET_CLK pulse width high | 35% | 65% | ENET_CLK period |
| M17 | ENET_CLK pulse width low | 35% | 65% | ENET_CLK period |
| M18 | ENET_CLK to ENET0_TXD[1:0], ENET_TX_EN invalid | 4 | — | ns |
| M19 | ENET_CLK to ENET0_TXD[1:0], ENET_TX_EN valid | — | 13.5 | ns |
| M20 | ENET_RXD[1:0], ENET_RX_EN(ENET_RX_EN), ENET_RX_ER to ENET_CLK setup | 4 | — | ns |
| M21 | ENET_CLK to ENET_RXD[1:0], ENET_RX_EN, ENET_RX_ER hold | 2 | — | ns |

- The ipp_pin_1– ipp_pin_7 are general purpose synchronous pins, that can be used to provide HSYNC, VSYNC, DRDY or any else independent signal to a display.

The IPU has a system of internal binding counters for internal events (such as, HSYNC/VSYNC) calculation. The internal event (local start point) is synchronized with internal DI_CLK. A suitable control starts from the local start point with predefined UP and DOWN values to calculate control's changing points with half DI_CLK resolution. A full description of the counter system can be found in the IPU chapter of the i.MX 6Dual/6Quad reference manual (IMX6DQRM).

#### 4.11.10.5.2 Asynchronous Controls

The asynchronous control is a data-oriented signal that changes its value with an output data according to additional internal flags coming with the data.

There are special physical outputs to provide asynchronous controls, as follows:

- The ipp_d0_cs and ipp_d1_cs pins are dedicated to provide chip select signals to two displays.
- The ipp_pin_11– ipp_pin_17 are general purpose asynchronous pins, that can be used to provide WR. RD, RS or any other data-oriented signal to display.

**NOTE**

The IPU has independent signal generators for asynchronous signals toggling. When a DI decides to put a new asynchronous data on the bus, a new internal start (local start point) is generated. The signal generators calculate predefined UP and DOWN values to change pins states with half DI_CLK resolution.

### 4.11.10.6 Synchronous Interfaces to Standard Active Matrix TFT LCD Panels

#### 4.11.10.6.1 IPU Display Operating Signals

The IPU uses four control signals and data to operate a standard synchronous interface:

- IPP_DISP_CLK—Clock to display
- HSYNC—Horizontal synchronization
- VSYNC—Vertical synchronization
- DRDY—Active data

All synchronous display controls are generated on the base of an internally generated "local start point". The synchronous display controls can be placed on time axis with DI's offset, up and down parameters. The display access can be whole number of DI clock (Tdiclk) only. The IPP_DATA can not be moved relative to the local start point. The data bus of the synchronous interface is output direction only.

#### 4.11.10.6.2 LCD Interface Functional Description

Figure 68 depicts the LCD interface timing for a generic active matrix color TFT panel. In this figure, signals are shown with negative polarity. The sequence of events for active matrix interface timing is:

- DI_CLK internal DI clock is used for calculation of other controls.

**Table 73. Electrical and Timing Information (continued)**

| Symbol | Parameters | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **LP Line Drivers AC Specifications** | | | | | | |
| $t_{rlp}$,$t_{flp}$ | Single ended output rise/fall time | 15% to 85%, $C_L$<70 pF | — | — | 25 | ns |
| $t_{reo}$ | — | 30% to 85%, $C_L$<70 pF | — | — | 35 | ns |
| $\delta V/\delta t_{SR}$ | Signal slew rate | 15% to 85%, $C_L$<70 pF | — | — | 120 | mV/ns |
| $C_L$ | Load capacitance | — | 0 | — | 70 | pF |
| **HS Line Receiver AC Specifications** | | | | | | |
| $t_{SETUP[RX]}$ | Data to Clock Receiver Setup time | — | 0.15 | — | — | UI |
| $t_{HOLD[RX]}$ | Clock to Data Receiver Hold time | — | 0.15 | — | — | UI |
| $\Delta V_{CMRX(HF)}$ | Common mode interference beyond 450 MHz | — | — | — | 200 | mVpp |
| $\Delta V_{CMRX(LF)}$ | Common mode interference between 50 MHz and 450 MHz | — | -50 | — | 50 | mVpp |
| $C_{CM}$ | Common mode termination | — | — | — | 60 | pF |
| **LP Line Receiver AC Specifications** | | | | | | |
| $e_{SPIKE}$ | Input pulse rejection | — | — | — | 300 | Vps |
| $T_{MIN}$ | Minimum pulse response | — | 50 | — | — | ns |
| $V_{INT}$ | Pk-to-Pk interference voltage | — | — | — | 400 | mV |
| $f_{INT}$ | Interference frequency | — | 450 | — | — | MHz |
| **Model Parameters used for Driver Load switching performance evaluation** | | | | | | |
| $C_{PAD}$ | Equivalent Single ended I/O PAD capacitance. | — | — | — | 1 | pF |
| $C_{PIN}$ | Equivalent Single ended Package + PCB capacitance. | — | — | — | 2 | pF |
| $L_S$ | Equivalent wire bond series inductance | — | — | — | 1.5 | nH |
| $R_S$ | Equivalent wire bond series resistance | — | — | — | 0.15 | Ω |
| $R_L$ | Load Resistance | — | 80 | 100 | 125 | Ω |

### 4.11.12.9 Low-Power Receiver Timing

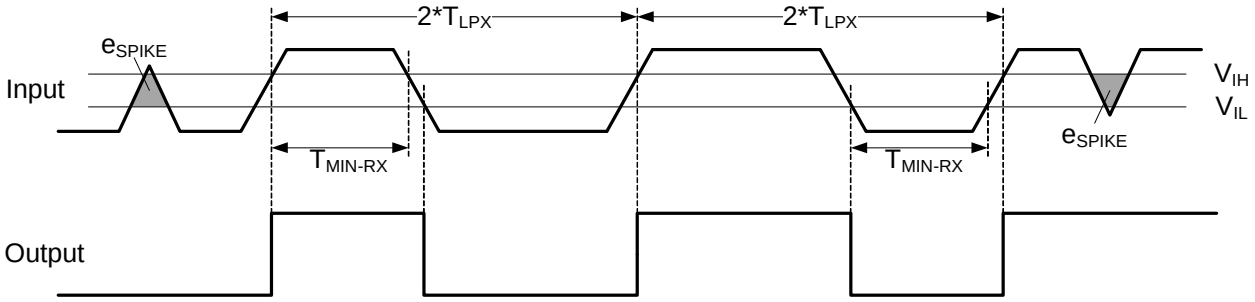


**Figure 78. Input Glitch Rejection of Low-Power Receivers**

## 4.11.13 HSI Host Controller Timing Parameters

This section describes the timing parameters of the HSI Host Controller which are compliant with High-Speed Synchronous Serial Interface (HSI) Physical Layer specification version 1.01.

### 4.11.13.1 Synchronous Data Flow

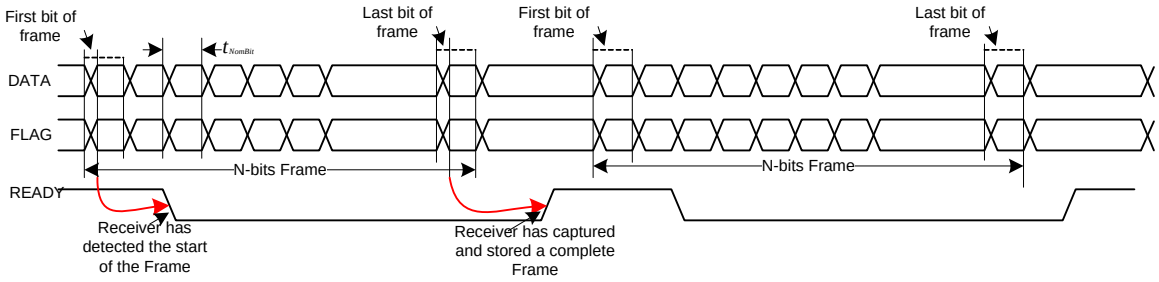


**Figure 79. Synchronized Data Flow READY Signal Timing (Frame and Stream Transmission)**

### 4.11.13.2 Pipelined Data Flow

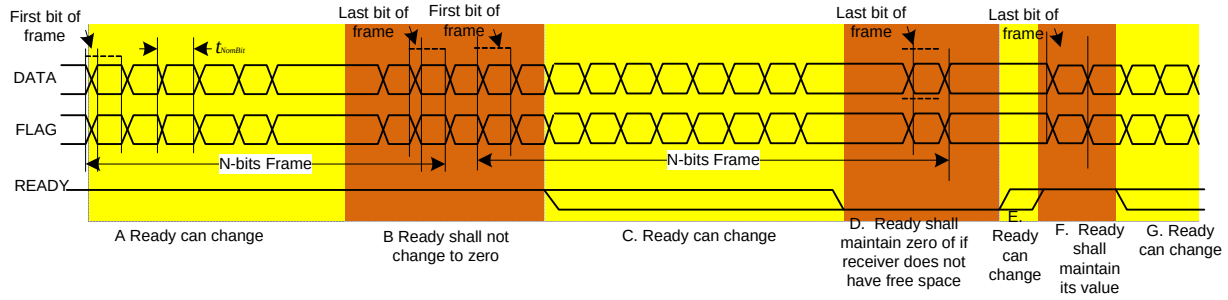


**Figure 80. Pipelined Data Flow READY Signal Timing (Frame Transmission Mode)**

### 4.11.13.3 Receiver Real-Time Data Flow

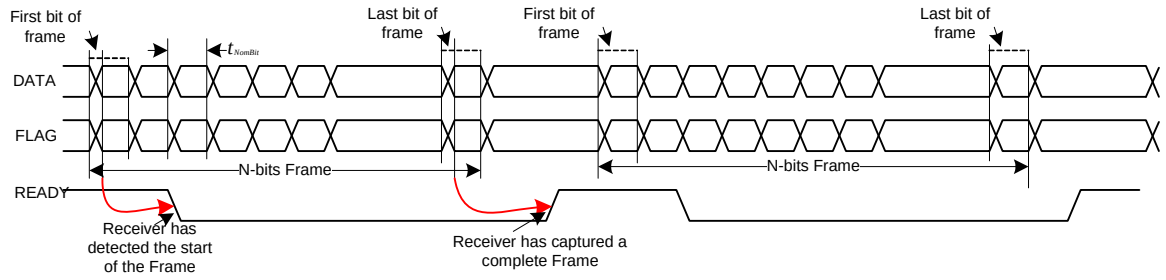


**Figure 81. Receiver Real-Time Data Flow READY Signal Timing**

### 4.11.13.4 Synchronized Data Flow Transmission with Wake

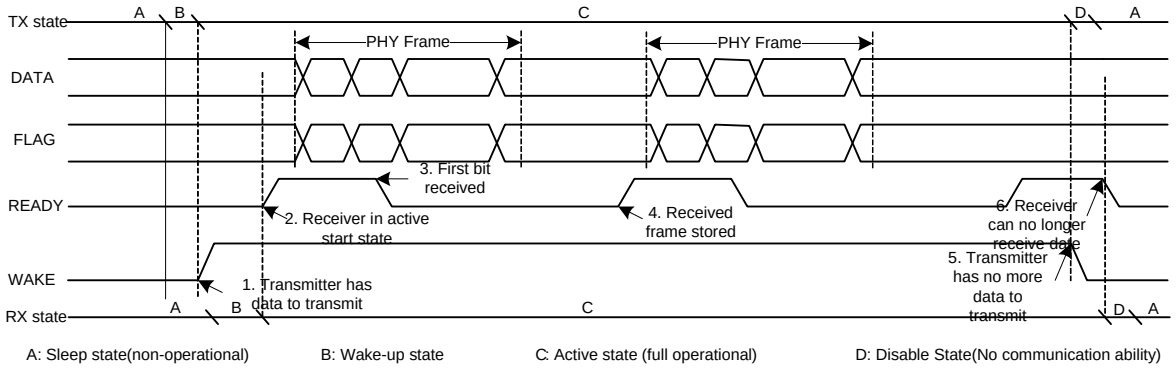


**Figure 82. Synchronized Data Flow Transmission with WAKE**

### 4.11.13.5 Stream Transmission Mode Frame Transfer

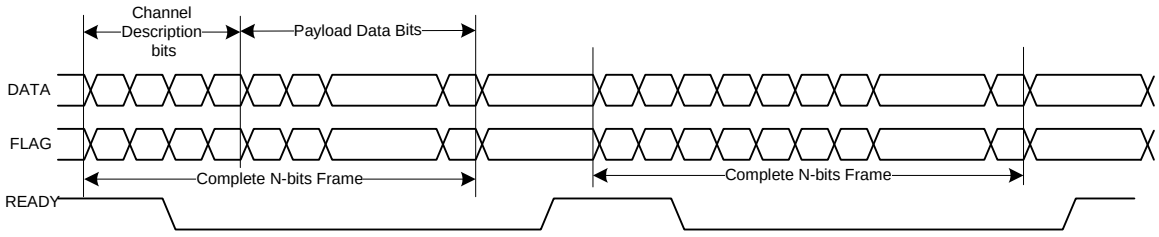


**Figure 83. Stream Transmission Mode Frame Transfer (Synchronized Data Flow)**

**Table 79. MLB 6-Pin Interface Timing Parameters**

| Parameter | Symbol | Min | Max | Unit | Comment |
|---|---|---|---|---|---|
| Cycle-to-cycle system jitter | $t_{jitter}$ | — | 600 | ps | — |
| Transmitter MLB_SIG_P/_N (MLB_DATA_P/_N) output valid from transition of MLB_CLK_P/_N (low-to-high)[1] | $t_{delay}$ | 0.6 | 1.3 | ns | — |
| Disable turnaround time from transition of MLB_CLK_P/_N (low-to-high) | $t_{phz}$ | 0.6 | 3.5 | ns | — |
| Enable turnaround time from transition of MLB_CLK_P/_N (low-to-high) | $t_{plz}$ | 0.6 | 5.6 | ns | — |
| MLB_SIG_P/_N (MLB_DATA_P/_N) valid to transition of MLB_CLK_P/_N (low-to-high) | $t_{su}$ | 0.05 | — | ns | — |
| MLB_SIG_P/_N (MLB_DATA_P/_N) hold from transition of MLB_CLK_P/_N (low-to-high)[2] | $t_{hd}$ | 0.6 | — | ns | — |

1 $t_{delay}$, $t_{phz}$, $t_{plz}$, $t_{su}$, and $t_{hd}$ may also be referenced from a low-to-high transition of the recovered clock for 2:1 and 4:1 recovered-to-external clock ratios.

2 The transmitting device must ensure valid data on MLB_SIG_P/_N (MLB_DATA_P/_N) for at least $t_{hd(min)}$ following the rising edge of MLBCP/N; receivers must latch MLB_SIG_P/_N (MLB_DATA_P/_N) data within $t_{hd(min)}$ of the rising edge of MLB_CLK_P/_N.

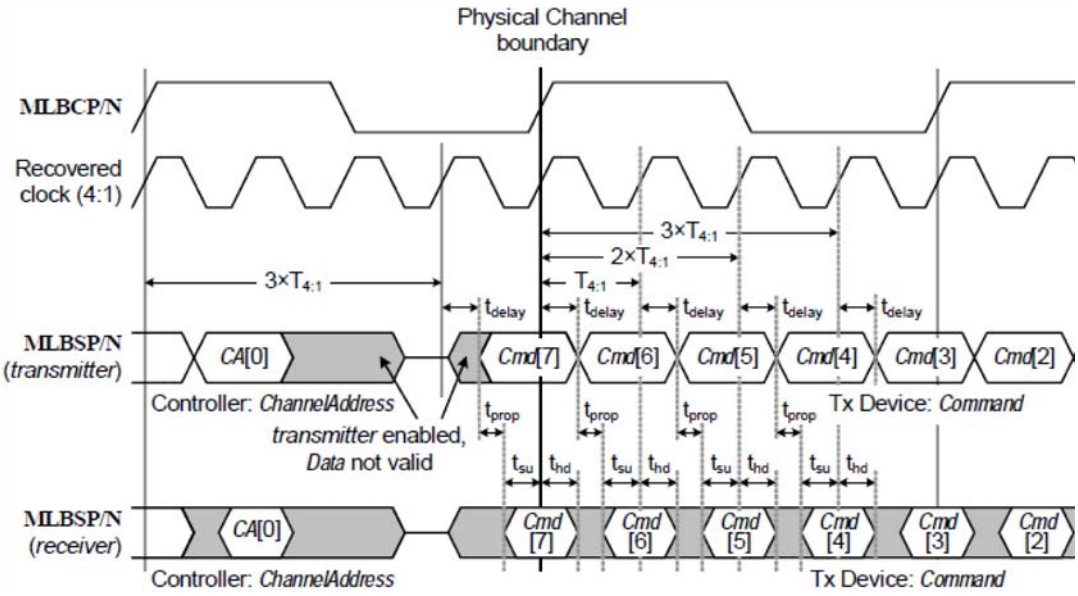


**Figure 88. MLB 6-Pin Delay, Setup, and Hold Times**

## 4.11.15 PCIe PHY Parameters

The PCIe interface complies with PCIe specification Gen2 x1 lane and supports the PCI Express 1.1/2.0 standard.

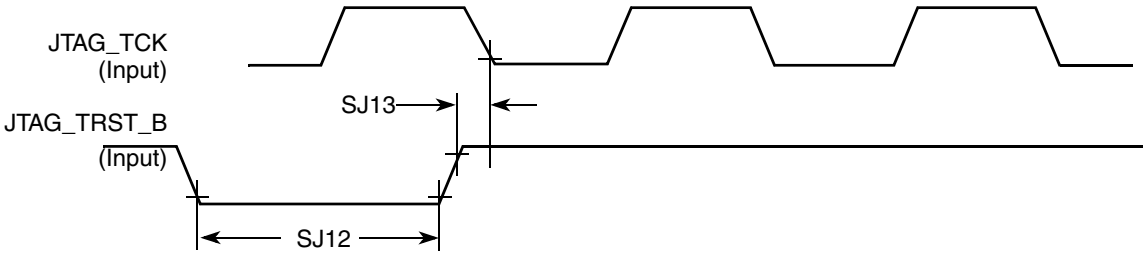


**Figure 93. JTAG_TRST_B Timing Diagram**

**Table 83. JTAG Timing**

| ID | Parameter[1,2] | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| SJ0 | JTAG_TCK frequency of operation $1/(3xT_{DC})$[1] | 0.001 | 22 | MHz |
| SJ1 | JTAG_TCK cycle time in crystal mode | 45 | — | ns |
| SJ2 | JTAG_TCK clock pulse width measured at $V_M$[2] | 22.5 | — | ns |
| SJ3 | JTAG_TCK rise and fall times | — | 3 | ns |
| SJ4 | Boundary scan input data set-up time | 5 | — | ns |
| SJ5 | Boundary scan input data hold time | 24 | — | ns |
| SJ6 | JTAG_TCK low to output data valid | — | 40 | ns |
| SJ7 | JTAG_TCK low to output high impedance | — | 40 | ns |
| SJ8 | JTAG_TMS, JTAG_TDI data set-up time | 5 | — | ns |
| SJ9 | JTAG_TMS, JTAG_TDI data hold time | 25 | — | ns |
| SJ10 | JTAG_TCK low to JTAG_TDO data valid | — | 44 | ns |
| SJ11 | JTAG_TCK low to JTAG_TDO high impedance | — | 44 | ns |
| SJ12 | JTAG_TRST_B assert time | 100 | — | ns |
| SJ13 | JTAG_TRST_B set-up time to JTAG_TCK low | 40 | — | ns |

1 $T_{DC}$ = target frequency of SJC
2 $V_M$ = mid-point voltage

## 4.11.19 SPDIF Timing Parameters

The Sony/Philips Digital Interconnect Format (SPDIF) data is sent using the bi-phase marking code. When encoding, the SPDIF data signal is modulated by a clock that is twice the bit rate of the data signal.

Table 84 and Figure 94 and Figure 95 show SPDIF timing parameters for the Sony/Philips Digital Interconnect Format (SPDIF), including the timing of the modulating Rx clock (SPDIF_SR_CLK) for SPDIF in Rx mode and the timing of the modulating Tx clock (SPDIF_ST_CLK) for SPDIF in Tx mode.

# 5 Boot Mode Configuration

This section provides information on boot mode configuration pins allocation and boot devices interfaces allocation.

## 5.1 Boot Mode Configuration Pins

Table 97 provides boot options, functionality, fuse values, and associated pins. Several input pins are also sampled at reset and can be used to override fuse values, depending on the value of BT_FUSE_SEL fuse. The boot option pins are in effect when BT_FUSE_SEL fuse is '0' (cleared, which is the case for an unblown fuse). For detailed boot mode options configured by the boot mode pins, see the i.MX 6Dual/6Quad Fuse Map document and the System Boot chapter of the i.MX 6Dual/6Quad reference manual (IMX6DQRM).

**Table 97. Fuses and Associated Pins Used for Boot**

| Pin | Direction at Reset | eFuse Name |
|---|---|---|
| **Boot Mode Selection** | | |
| BOOT_MODE1 | Input | Boot Mode Selection |
| BOOT_MODE0 | Input | Boot Mode Selection |
| **Boot Options[1]** | | |
| EIM_DA0 | Input | BOOT_CFG1[0] |
| EIM_DA1 | Input | BOOT_CFG1[1] |
| EIM_DA2 | Input | BOOT_CFG1[2] |
| EIM_DA3 | Input | BOOT_CFG1[3] |
| EIM_DA4 | Input | BOOT_CFG1[4] |
| EIM_DA5 | Input | BOOT_CFG1[5] |
| EIM_DA6 | Input | BOOT_CFG1[6] |
| EIM_DA7 | Input | BOOT_CFG1[7] |
| EIM_DA8 | Input | BOOT_CFG2[0] |
| EIM_DA9 | Input | BOOT_CFG2[1] |
| EIM_DA10 | Input | BOOT_CFG2[2] |
| EIM_DA11 | Input | BOOT_CFG2[3] |
| EIM_DA12 | Input | BOOT_CFG2[4] |
| EIM_DA13 | Input | BOOT_CFG2[5] |
| EIM_DA14 | Input | BOOT_CFG2[6] |
| EIM_DA15 | Input | BOOT_CFG2[7] |
| EIM_A16 | Input | BOOT_CFG3[0] |
| EIM_A17 | Input | BOOT_CFG3[1] |