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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	4 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (1)
SATA	SATA 3Gbps (1)
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-40°C ~ 125°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	624-FBGA, FCBGA
Supplier Device Package	624-FCBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6q6avt10ad

Introduction

The i.MX 6Dual/6Quad processors are specifically useful for applications such as the following:

- Automotive navigation and entertainment
- Graphics rendering for Human Machine Interfaces (HMI)
- High-performance speech processing with large databases
- Audio playback

The i.MX 6Dual/6Quad processors offers numerous advanced features, such as:

- **Multilevel memory system**—The multilevel memory system of each processor is based on the L1 instruction and data caches, L2 cache, and internal and external memory. The processors support many types of external memory devices, including DDR3, low voltage DDR3, LPDDR2, NOR Flash, PSRAM, cellular RAM, NAND Flash (MLC and SLC), OneNAND™, and managed NAND, including eMMC up to rev 4.4/4.41.
- **Smart speed technology**—The processors have power management throughout the device that enables the rich suite of multimedia features and peripherals to consume minimum power in both active and various low power modes. Smart speed technology enables the designer to deliver a feature-rich product, requiring levels of power far lower than industry expectations.
- **Dynamic voltage and frequency scaling**—The processors improve the power efficiency of devices by scaling the voltage and frequency to optimize performance.
- **Multimedia powerhouse**—The multimedia performance of each processor is enhanced by a multilevel cache system, Neon® MPE (Media Processor Engine) co-processor, a multi-standard hardware video codec, 2 autonomous and independent image processing units (IPU), and a programmable smart DMA (SDMA) controller.
- **Powerful graphics acceleration**—Each processor provides three independent, integrated graphics processing units: an OpenGL® ES 2.0 3D graphics accelerator with four shaders (up to 200 MTri/s and OpenCL support), 2D graphics accelerator, and dedicated OpenVG™ 1.1 accelerator.
- **Interface flexibility**—Each processor supports connections to a variety of interfaces: LCD controller for up to four displays (including parallel display, HDMI1.4, MIPI display, and LVDS display), dual CMOS sensor interface (parallel or through MIPI), high-speed USB on-the-go with PHY, high-speed USB host with PHY, multiple expansion card ports (high-speed MMC/SDIO host and other), 10/100/1000 Mbps Gigabit Ethernet controller, and a variety of other popular interfaces (such as UART, I²C, and I²S serial audio, SATA-II, and PCIe-II).
- **Automotive environment support**—Each processor includes interfaces, such as two CAN ports, an MLB150/50 port, an ESAI audio interface, and an asynchronous sample rate converter for multichannel/multisource audio.
- **Advanced security**—The processors deliver hardware-enabled security features that enable secure e-commerce, digital rights management (DRM), information encryption, secure boot, and secure software downloads. The security features are discussed in detail in the i.MX 6Dual/6Quad security reference manual (IMX6DQ6SDLSRM).
- **Integrated power management**—The processors integrate linear regulators and internally generate voltage levels for different domains. This significantly simplifies system power management structure.

1.1 Ordering Information

Table 1 shows examples of orderable part numbers covered by this data sheet. This table does not include all possible orderable part numbers. The latest part numbers are available on freescale.com/imx6series. If your desired part number is not listed in the table, or you have questions about available parts, see freescale.com/imx6series or contact your Freescale representative.

Table 1. Example Orderable Part Numbers

Part Number	Quad/Dual CPU	Options	Speed ¹ Grade	Temperature Grade	Package
MCIMX6Q6AVT10AC	i.MX 6Quad	With VPU, GPU	1 GHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6Q6AVT10AD	i.MX 6Quad	With VPU, GPU	1 GHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6Q4AVT10AC	i.MX 6Quad	With GPU, no VPU	1 GHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6Q4AVT10AD	i.MX 6Quad	With GPU, no VPU	1 GHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6Q6AVT08AC	i.MX 6Quad	With VPU, GPU	852 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6Q6AVT08AD	i.MX 6Quad	With VPU, GPU	852 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6Q4AVT08AC	i.MX 6Quad	With GPU, no VPU	852 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6Q4AVT08AD	i.MX 6Quad	With GPU, no VPU	852 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6D6AVT10AC	i.MX 6Dual	With VPU, GPU	1 GHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6D6AVT10AD	i.MX 6Dual	With VPU, GPU	1 GHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6D4AVT10AC	i.MX 6Dual	With GPU, no VPU	1 GHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6D4AVT10AD	i.MX 6Dual	With GPU, no VPU	1 GHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6D6AVT08AC	i.MX 6Dual	With VPU, GPU	852 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6D6AVT08AD	i.MX 6Dual	With VPU, GPU	852 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6D4AVT08AC	i.MX 6Dual	With GPU, no VPU	852 MHz	Automotive ¹	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6D4AVT08AD	i.MX 6Dual	With GPU, no VPU	852 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)

¹ If a 24 MHz input clock is used (required for USB), the maximum SoC speed is limited to 996 MHz.

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
EPIT-1 EPIT-2	Enhanced Periodic Interrupt Timer	Timer Peripherals	Each EPIT is a 32-bit “set and forget” timer that starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler for division of input clock frequency to get the required time setting for the interrupts to occur, and counter value can be programmed on the fly.
ESAI	Enhanced Serial Audio Interface	Connectivity Peripherals	The Enhanced Serial Audio Interface (ESAI) provides a full-duplex serial port for serial communication with a variety of serial devices, including industry-standard codecs, SPDIF transceivers, and other processors. The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. All serial transfers are synchronized to a clock. Additional synchronization signals are used to delineate the word frames. The normal mode of operation is used to transfer data at a periodic rate, one word per period. The network mode is also intended for periodic transfers; however, it supports up to 32 words (time slots) per period. This mode can be used to build time division multiplexed (TDM) networks. In contrast, the on-demand mode is intended for non-periodic transfers of data and to transfer data serially at high speed when the data becomes available. The ESAI has 12 pins for data and clocking connection to external devices.
FlexCAN-1 FlexCAN-2	Flexible Controller Area Network	Connectivity Peripherals	The CAN protocol was primarily, but not only, designed to be used as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the Electromagnetic interference (EMI) environment of a vehicle, cost-effectiveness and required bandwidth. The FlexCAN module is a full implementation of the CAN protocol specification, Version 2.0 B, which supports both standard and extended message frames.
GPIO-1 GPIO-2 GPIO-3 GPIO-4 GPIO-5 GPIO-6 GPIO-7	General Purpose I/O Modules	System Control Peripherals	Used for general purpose input/output to external devices. Each GPIO module supports 32 bits of I/O.
GPMI	General Purpose Media Interface	Connectivity Peripherals	The GPMI module supports up to 8x NAND devices. 40-bit ECC encryption/decryption for NAND Flash controller (GPMI2). The GPMI supports separate DMA channels per NAND device.
GPT	General Purpose Timer	Timer Peripherals	Each GPT is a 32-bit “free-running” or “set and forget” mode timer with programmable prescaler and compare and capture register. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in “set and forget” mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
uSDHC-1 uSDHC-2 uSDHC-2 uSDHC-4	SD/MMC and SDXC Enhanced Multi-Media Card / Secure Digital Host Controller	Connectivity Peripherals	<p>i.MX 6Dual/6Quad specific SoC characteristics: All four MMC/SD/SDIO controller IPs are identical and are based on the uSDHC IP. They are:</p> <ul style="list-style-type: none"> • Conforms to the SD Host Controller Standard Specification version 3.0 • Fully compliant with MMC command/response sets and Physical Layer as defined in the Multimedia Card System Specification, v4.2/4.3/4.4/4.41 including high-capacity (size > 2 GB) cards HC MMC. Hardware reset as specified for eMMC cards is supported at ports #3 and #4 only. • Fully compliant with SD command/response sets and Physical Layer as defined in the SD Memory Card Specifications, v3.0 including high-capacity SDHC cards up to 32 GB and SDXC cards up to 2TB. • Fully compliant with SDIO command/response sets and interrupt/read-wait mode as defined in the SDIO Card Specification, Part E1, v1.10 • Fully compliant with SD Card Specification, Part A2, SD Host Controller Standard Specification, v2.00 <p>All four ports support:</p> <ul style="list-style-type: none"> • 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR104 mode (104 MB/s max) • 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max) <p>However, the SoC-level integration and I/O muxing logic restrict the functionality to the following:</p> <ul style="list-style-type: none"> • Instances #1 and #2 are primarily intended to serve as external slots or interfaces to on-board SDIO devices. These ports are equipped with “Card Detection” and “Write Protection” pads and do not support hardware reset. • Instances #3 and #4 are primarily intended to serve interfaces to embedded MMC memory or interfaces to on-board SDIO devices. These ports do not have “Card detection” and “Write Protection” pads and do support hardware reset. • All ports can work with 1.8 V and 3.3 V cards. There are two completely independent I/O power domains for Ports #1 and #2 in four bit configuration (SD interface). Port #3 is placed in his own independent power domain and port #4 shares power domain with some other interfaces.
VDOA	VDOA	Multimedia Peripherals	The Video Data Order Adapter (VDOA) is used to re-order video data from the “tiled” order used by the VPU to the conventional raster-scan order needed by the IPU.
VPU	Video Processing Unit	Multimedia Peripherals	A high-performing video processing unit (VPU), which covers many SD-level and HD-level video decoders and SD-level encoders as a multi-standard video codec engine as well as several important video processing, such as rotation and mirroring. See the i.MX 6Dual/6Quad reference manual (IMX6DQRM) for complete list of VPU’s decoding/encoding capabilities.
WDOG-1	Watchdog	Timer Peripherals	The Watchdog Timer supports two comparison points during each counting period. Each of the comparison points is configurable to evoke an interrupt to the ARM core, and a second point evokes an external event on the WDOG line.

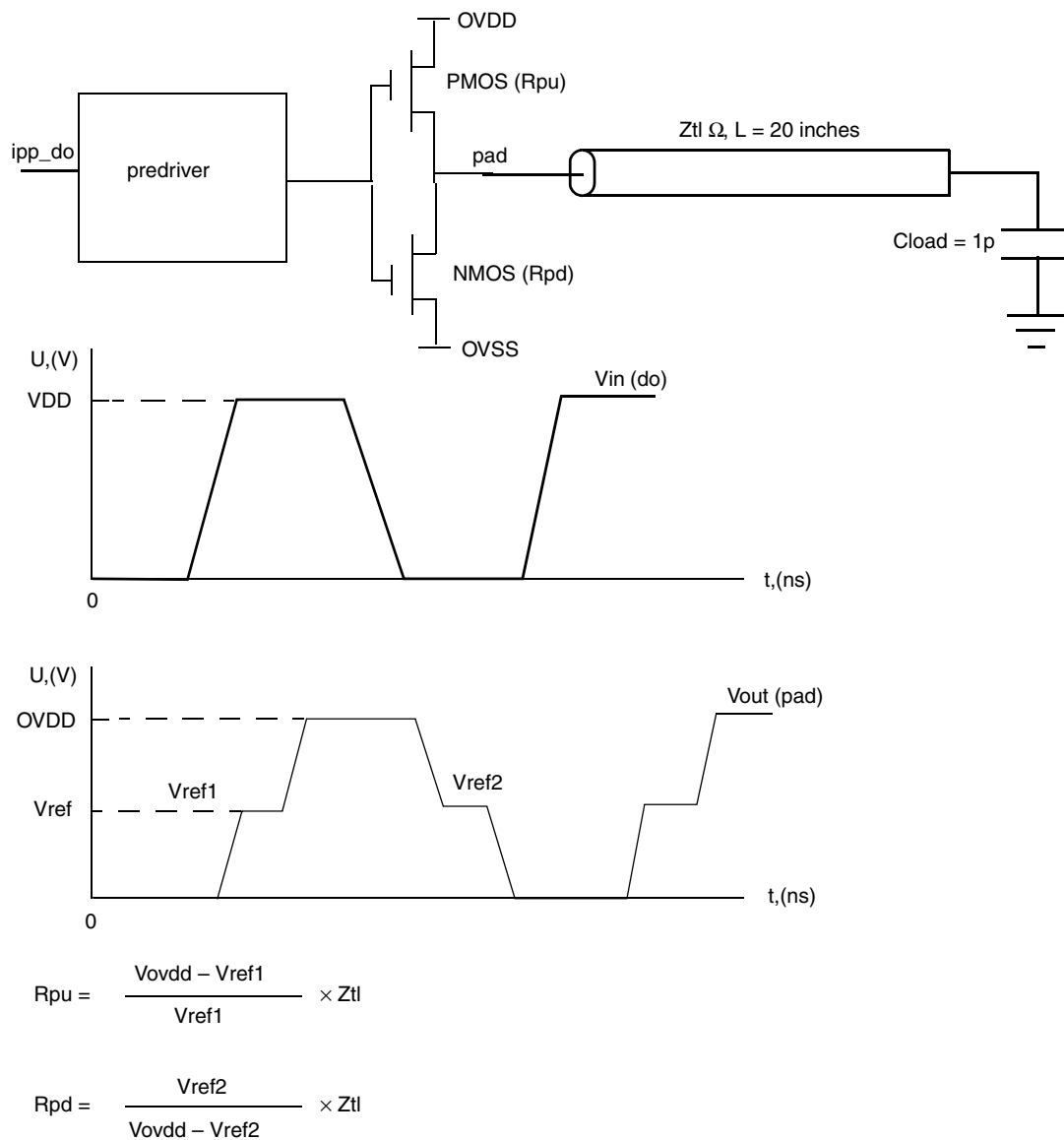


Figure 9. Impedance Matching Load for Measurement

Electrical Characteristics

⁴ Refer to JEDEC DDR3 SDRAM Standards for Data Setup (tDS), Hold (tDH) and Slew Rate Derating tables.

Figure 26 shows the DDR3/DDR3L read timing diagram. The timing parameters for this diagram appear in Table 44.

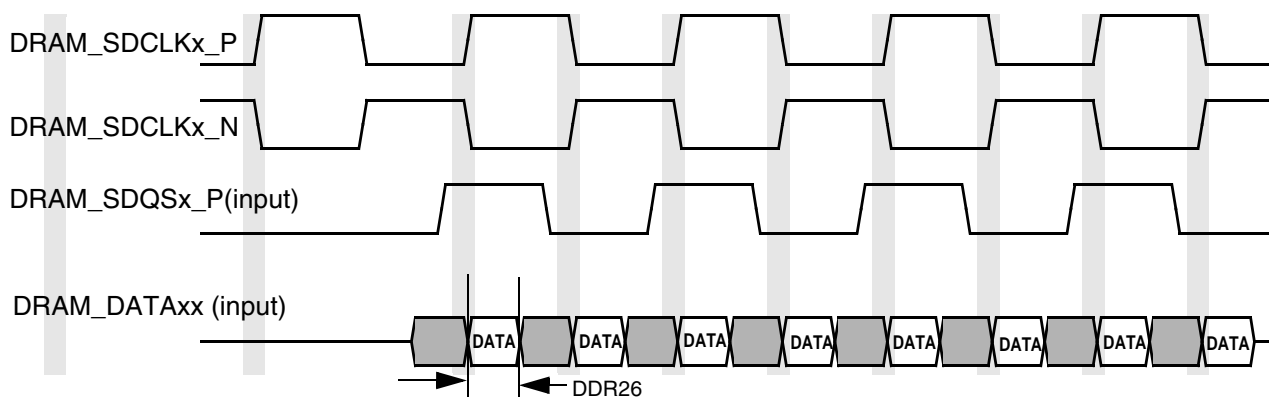


Figure 26. DDR3/DDR3L Read Cycle

4.9.4.2 LPDDR2 Parameters

Table 44. DDR3/DDR3L Read Cycle

ID	Parameter ^{1,2,3}	Symbol	CK = 532 MHz		Unit
			Min	Max	
DDR26	Minimum required DRAM_DATAxx valid window width.	—	450	—	ps

¹ To receive the reported setup and hold values, the read calibration must be performed to locate the DRAM_SDQSx_P in the middle of DRAM_DATAxx window.

² All measurements are in reference to Vref level.

³ Measurements were completed using balanced load and a 25 Ω resistor from outputs to DRAM_VREF.

Figure 27 shows the LPDDR2 basic timing diagram. The timing parameters for this diagram appear in Table 45.

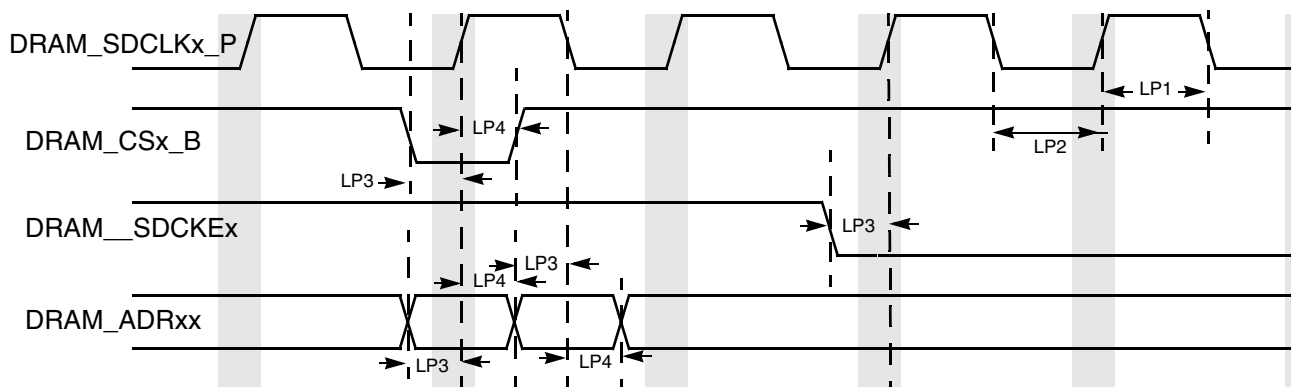


Figure 27. LPDDR2 Command and Address Timing Diagram

4.10.2 Source Synchronous Mode AC Timing (ONFI 2.x Compatible)

Figure 35 shows the write and read timing of Source Synchronous mode.

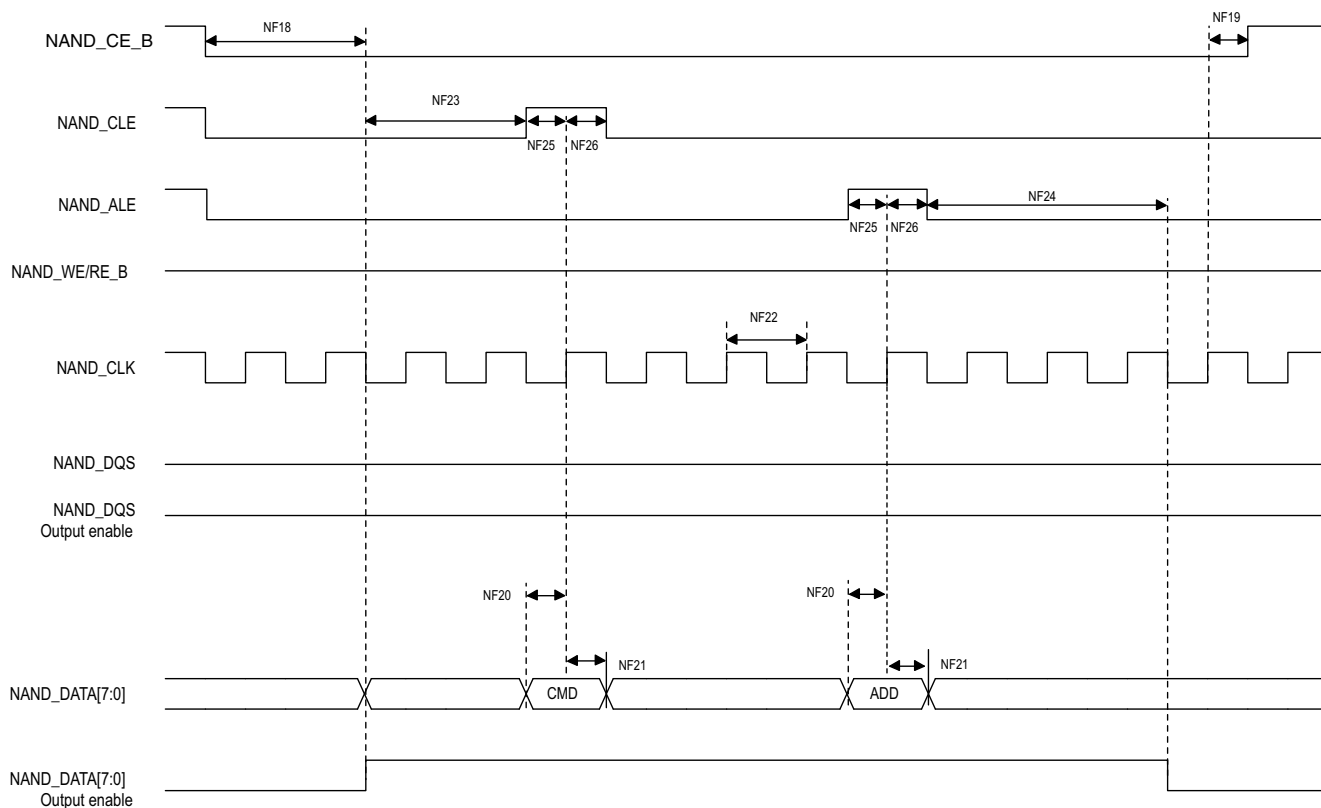
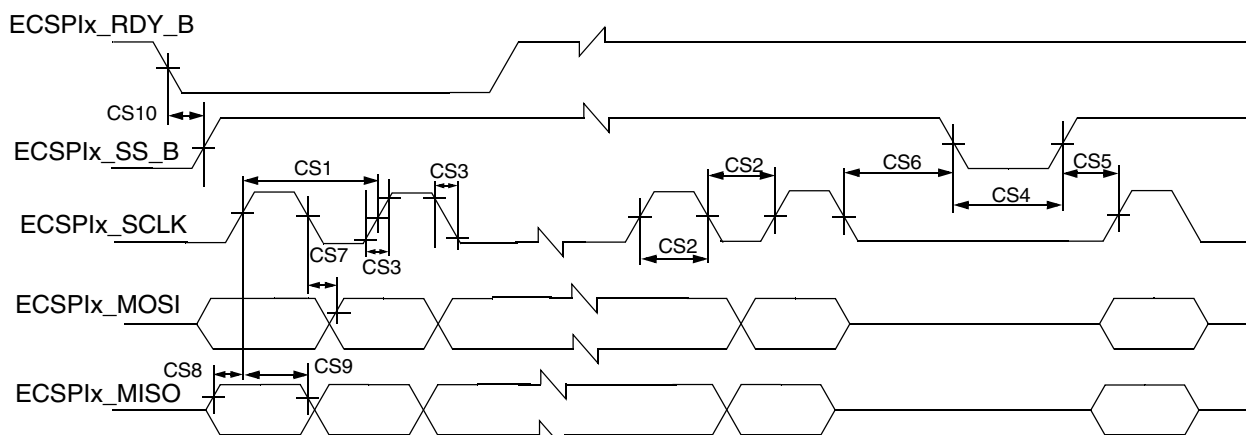


Figure 35. Source Synchronous Mode Command and Address Timing Diagram

4.11.2.1 ECSPi Master Mode Timing

Figure 41 depicts the timing of ECSPi in master mode and Table 51 lists the ECSPi master mode timing characteristics.



Note: ECSPi_MOSI is always driven (not tri-stated) between actual data transmissions. This limits the ECSPi to be connected between a single master and a single slave.

Figure 41. ECSPi Master Mode Timing Diagram

Table 51. ECSPi Master Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit	
CS1	ECSPi_SCLK Cycle Time–Read	t_{clk}	55	—	ns	
	• Slow group ¹		40			
	• Fast group ²		15			
CS2	ECSPi_SCLK High or Low Time–Read	t_{sw}	26	—	ns	
	• Slow group ¹		20			
	• Fast group ²		7			
CS3	ECSPi_SCLK Rise or Fall ³	$t_{RISE/FALL}$	—	—	ns	
CS4	ECSPi_SSx pulse width	t_{CSLH}	Half ECSPi_SCLK period	—	ns	
CS5	ECSPi_SSx Lead Time (CS setup time)	t_{SCS}	Half ECSPi_SCLK period - 4	—	ns	
CS6	ECSPi_SSx Lag Time (CS hold time)	t_{HCS}	Half ECSPi_SCLK period - 2	—	ns	
CS7	ECSPi_MOSI Propagation Delay ($C_{LOAD} = 20 \text{ pF}$)	t_{PDmosi}	-1	1	ns	
CS8	ECSPi_MISO Setup Time	t_{Smiso}	21.5	—	ns	
			• Slow group ¹			16
			• Fast group ²			
CS9	ECSPi_MISO Hold Time	t_{Hmiso}	0	—	ns	
CS10	ECSPi_RDY to ECSPi_SSx Time ⁴	t_{SDRY}	5	—	ns	

¹ ECSPi slow includes:

ECSPi1/DISP0_DAT22, ECSPi1/KEY_COL1, ECSPi1/CSI0_DAT6, ECSPi2/EIM_OE, ECSPi2/ ECSPi2/CSI0_DAT10, ECSPi3/DISP0_DAT2

² ECSPi fast includes:

ECSPi1/EIM_D17, ECSPi4/EIM_D22, ECSPi5/SD2_DAT0, ECSPi5/SD1_DAT0

³ See specific I/O AC parameters Section 4.7, “I/O AC Parameters.”

⁴ ECSPi_RDY is sampled internally by ipg_clk and is asynchronous to all other CSPI signals.

Table 59. MII Asynchronous Inputs Signal Timing

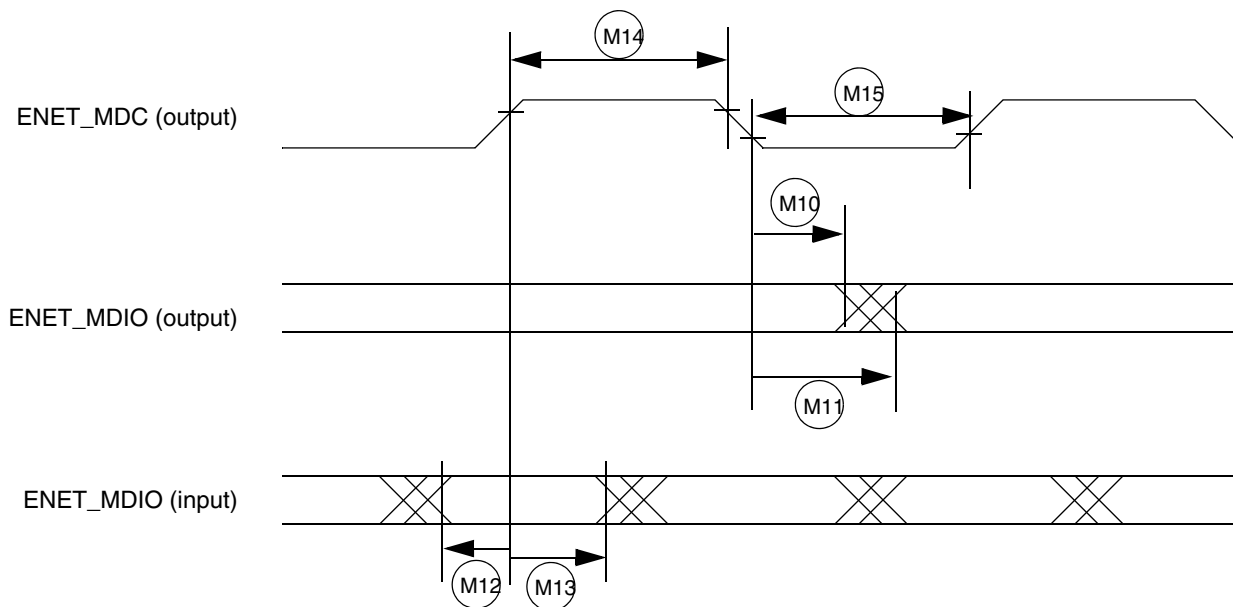
ID	Characteristic	Min	Max	Unit
M9 ¹	ENET_CRS to ENET_COL minimum pulse width	1.5	—	ENET_TX_CLK period

¹ ENET_COL has the same timing in 10-Mbit 7-wire interface mode.

4.11.5.1.4 MII Serial Management Channel Timing (ENET_MDIO and ENET_MDC)

The MDC frequency is designed to be equal to or less than 2.5 MHz to be compatible with the IEEE 802.3 MII specification. However the ENET can function correctly with a maximum MDC frequency of 15 MHz.

Figure 51 shows MII asynchronous input timings. Table 60 describes the timing parameters (M10–M15) shown in the figure.


Figure 51. MII Serial Management Channel Timing Diagram
Table 60. MII Serial Management Channel Timing

ID	Characteristic	Min	Max	Unit
M10	ENET_MDC falling edge to ENET_MDIO output invalid (minimum propagation delay)	0	—	ns
M11	ENET_MDC falling edge to ENET_MDIO output valid (maximum propagation delay)	—	5	ns
M12	ENET_MDIO (input) to ENET_MDC rising edge setup	18	—	ns
M13	ENET_MDIO (input) to ENET_MDC rising edge hold	0	—	ns
M14	ENET_MDC pulse width high	40%	60%	ENET_MDC period
M15	ENET_MDC pulse width low	40%	60%	ENET_MDC period

Power-up time for the HDMI 3D Tx PHY while operating with the fastest input reference clock supported (340 MHz) is 133 μ s.

4.11.7.2 Electrical Characteristics

The table below provides electrical characteristics for the HDMI 3D Tx PHY. The following three figures illustrate various definitions and measurement conditions specified in the table below.

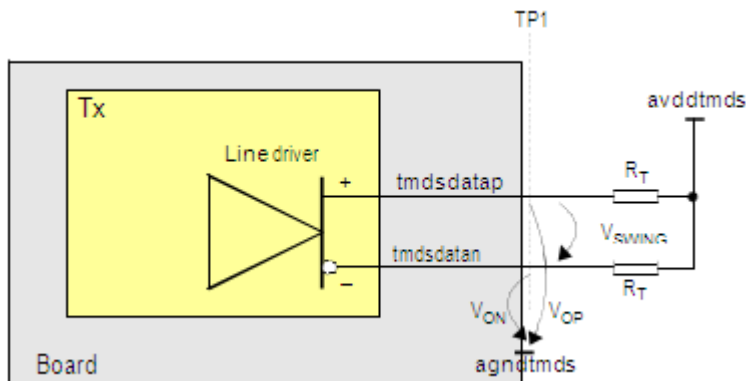


Figure 56. Driver Measuring Conditions

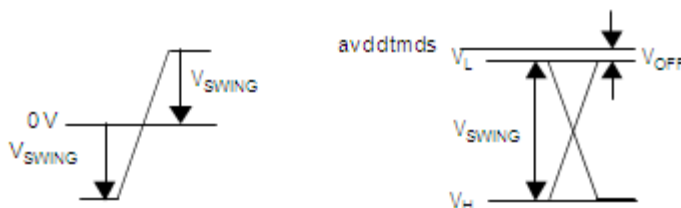


Figure 57. Driver Definitions

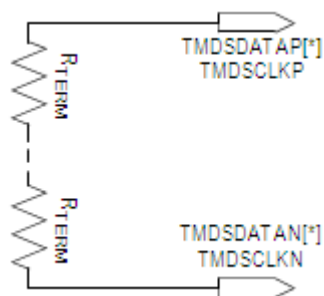


Figure 58. Source Termination

Table 63. Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Operating conditions for HDMI						
avddtmds	Termination supply voltage	—	3.15	3.3	3.45	V

4.11.12.9 Low-Power Receiver Timing

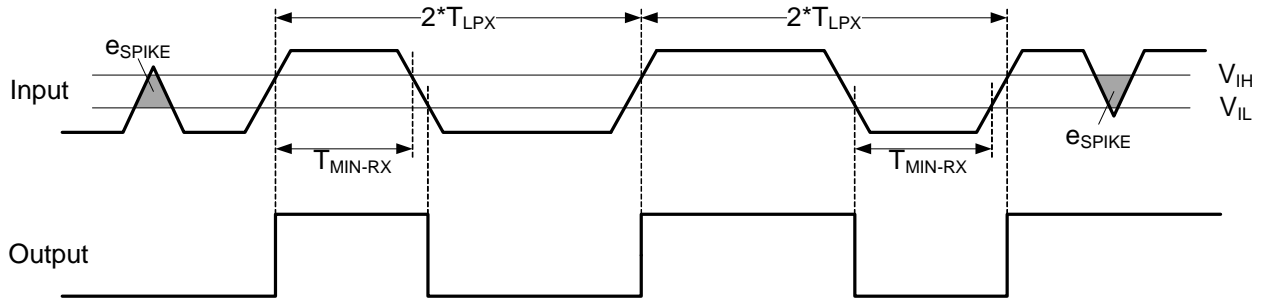


Figure 78. Input Glitch Rejection of Low-Power Receivers

4.11.13 HSI Host Controller Timing Parameters

This section describes the timing parameters of the HSI Host Controller which are compliant with High-Speed Synchronous Serial Interface (HSI) Physical Layer specification version 1.01.

4.11.13.1 Synchronous Data Flow

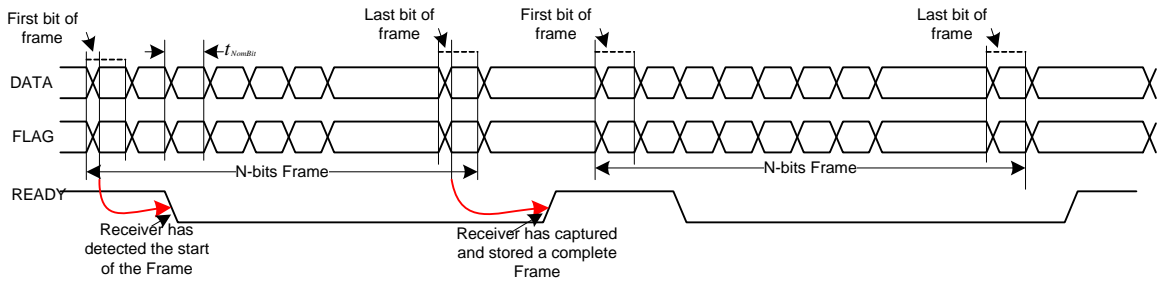


Figure 79. Synchronized Data Flow READY Signal Timing (Frame and Stream Transmission)

4.11.13.2 Pipelined Data Flow

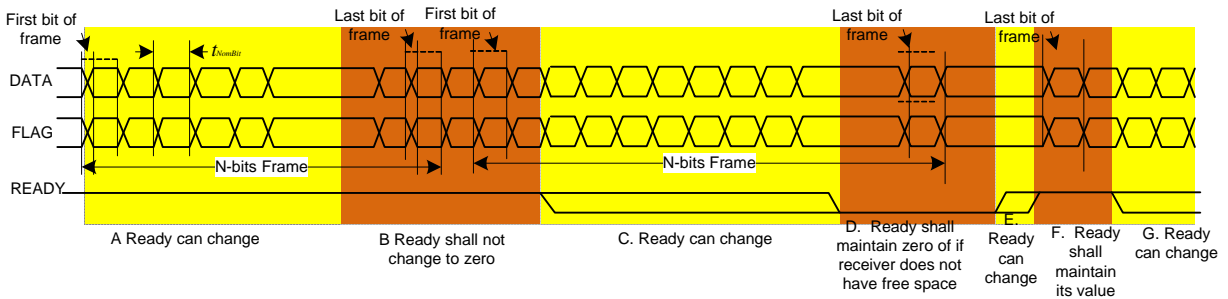


Figure 80. Pipelined Data Flow READY Signal Timing (Frame Transmission Mode)

4.11.13.6 Frame Transmission Mode (Synchronized Data Flow)

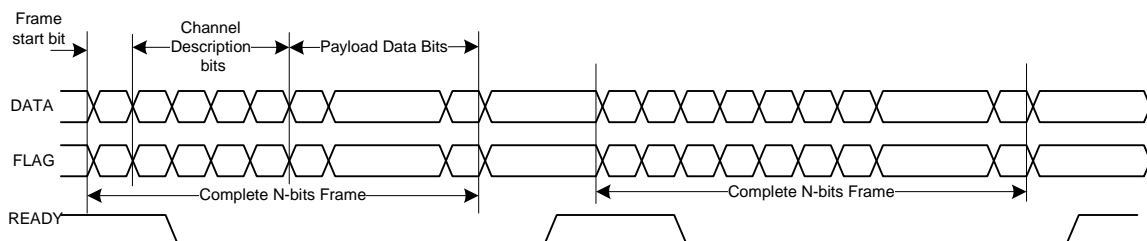


Figure 84. Frame Transmission Mode Transfer of Two Frames (Synchronized Data Flow)

4.11.13.7 Frame Transmission Mode (Pipelined Data Flow)

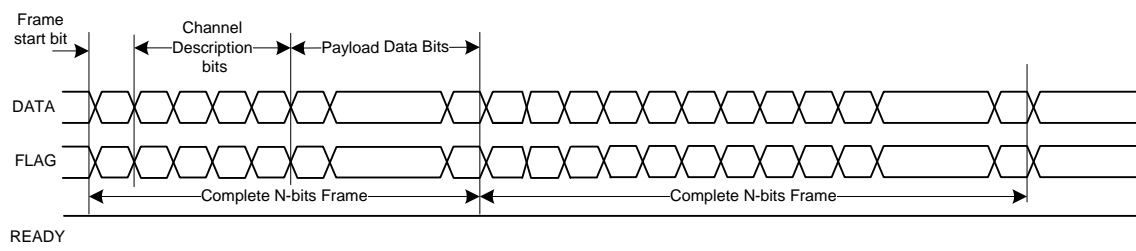


Figure 85. Frame Transmission Mode Transfer of Two Frames (Pipelined Data Flow)

4.11.13.8 DATA and FLAG Signal Timing Requirement for a 15 pF Load

Table 74. DATA and FLAG Timing

Parameter	Description	1 Mbit/s	100 Mbit/s
$t_{Bit, nom}$	Nominal bit time	1000 ns	10 ns
$t_{Rise, min}$ and $t_{Fall, min}$	Minimum allowed rise and fall time	2 ns	2 ns
$t_{TxToRxSkew, maxfq}$	Maximum skew between transmitter and receiver package pins	50 ns	0.5 ns
$t_{EageSepTx, min}$	Minimum allowed separation of signal transitions at transmitter package pins, including all timing defects, for example, jitter and skew, inside the transmitter.	400 ns	4 ns
$t_{EageSepRx, min}$	Minimum separation of signal transitions, measured at the receiver package pins, including all timing defects, for example, jitter and skew, inside the receiver.	350 ns	3.5 ns

Table 84. SPDIF Timing Parameters

Parameter	Symbol	Timing Parameter Range		Unit
		Min	Max	
SPDIF_IN Skew: asynchronous inputs, no specs apply	—	—	0.7	ns
SPDIF_OUT output (Load = 50pf)				
• Skew	—	—	1.5	ns
• Transition rising	—	—	24.2	
• Transition falling	—	—	31.3	
SPDIF_OUT output (Load = 30pf)				
• Skew	—	—	1.5	ns
• Transition rising	—	—	13.6	
• Transition falling	—	—	18.0	
Modulating Rx clock (SPDIF_SR_CLK) period	srckp	40.0	—	ns
SPDIF_SR_CLK high period	srckph	16.0	—	ns
SPDIF_SR_CLK low period	srckpl	16.0	—	ns
Modulating Tx clock (SPDIF_ST_CLK) period	stckp	40.0	—	ns
SPDIF_ST_CLK high period	stckph	16.0	—	ns
SPDIF_ST_CLK low period	stckpl	16.0	—	ns

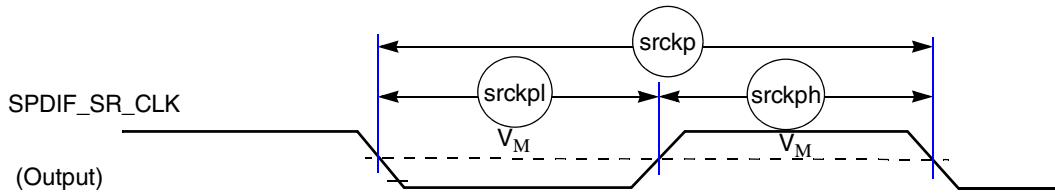


Figure 94. SPDIF_SR_CLK Timing Diagram

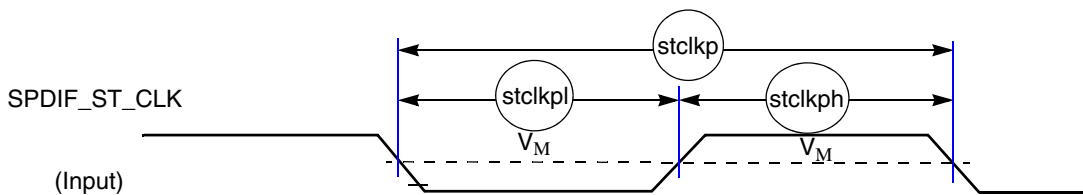


Figure 95. SPDIF_ST_CLK Timing Diagram

4.11.21 UART I/O Configuration and Timing Parameters

4.11.21.1 UART RS-232 I/O Configuration in Different Modes

The i.MX 6Dual/6Quad UART interfaces can serve both as DTE or DCE device. This can be configured by the DCEDTE control bit (default 0 – DCE mode). [Table 90](#) shows the UART I/O configuration based on the enabled mode.

Table 90. UART I/O Configuration vs. Mode

Port	DTE Mode		DCE Mode	
	Direction	Description	Direction	Description
UARTx_RTS_B	Output	RTS from DTE to DCE	Input	RTS from DTE to DCE
UARTx_CTS_B	Input	CTS from DCE to DTE	Output	CTS from DCE to DTE
UARTx_DTR_B	Output	DTR from DTE to DCE	Input	DTR from DTE to DCE
UARTx_DSR_B	Input	DSR from DCE to DTE	Output	DSR from DCE to DTE
UARTx_DCD_B	Input	DCD from DCE to DTE	Output	DCD from DCE to DTE
UARTx_RI_B	Input	RING from DCE to DTE	Output	RING from DCE to DTE
UARTx_TX_DATA	Input	Serial data from DCE to DTE	Output	Serial data from DCE to DTE
UARTx_RX_DATA	Output	Serial data from DTE to DCE	Input	Serial data from DTE to DCE

Table 97. Fuses and Associated Pins Used for Boot (continued)

Pin	Direction at Reset	eFuse Name
EIM_A18	Input	BOOT_CFG3[2]
EIM_A19	Input	BOOT_CFG3[3]
EIM_A20	Input	BOOT_CFG3[4]
EIM_A21	Input	BOOT_CFG3[5]
EIM_A22	Input	BOOT_CFG3[6]
EIM_A23	Input	BOOT_CFG3[7]
EIM_A24	Input	BOOT_CFG4[0]
EIM_WAIT	Input	BOOT_CFG4[1]
EIM_LBA	Input	BOOT_CFG4[2]
EIM_EB0	Input	BOOT_CFG4[3]
EIM_EB1	Input	BOOT_CFG4[4]
EIM_RW	Input	BOOT_CFG4[5]
EIM_EB2	Input	BOOT_CFG4[6]
EIM_EB3	Input	BOOT_CFG4[7]

¹ Pin value overrides fuse settings for BT_FUSE_SEL = '0'. Signal Configuration as Fuse Override Input at Power Up. These are special I/O lines that control the boot up configuration during product development. In production, the boot configuration can be controlled by fuses.

5.2 Boot Devices Interfaces Allocation

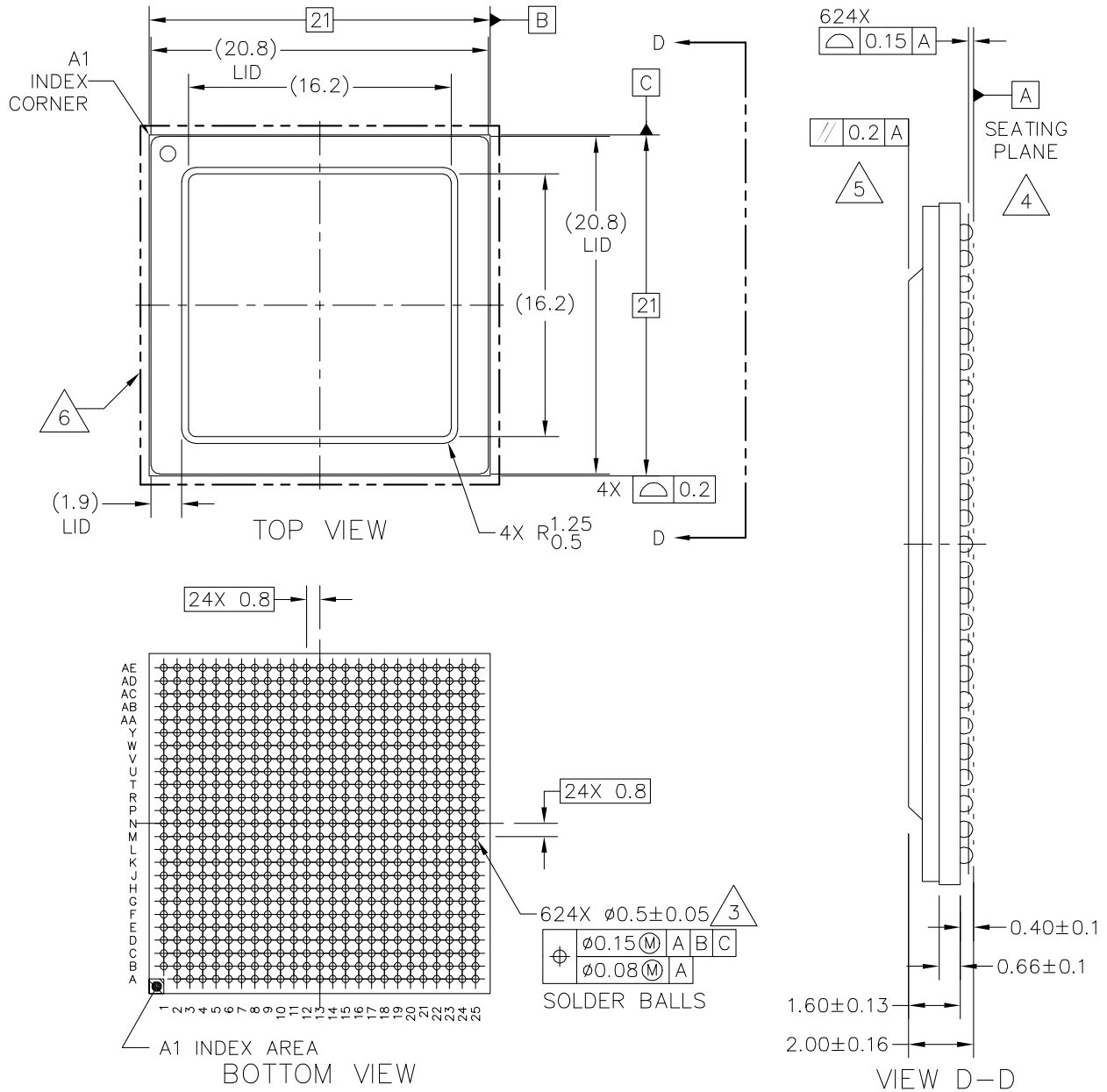
Table 98 lists the interfaces that can be used by the boot process in accordance with the specific boot mode configuration. The table also describes the interface's specific modes and IOMUXC allocation, which are configured during boot when appropriate.

Table 98. Interfaces Allocation During Boot

Interface	IP Instance	Allocated Pads During Boot	Comment
SPI	ECSPI-1	EIM_D17, EIM_D18, EIM_D16, EIM_EB2, EIM_D19, EIM_D24, EIM_D25	—
SPI	ECSPI-2	CSI0_DAT10, CSI0_DAT9, CSI0_DAT8, CSI0_DAT11, EIM_LBA, EIM_D24, EIM_D25	—
SPI	ECSPI-3	DISP0_DAT2, DISP0_DAT1, DISP0_DAT0, DISP0_DAT3, DISP0_DAT4, DISP0_DAT5, DISP0_DAT6	—
SPI	ECSPI-4	EIM_D22, EIM_D28, EIM_D21, EIM_D20, EIM_A25, EIM_D24, EIM_D25	—
SPI	ECSPI-5	SD1_DAT0, SD1_CMD, SD1_CLK, SD1_DAT1, SD1_DAT2, SD1_DAT3, SD2_DAT3	—
EIM	EIM	EIM_DA[15:0], EIM_D[31:16], CSI0_DAT[19:4], CSI0_DATA_EN, CSI0_VSYNC	Used for NOR, OneNAND boot Only CS0 is supported

6.2.1.1 21 x 21 mm Lidded Package

Figure 107 shows the top, bottom, and side views of the 21 × 21 mm lidded package.



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TITLE: 624 I/O FC PBGA, 21 X 21 X 2 PKG, 0.8 MM PITCH, STAMPED LID	DOCUMENT NO: 98ASA00330D STANDARD: NON-JEDEC	REV: D 08 OCT 2013

Figure 106. 21 x 21 mm Lidded Package Top, Bottom, and Side Views (Sheet 1 of 2)

Table 100. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition ¹			
				Default Mode (Reset Mode)	Default Function (Signal Name)	Input/Output	Value ²
DISP0_DAT18	V25	NVCC_LCD	GPIO	ALT5	GPIO5_IO12	Input	PU (100K)
DISP0_DAT19	U23	NVCC_LCD	GPIO	ALT5	GPIO5_IO13	Input	PU (100K)
DISP0_DAT2	P23	NVCC_LCD	GPIO	ALT5	GPIO4_IO23	Input	PU (100K)
DISP0_DAT20	U22	NVCC_LCD	GPIO	ALT5	GPIO5_IO14	Input	PU (100K)
DISP0_DAT21	T20	NVCC_LCD	GPIO	ALT5	GPIO5_IO15	Input	PU (100K)
DISP0_DAT22	V24	NVCC_LCD	GPIO	ALT5	GPIO5_IO16	Input	PU (100K)
DISP0_DAT23	W24	NVCC_LCD	GPIO	ALT5	GPIO5_IO17	Input	PU (100K)
DISP0_DAT3	P21	NVCC_LCD	GPIO	ALT5	GPIO4_IO24	Input	PU (100K)
DISP0_DAT4	P20	NVCC_LCD	GPIO	ALT5	GPIO4_IO25	Input	PU (100K)
DISP0_DAT5	R25	NVCC_LCD	GPIO	ALT5	GPIO4_IO26	Input	PU (100K)
DISP0_DAT6	R23	NVCC_LCD	GPIO	ALT5	GPIO4_IO27	Input	PU (100K)
DISP0_DAT7	R24	NVCC_LCD	GPIO	ALT5	GPIO4_IO28	Input	PU (100K)
DISP0_DAT8	R22	NVCC_LCD	GPIO	ALT5	GPIO4_IO29	Input	PU (100K)
DISP0_DAT9	T25	NVCC_LCD	GPIO	ALT5	GPIO4_IO30	Input	PU (100K)
DRAM_A0	AC14	NVCC_DRAM	DDR	ALT0	DRAM_ADDR00	Output	0
DRAM_A1	AB14	NVCC_DRAM	DDR	ALT0	DRAM_ADDR01	Output	0
DRAM_A10	AA15	NVCC_DRAM	DDR	ALT0	DRAM_ADDR10	Output	0
DRAM_A11	AC12	NVCC_DRAM	DDR	ALT0	DRAM_ADDR11	Output	0
DRAM_A12	AD12	NVCC_DRAM	DDR	ALT0	DRAM_ADDR12	Output	0
DRAM_A13	AC17	NVCC_DRAM	DDR	ALT0	DRAM_ADDR13	Output	0
DRAM_A14	AA12	NVCC_DRAM	DDR	ALT0	DRAM_ADDR14	Output	0
DRAM_A15	Y12	NVCC_DRAM	DDR	ALT0	DRAM_ADDR15	Output	0
DRAM_A2	AA14	NVCC_DRAM	DDR	ALT0	DRAM_ADDR02	Output	0
DRAM_A3	Y14	NVCC_DRAM	DDR	ALT0	DRAM_ADDR03	Output	0
DRAM_A4	W14	NVCC_DRAM	DDR	ALT0	DRAM_ADDR04	Output	0
DRAM_A5	AE13	NVCC_DRAM	DDR	ALT0	DRAM_ADDR05	Output	0
DRAM_A6	AC13	NVCC_DRAM	DDR	ALT0	DRAM_ADDR06	Output	0
DRAM_A7	Y13	NVCC_DRAM	DDR	ALT0	DRAM_ADDR07	Output	0
DRAM_A8	AB13	NVCC_DRAM	DDR	ALT0	DRAM_ADDR08	Output	0
DRAM_A9	AE12	NVCC_DRAM	DDR	ALT0	DRAM_ADDR09	Output	0
DRAM_CAS	AE16	NVCC_DRAM	DDR	ALT0	DRAM_CAS_B	Output	0
DRAM_CS0	Y16	NVCC_DRAM	DDR	ALT0	DRAM_CS0_B	Output	0
DRAM_CS1	AD17	NVCC_DRAM	DDR	ALT0	DRAM_CS1_B	Output	0
DRAM_D0	AD2	NVCC_DRAM	DDR	ALT0	DRAM_DATA00	Input	PU (100K)
DRAM_D1	AE2	NVCC_DRAM	DDR	ALT0	DRAM_DATA01	Input	PU (100K)
DRAM_D10	AA6	NVCC_DRAM	DDR	ALT0	DRAM_DATA10	Input	PU (100K)

Table 100. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition ¹			
				Default Mode (Reset Mode)	Default Function (Signal Name)	Input/Output	Value ²
DRAM_D11	AE7	NVCC_DRAM	DDR	ALT0	DRAM_DATA11	Input	PU (100K)
DRAM_D12	AB5	NVCC_DRAM	DDR	ALT0	DRAM_DATA12	Input	PU (100K)
DRAM_D13	AC5	NVCC_DRAM	DDR	ALT0	DRAM_DATA13	Input	PU (100K)
DRAM_D14	AB6	NVCC_DRAM	DDR	ALT0	DRAM_DATA14	Input	PU (100K)
DRAM_D15	AC7	NVCC_DRAM	DDR	ALT0	DRAM_DATA15	Input	PU (100K)
DRAM_D16	AB7	NVCC_DRAM	DDR	ALT0	DRAM_DATA16	Input	PU (100K)
DRAM_D17	AA8	NVCC_DRAM	DDR	ALT0	DRAM_DATA17	Input	PU (100K)
DRAM_D18	AB9	NVCC_DRAM	DDR	ALT0	DRAM_DATA18	Input	PU (100K)
DRAM_D19	Y9	NVCC_DRAM	DDR	ALT0	DRAM_DATA19	Input	PU (100K)
DRAM_D2	AC4	NVCC_DRAM	DDR	ALT0	DRAM_DATA02	Input	PU (100K)
DRAM_D20	Y7	NVCC_DRAM	DDR	ALT0	DRAM_DATA20	Input	PU (100K)
DRAM_D21	Y8	NVCC_DRAM	DDR	ALT0	DRAM_DATA21	Input	PU (100K)
DRAM_D22	AC8	NVCC_DRAM	DDR	ALT0	DRAM_DATA22	Input	PU (100K)
DRAM_D23	AA9	NVCC_DRAM	DDR	ALT0	DRAM_DATA23	Input	PU (100K)
DRAM_D24	AE9	NVCC_DRAM	DDR	ALT0	DRAM_DATA24	Input	PU (100K)
DRAM_D25	Y10	NVCC_DRAM	DDR	ALT0	DRAM_DATA25	Input	PU (100K)
DRAM_D26	AE11	NVCC_DRAM	DDR	ALT0	DRAM_DATA26	Input	PU (100K)
DRAM_D27	AB11	NVCC_DRAM	DDR	ALT0	DRAM_DATA27	Input	PU (100K)
DRAM_D28	AC9	NVCC_DRAM	DDR	ALT0	DRAM_DATA28	Input	PU (100K)
DRAM_D29	AD9	NVCC_DRAM	DDR	ALT0	DRAM_DATA29	Input	PU (100K)
DRAM_D3	AA5	NVCC_DRAM	DDR	ALT0	DRAM_DATA03	Input	PU (100K)
DRAM_D30	AD11	NVCC_DRAM	DDR	ALT0	DRAM_DATA30	Input	PU (100K)
DRAM_D31	AC11	NVCC_DRAM	DDR	ALT0	DRAM_DATA31	Input	PU (100K)
DRAM_D32	AA17	NVCC_DRAM	DDR	ALT0	DRAM_DATA32	Input	PU (100K)
DRAM_D33	AA18	NVCC_DRAM	DDR	ALT0	DRAM_DATA33	Input	PU (100K)
DRAM_D34	AC18	NVCC_DRAM	DDR	ALT0	DRAM_DATA34	Input	PU (100K)
DRAM_D35	AE19	NVCC_DRAM	DDR	ALT0	DRAM_DATA35	Input	PU (100K)
DRAM_D36	Y17	NVCC_DRAM	DDR	ALT0	DRAM_DATA36	Input	PU (100K)
DRAM_D37	Y18	NVCC_DRAM	DDR	ALT0	DRAM_DATA37	Input	PU (100K)
DRAM_D38	AB19	NVCC_DRAM	DDR	ALT0	DRAM_DATA38	Input	PU (100K)
DRAM_D39	AC19	NVCC_DRAM	DDR	ALT0	DRAM_DATA39	Input	PU (100K)
DRAM_D4	AC1	NVCC_DRAM	DDR	ALT0	DRAM_DATA04	Input	PU (100K)
DRAM_D40	Y19	NVCC_DRAM	DDR	ALT0	DRAM_DATA40	Input	PU (100K)
DRAM_D41	AB20	NVCC_DRAM	DDR	ALT0	DRAM_DATA41	Input	PU (100K)
DRAM_D42	AB21	NVCC_DRAM	DDR	ALT0	DRAM_DATA42	Input	PU (100K)
DRAM_D43	AD21	NVCC_DRAM	DDR	ALT0	DRAM_DATA43	Input	PU (100K)

Table 100. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition ¹			
				Default Mode (Reset Mode)	Default Function (Signal Name)	Input/Output	Value ²
EIM_DA10	M22	NVCC_EIM2	GPIO	ALT0	EIM_AD10	Input	PU (100K)
EIM_DA11	M20	NVCC_EIM2	GPIO	ALT0	EIM_AD11	Input	PU (100K)
EIM_DA12	M24	NVCC_EIM2	GPIO	ALT0	EIM_AD12	Input	PU (100K)
EIM_DA13	M23	NVCC_EIM2	GPIO	ALT0	EIM_AD13	Input	PU (100K)
EIM_DA14	N23	NVCC_EIM2	GPIO	ALT0	EIM_AD14	Input	PU (100K)
EIM_DA15	N24	NVCC_EIM2	GPIO	ALT0	EIM_AD15	Input	PU (100K)
EIM_EB0	K21	NVCC_EIM2	GPIO	ALT0	EIM_EB0_B	Output	1
EIM_EB1	K23	NVCC_EIM2	GPIO	ALT0	EIM_EB1_B	Output	1
EIM_EB2	E22	NVCC_EIM0	GPIO	ALT5	GPIO2_IO30	Input	PU (100K)
EIM_EB3	F23	NVCC_EIM0	GPIO	ALT5	GPIO2_IO31	Input	PU (100K)
EIM_LBA	K22	NVCC_EIM1	GPIO	ALT0	EIM_LBA_B	Output	1
EIM_OE	J24	NVCC_EIM1	GPIO	ALT0	EIM_OE	Output	1
EIM_RW	K20	NVCC_EIM1	GPIO	ALT0	EIM_RW	Output	1
EIM_WAIT	M25	NVCC_EIM2	GPIO	ALT0	EIM_WAIT	Input	PU (100K)
ENET_CRSDV	U21	NVCC_ENET	GPIO	ALT5	GPIO1_IO25	Input	PU (100K)
ENET_MDC	V20	NVCC_ENET	GPIO	ALT5	GPIO1_IO31	Input	PU (100K)
ENET_MDIO	V23	NVCC_ENET	GPIO	ALT5	GPIO1_IO22	Input	PU (100K)
ENET_REF_CLK ³	V22	NVCC_ENET	GPIO	ALT5	GPIO1_IO23	Input	PU (100K)
ENET_RX_ER	W23	NVCC_ENET	GPIO	ALT5	GPIO1_IO24	Input	PU (100K)
ENET_RXD0	W21	NVCC_ENET	GPIO	ALT5	GPIO1_IO27	Input	PU (100K)
ENET_RXD1	W22	NVCC_ENET	GPIO	ALT5	GPIO1_IO26	Input	PU (100K)
ENET_TX_EN	V21	NVCC_ENET	GPIO	ALT5	GPIO1_IO28	Input	PU (100K)
ENET_TXD0	U20	NVCC_ENET	GPIO	ALT5	GPIO1_IO30	Input	PU (100K)
ENET_TXD1	W20	NVCC_ENET	GPIO	ALT5	GPIO1_IO29	Input	PU (100K)
GPIO_0	T5	NVCC_GPIO	GPIO	ALT5	GPIO1_IO00	Input	PD (100K)
GPIO_1	T4	NVCC_GPIO	GPIO	ALT5	GPIO1_IO01	Input	PU (100K)
GPIO_16	R2	NVCC_GPIO	GPIO	ALT5	GPIO7_IO11	Input	PU (100K)
GPIO_17	R1	NVCC_GPIO	GPIO	ALT5	GPIO7_IO12	Input	PU (100K)
GPIO_18	P6	NVCC_GPIO	GPIO	ALT5	GPIO7_IO13	Input	PU (100K)
GPIO_19	P5	NVCC_GPIO	GPIO	ALT5	GPIO4_IO05	Input	PU (100K)
GPIO_2	T1	NVCC_GPIO	GPIO	ALT5	GPIO1_IO02	Input	PU (100K)
GPIO_3	R7	NVCC_GPIO	GPIO	ALT5	GPIO1_IO03	Input	PU (100K)
GPIO_4	R6	NVCC_GPIO	GPIO	ALT5	GPIO1_IO04	Input	PU (100K)
GPIO_5	R4	NVCC_GPIO	GPIO	ALT5	GPIO1_IO05	Input	PU (100K)
GPIO_6	T3	NVCC_GPIO	GPIO	ALT5	GPIO1_IO06	Input	PU (100K)
GPIO_7	R3	NVCC_GPIO	GPIO	ALT5	GPIO1_IO07	Input	PU (100K)

Table 100. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition ¹			
				Default Mode (Reset Mode)	Default Function (Signal Name)	Input/Output	Value ²
LVDS0_TX3_P	W1	NVCC_LVDS_2P5	LVDS	ALT0	LVDS0_TX3_P	Input	Keeper
LVDS1_CLK_N	Y3	NVCC_LVDS_2P5	LVDS	—	LVDS1_CLK_N	—	—
LVDS1_CLK_P	Y4	NVCC_LVDS_2P5	LVDS	ALT0	LVDS1_CLK_P	Input	Keeper
LVDS1_TX0_N	Y1	NVCC_LVDS_2P5	LVDS	—	LVDS1_TX0_N	—	—
LVDS1_TX0_P	Y2	NVCC_LVDS_2P5	LVDS	ALT0	LVDS1_TX0_P	Input	Keeper
LVDS1_TX1_N	AA2	NVCC_LVDS_2P5	LVDS	—	LVDS1_TX1_N	—	—
LVDS1_TX1_P	AA1	NVCC_LVDS_2P5	LVDS	ALT0	LVDS1_TX1_P	Input	Keeper
LVDS1_TX2_N	AB1	NVCC_LVDS_2P5	LVDS	—	LVDS1_TX2_N	—	—
LVDS1_TX2_P	AB2	NVCC_LVDS_2P5	LVDS	ALT0	LVDS1_TX2_P	Input	Keeper
LVDS1_TX3_N	AA3	NVCC_LVDS_2P5	LVDS	—	LVDS1_TX3_N	—	—
LVDS1_TX3_P	AA4	NVCC_LVDS_2P5	LVDS	ALT0	LVDS1_TX3_P	Input	Keeper
MLB_CN	A11	VDD_HIGH_CAP	LVDS	—	MLB_CLK_N	—	—
MLB_CP	B11	VDD_HIGH_CAP	LVDS	—	MLB_CLK_P	—	—
MLB_DN	B10	VDD_HIGH_CAP	LVDS	—	MLB_DATA_N	—	—
MLB_DP	A10	VDD_HIGH_CAP	LVDS	—	MLB_DATA_P	—	—
MLB_SN	A9	VDD_HIGH_CAP	LVDS	—	MLB_SIG_N	—	—
MLB_SP	B9	VDD_HIGH_CAP	LVDS	—	MLB_SIG_P	—	—
NANDF_ALE	A16	NVCC_NANDF	GPIO	ALT5	GPIO6_IO08	Input	PU (100K)
NANDF_CLE	C15	NVCC_NANDF	GPIO	ALT5	GPIO6_IO07	Input	PU (100K)
NANDF_CS0	F15	NVCC_NANDF	GPIO	ALT5	GPIO6_IO11	Input	PU (100K)
NANDF_CS1	C16	NVCC_NANDF	GPIO	ALT5	GPIO6_IO14	Input	PU (100K)
NANDF_CS2	A17	NVCC_NANDF	GPIO	ALT5	GPIO6_IO15	Input	PU (100K)
NANDF_CS3	D16	NVCC_NANDF	GPIO	ALT5	GPIO6_IO16	Input	PU (100K)
NANDF_D0	A18	NVCC_NANDF	GPIO	ALT5	GPIO2_IO00	Input	PU (100K)
NANDF_D1	C17	NVCC_NANDF	GPIO	ALT5	GPIO2_IO01	Input	PU (100K)
NANDF_D2	F16	NVCC_NANDF	GPIO	ALT5	GPIO2_IO02	Input	PU (100K)
NANDF_D3	D17	NVCC_NANDF	GPIO	ALT5	GPIO2_IO03	Input	PU (100K)
NANDF_D4	A19	NVCC_NANDF	GPIO	ALT5	GPIO2_IO04	Input	PU (100K)
NANDF_D5	B18	NVCC_NANDF	GPIO	ALT5	GPIO2_IO05	Input	PU (100K)
NANDF_D6	E17	NVCC_NANDF	GPIO	ALT5	GPIO2_IO06	Input	PU (100K)
NANDF_D7	C18	NVCC_NANDF	GPIO	ALT5	GPIO2_IO07	Input	PU (100K)
NANDF_RB0	B16	NVCC_NANDF	GPIO	ALT5	GPIO6_IO10	Input	PU (100K)
NANDF_WP_B	E15	NVCC_NANDF	GPIO	ALT5	GPIO6_IO09	Input	PU (100K)
ONOFF	D12	VDD_SNVS_IN	GPIO	—	SRC_ONOFF	Input	PU (100K)
PCIE_RXM	B1	PCIE_VPH	—	—	PCIE_RX_N	—	—
PCIE_RXP	B2	PCIE_VPH	—	—	PCIE_RX_P	—	—