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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST7
Core Size	8-Bit
Speed	8MHz
Connectivity	CANbus, I²C, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	48
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3.8V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st72f521r6tatr

Table 3. Device pin description (continued)

Pin			Type	Level		Port						Main function (after reset)	Alternate function	
No.		Name				Input				Output				
LQFP80	LQFP64			Input	Output	float	wpu	int	ana	OD	PP			
23	17	PD4/AIN4	I/O	C_T		**X**	X		X	X	X	Port D4	ADC Analog Input 4	
24	18	PD5/AIN5	I/O	C_T		**X**	X		X	X	X	Port D5	ADC Analog Input 5	
25	19	PD6/AIN6	I/O	C_T		**X**	X		X	X	X	Port D6	ADC Analog Input 6	
26	20	PD7/AIN7	I/O	C_T		**X**	X		X	X	X	Port D7	ADC Analog Input 7	
27	21	V_{AREF}(2)	I									Analog Reference Voltage for ADC		
28	22	V_{SSA}(2)	S									Analog Ground Voltage		
29	23	V_{DD_3}(2)	S									Digital Main Supply Voltage		
30	24	V_{SS_3}(2)	S									Digital Ground Voltage		
31	-(1)	PG4	I/O	T_T		**X**	X			X	X	Port G4		
32	-(1)	PG5	I/O	T_T		**X**	X			X	X	Port G5		
33	25	PF0/MCO/AIN8	I/O	C_T		**X**	ei1		X	X	X	Port F0	Main clock out (f_{CPU})	ADC Analog Input 8
34	26	PF1 (HS)/BEEP	I/O	C_T	HS	**X**	ei1			X	X	Port F1	Beep signal output	
35	27	PF2 (HS)	I/O	C_T	HS	**X**		ei1		X	X	Port F2		
36	28	PF3/OCMP2_A/AIN9	I/O	C_T		**X**	X		X	X	X	Port F3	Timer A Output Compare 2	ADC Analog Input 9
37	29	PF4/OCMP1_A/AIN10	I/O	C_T		**X**	X		X	X	X	Port F4	Timer A Output Compare 1	ADC Analog Input 10
38	30	PF5/ICAP2_A/AIN11	I/O	C_T		**X**	X		X	X	X	Port F5	Timer A Input Capture 2	ADC Analog Input 11
39	31	PF6 (HS)/ICAP1_A	I/O	C_T	HS	**X**	X			X	X	Port F6	Timer A Input Capture 1	
40	32	PF7 (HS)/EXTCLK_A	I/O	C_T	HS	**X**	X			X	X	Port F7	Timer A External Clock Source	
41	33	V_{DD_0}(2)	S									Digital Main Supply Voltage		
42	34	V_{SS_0}(2)	S									Digital Ground Voltage		
43	35	PC0/OCMP2_B/AIN12	I/O	C_T		**X**	X		X	X	X	Port C0	Timer B Output Compare 2	ADC Analog Input 12
44	36	PC1/OCMP1_B/AIN13	I/O	C_T		**X**	X		X	X	X	Port C1	Timer B Output Compare 1	ADC Analog Input 13

4 Flash program memory

4.1 Introduction

The ST7 dual voltage High Density Flash (HDFlash) is a non-volatile memory that can be electrically erased as a single block or by individual sectors and programmed on a byte-by-byte basis using an external V_{PP} supply.

The HDFlash devices can be programmed and erased off-board (plugged in a programming tool) or on-board using ICP (in-circuit programming) or IAP (in-application programming).

The array matrix organization allows each sector to be erased and reprogrammed without affecting other sectors.

4.2 Main features

- 3 Flash programming modes:
  - Insertion in a programming tool. In this mode, all sectors including option bytes can be programmed or erased.
  - ICP (in-circuit programming). In this mode, all sectors including option bytes can be programmed or erased without removing the device from the application board.
  - IAP (in-application programming). In this mode, all sectors except Sector 0 can be programmed or erased without removing the device from the application board and while the application is running.
- ICT (in-circuit testing) for downloading and executing user application test patterns in RAM
- Readout protection
- Register Access Security System (RASS) to prevent accidental programming or erasing

4.3 Structure

The Flash memory is organized in sectors and can be used for both code and data storage.

Depending on the overall Flash memory size in the microcontroller device, there are up to three user sectors (see *Table 5*). Each of these sectors can be erased independently to avoid unnecessary erasing of the whole Flash memory when only a partial erasing is required.

Table 5. Sectors available in Flash devices

Flash size (bytes)	Available sectors
4K	Sector 0
8K	Sectors 0, 1
> 8K	Sectors 0, 1, 2

The first two sectors have a fixed size of 4 Kbytes (see *Figure 5*). They are mapped in the upper part of the ST7 addressing space so the reset and interrupt vectors are located in Sector 0 (F000h-FFFFh).

Crystal/ceramic oscillators

This family of oscillators has the advantage of producing a very accurate rate on the main clock of the ST7. The selection within a list of four oscillators with different frequency ranges has to be done by option byte in order to reduce consumption (refer to *Section 22.1.1: Flash configuration on page 257* for more details on the frequency ranges). In this mode of the multi-oscillator, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and start-up stabilization time. The loading capacitance values must be adjusted according to the selected oscillator.

These oscillators are not stopped during the RESET phase to avoid losing time in the oscillator start-up phase.

Internal RC oscillator

This oscillator allows a low cost solution for the main clock of the ST7 using only an internal resistor and capacitor. Internal RC oscillator mode has the drawback of a lower frequency accuracy and should not be used in applications that require accurate timing.

In this mode, the two oscillator pins have to be tied to ground.

Table 10. ST7 clock sources

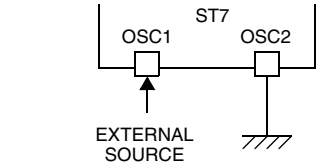
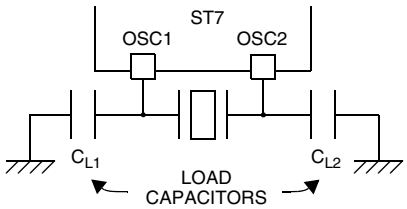
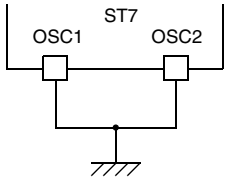
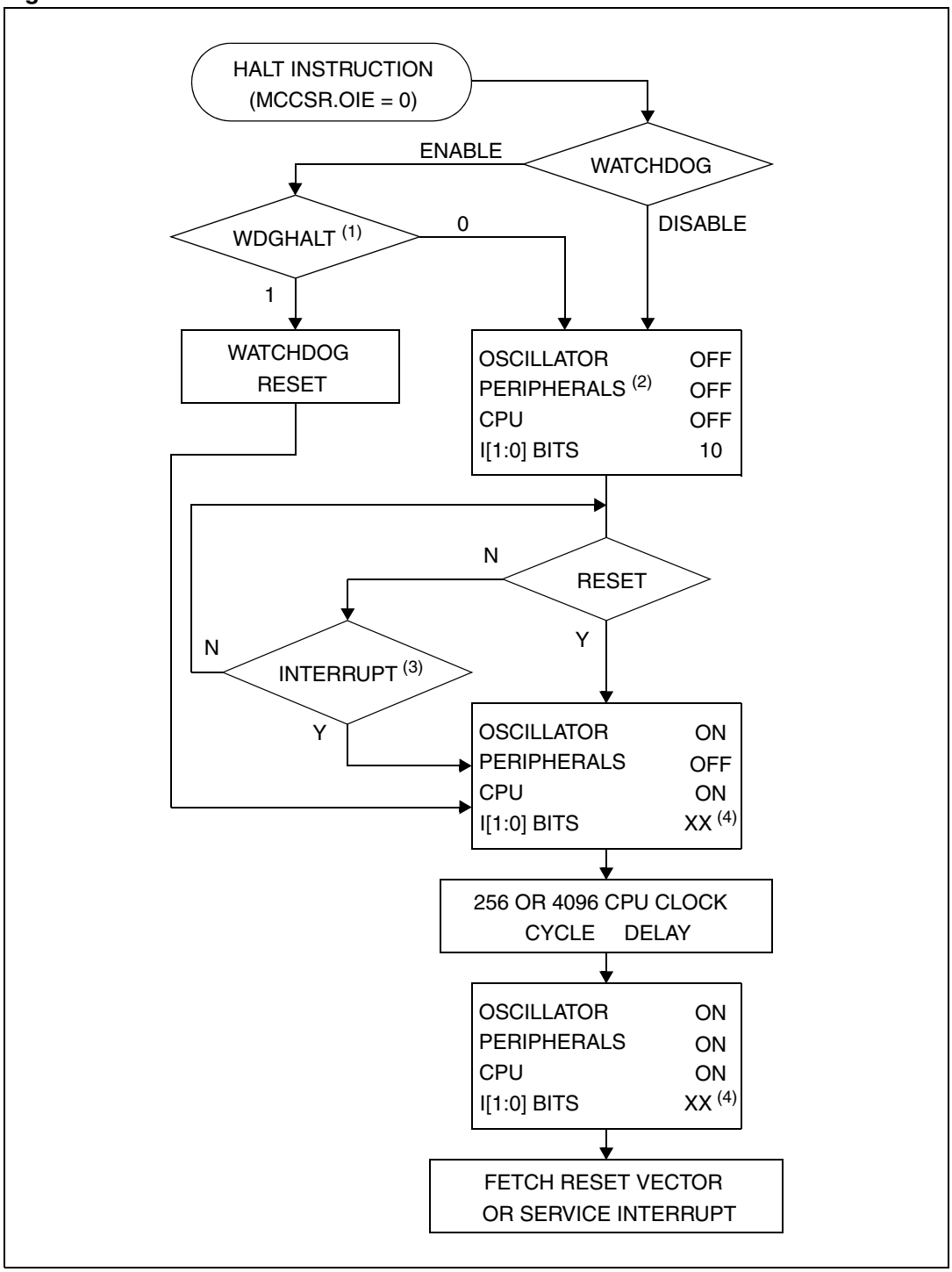
	Hardware configuration
External clock	
Crystal/Ceramic resonators	
Internal RC oscillator	

Table 26. Nested interrupts register map and reset values

Address (Hex.)	Register label	7	6	5	4	3	2	1	0
0024h	ISPR0	ei1		ei0		MCC		TLI	
	Reset value	I1_3 1	I0_3 1	I1_2 1	I0_2 1	I1_1 1	I0_1 1	1	1
0025h	ISPR1	SPI		CAN		ei3		ei2	
	Reset value	I1_7 1	I0_7 1	I1_6 1	I0_6 1	I1_5 1	I0_5 1	I1_4 1	I0_4 1
0026h	ISPR2	AVD		SCI		TIMER B		TIMER A	
	Reset value	I1_11 1	I0_11 1	I1_10 1	I0_10 1	I1_9 1	I0_9 1	I1_8 1	I0_8 1
0027h	ISPR3					PWMART		I2C	
	Reset value	1	1	1	1	I1_13 1	I0_13 1	I1_12 1	I0_12 1
0028h	EICR	IS11	IS10	IPB	IS21	IS20	IPA	TLIS	TLIE
	Reset value	0	0	0	0	0	0	0	0

Figure 28. Halt mode flowchart



1. WDGHALT is an option bit. See *Section 22.1.1: Flash configuration on page 257* for more details.
2. Peripheral clocked with an external clock source can still be active.
3. Only some specific interrupts can exit the MCU from Halt mode (such as external interrupt). Refer to *Table 20: Interrupt mapping* for more details.
4. Before servicing an interrupt, the CC register is pushed on the stack. The I[1:0] bits of the CC register are set to the current software priority level of the interrupt routine and recovered when the CC register is popped.

5 *The alternate inputs (ICAP1 and ICAP2) are always directly connected to the timer. So any transitions on these pins activates the input capture function.*

6 *Moreover if one of the ICAPi pins is configured as an input and the second one as an output, an interrupt can be generated if the user toggles the output pin and if the ICIE bit is set.*

7 *This can be avoided if the input capture function i is disabled by reading the ICiHR (see note 1).*

8 *The TOF bit can be used with interrupt generation in order to measure events that go beyond the timer range (FFFFh).*

Figure 46. Input capture block diagram

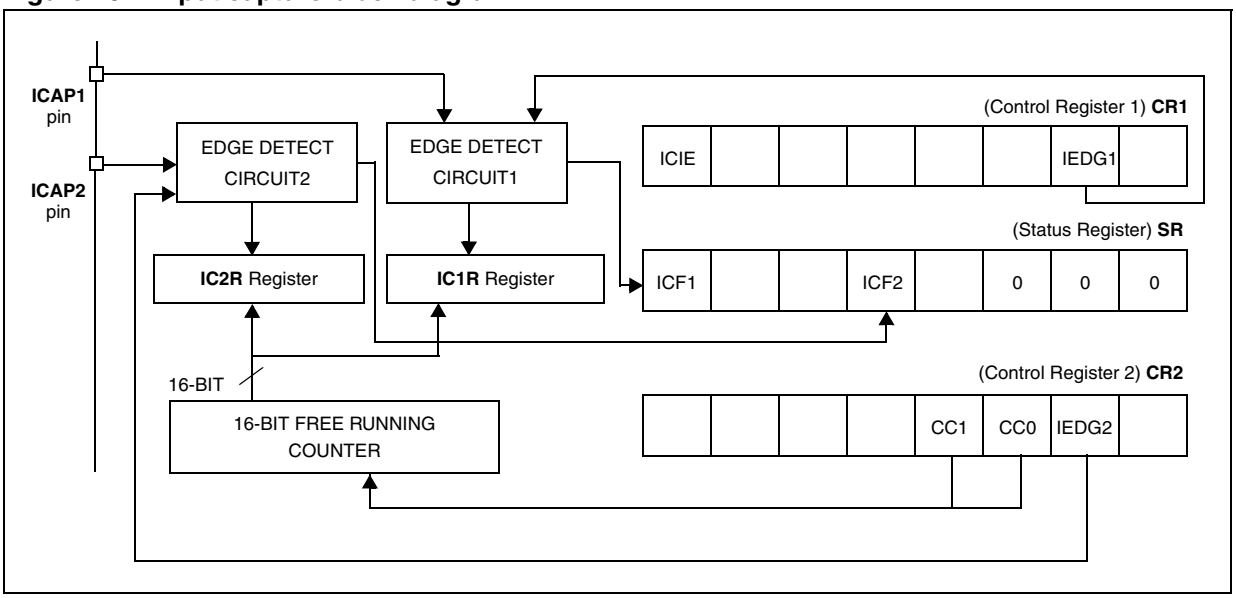
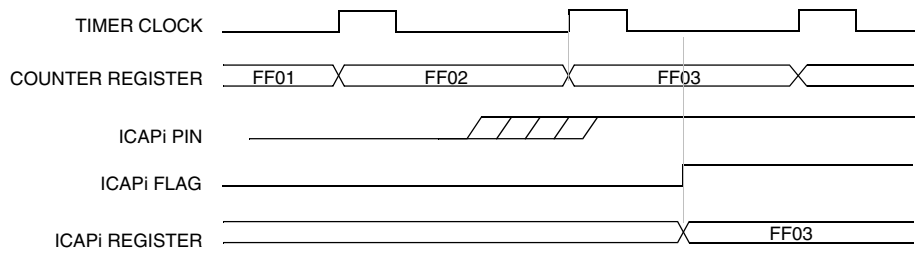


Figure 47. Input capture timing diagram



Note: The rising edge is the active edge.

13.3.6 One Pulse mode

One Pulse mode enables the generation of a pulse when an external event occurs. This mode is selected via the OPM bit in the CR2 register.

The one pulse mode uses the Input Capture1 function and the Output Compare1 function.

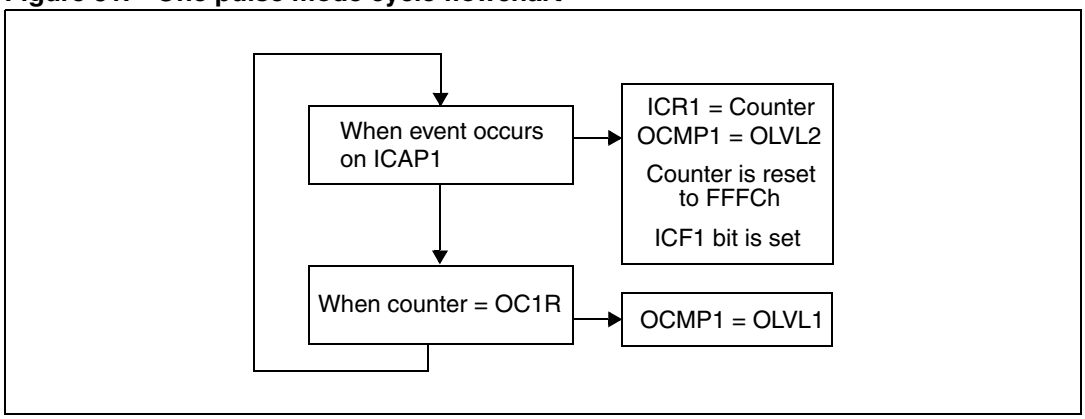
Procedure

To use one pulse mode:

1. Load the OC1R register with the value corresponding to the length of the pulse (using the appropriate formula below according to the timer clock source used).
2. Select the following in the CR1 register:
   - Using the OLVL1 bit, select the level to be applied to the OCMP1 pin after the pulse.
   - Using the OLVL2 bit, select the level to be applied to the OCMP1 pin during the pulse.
   - Select the edge of the active transition on the ICAP1 pin with the IEDG1 bit (the ICAP1 pin must be configured as floating input).
3. Select the following in the CR2 register:
   - Set the OC1E bit, the OCMP1 pin is then dedicated to the Output Compare 1 function.
   - Set the OPM bit.
   - Select the timer clock CC[1:0] (see *Table 61: Timer clock selection*).

Then, on a valid event on the ICAP1 pin, the counter is initialized to FFFCh and OLVL2 bit is loaded on the OCMP1 pin, the ICF1 bit is set and the value FFFDh is loaded in the IC1R register.

Figure 51. One pulse mode cycle flowchart



Because the ICF1 bit is set when an active edge occurs, an interrupt can be generated if the ICIE bit is set.

Clearing the input capture interrupt request (that is, clearing the ICF*i* bit) is done in two steps:

1. Reading the SR register while the ICF*i* bit is set
2. An access (read or write) to the IC*i*LR register

13.7.5 Input capture 1 low register (IC1LR)

This is an 8-bit read only register that contains the low part of the counter value (transferred by the input capture 1 event).

IC1LR — Reset value: Undefined

7	6	5	4	3	2	1	0
MSB							LSB
RO	RO	RO	RO	RO	RO	RO	RO

13.7.6 Output compare 1 high register (OC1HR)

This is an 8-bit register that contains the high part of the value to be compared to the CHR register.

OC1HR — Reset value: 1000 0000 (80h)

7	6	5	4	3	2	1	0
MSB							LSB
RW	RW	RW	RW	RW	RW	RW	RW

13.7.7 Output compare 1 low register (OC1LR)

This is an 8-bit register that contains the low part of the value to be compared to the CLR register.

OC1LR — Reset value: 0000 0000 (00h)

7	6	5	4	3	2	1	0
MSB							LSB
RW	RW	RW	RW	RW	RW	RW	RW

13.7.8 Output compare 2 high register (OC2HR)

This is an 8-bit register that contains the high part of the value to be compared to the CHR register.

OC2HR — Reset value: 1000 0000 (80h)

7	6	5	4	3	2	1	0
MSB							LSB
RW	RW	RW	RW	RW	RW	RW	RW

14.8 SPI registers

14.8.1 Control register (SPICR)

SPICR Reset value: 0000 xxxx (0xh)

7	6	5	4	3	2	1	0
SPIE	SPE	SPR2	MSTR	CPOL	CPHA	SPR[1:0]	
RW	RW	RW	RW	RW	RW	RW	

Table 66. SPICR register description

Bit	Name	Function
7	SPIE	*Serial Peripheral Interrupt Enable* This bit is set and cleared by software. 0: Interrupt is inhibited 1: An SPI interrupt is generated whenever SPIF = 1, MODF = 1 or OVR = 1 in the SPICSR register.
6	SPE	*Serial Peripheral Output Enable* This bit is set and cleared by software. It is also cleared by hardware when, in master mode, $\overline{SS}$ = 0 (see *Master mode fault (MODF) on page 131*). The SPE bit is cleared by reset, so the SPI peripheral is not initially connected to the external pins. 0: I/O pins free for general purpose I/O 1: SPI I/O pin alternate functions enabled
5	SPR2	*Divider Enable* This bit is set and cleared by software and is cleared by reset. It is used with the SPR[1:0] bits to set the baud rate. Refer to *Table 67*. 0: Divider by 2 enabled 1: Divider by 2 disabled *Note: This bit has no effect in slave mode.*
4	MSTR	*Master Mode* This bit is set and cleared by software. It is also cleared by hardware when, in master mode, $\overline{SS}$ = 0 (see *Master mode fault (MODF) on page 131*). 0: Slave mode 1: Master mode. The function of the SCK pin changes from an input to an output and the functions of the MISO and MOSI pins are reversed.
3	CPOL	*Clock Polarity* This bit is set and cleared by software. This bit determines the idle state of the serial Clock. The CPOL bit affects both the master and slave modes. 0: SCK pin has a low level idle state 1: SCK pin has a high level idle state *Note: If CPOL is changed at the communication byte boundaries, the SPI must be disabled by resetting the SPE bit.*
2	CPHA	*Clock Phase* This bit is set and cleared by software. 0: The first clock transition is the first data capture edge. 1: The second clock transition is the first capture edge. *Note: The slave must have the same CPOL and CPHA settings as the master.*

Table 66. SPICR register description (continued)

Bit	Name	Function
1:0	SPR[1:0]	*Serial Clock Frequency* These bits are set and cleared by software. Used with the SPR2 bit, they select the baud rate of the SPI serial clock SCK output by the SPI in master mode. *Note: These 2 bits have no effect in slave mode.*

Table 67. SPI master mode SCK frequency

Serial clock	SPR2	SPR1	SPR0
$f_{CPU}/4$	1	0	0
$f_{CPU}/8$	0	0	0
$f_{CPU}/16$	0	0	1
$f_{CPU}/32$	1	1	0
$f_{CPU}/64$	0	1	0
$f_{CPU}/128$	0	1	1

14.8.2 Control/status register (SPICSR)

SPICSR Reset value: 0000 0000 (00h)

7	6	5	4	3	2	1	0
SPIF	WCOL	OVR	MODF	Reserved	SOD	SSM	SSI
RO	RO	RO	RO	-	RW	RW	RW

Table 68. SPICSR register description

Bit	Name	Function
7	SPIF	*Serial Peripheral Data Transfer Flag* This bit is set by hardware when a transfer has been completed. An interrupt is generated if SPIE = 1 in the SPICR register. It is cleared by a software sequence (an access to the SPICSR register followed by a write or a read to the SPIDR register). 0: Data transfer is in progress or the flag has been cleared 1: Data transfer between the device and an external device has been completed. While the SPIF bit is set, all writes to the SPIDR register are inhibited until the SPICSR register is read.
6	WCOL	*Write Collision status* This bit is set by hardware when a write to the SPIDR register is done during a transmit sequence. It is cleared by a software sequence (see *Figure 60*). 0: No write collision occurred. 1: A write collision has been detected.
5	OVR	*SPI Overrun error* This bit is set by hardware when the byte currently being received in the shift register is ready to be transferred into the SPIDR register while SPIF = 1 (see *Overrun condition (OVR) on page 131*). An interrupt is generated if SPIE = 1 in SPICR register. The OVR bit is cleared by software reading the SPICSR register. 0: No overrun error 1: Overrun error detected

15 Serial communications interface (SCI)

15.1 Introduction

The Serial Communications Interface (SCI) offers a flexible means of full-duplex data exchange with external equipment requiring an industry standard NRZ asynchronous serial data format. The SCI offers a very wide range of baud rates using two baud rate generator systems.

15.2 Main features

- Full duplex, asynchronous communications
- NRZ standard format (Mark/Space)
- Dual baud rate generator systems
- Independently programmable transmit and receive baud rates up to 500K baud
- Programmable data word length (8 or 9 bits)
- Receive buffer full, Transmit buffer empty and End of Transmission flags
- 2 receiver wake-up modes:
  - Address bit (MSB)
  - Idle line
- Muting function for multiprocessor configurations
- Separate enable bits for Transmitter and Receiver
- 4 error detection flags:
  - Overrun error
  - Noise error
  - Frame error
  - Parity error
- 5 interrupt sources with flags:
  - Transmit data register empty
  - Transmission complete
  - Receive data register full
  - Idle line received
  - Overrun error detected
- Parity control:
  - Transmits parity bit
  - Checks parity of received data byte
- Reduced power consumption mode

Table 84. SR1 register description (continued)

Bit	Name	Function
1	M/SL	*Master/Slave* This bit is set by hardware as soon as the interface is in Master mode (writing START = 1). It is cleared by hardware after detecting a Stop condition on the bus or a loss of arbitration (ARLO = 1). It is also cleared when the interface is disabled (PE = 0). 0: Slave mode 1: Master mode
0	SB	*Start bit (Master mode)* This bit is set by hardware as soon as the Start condition is generated (following a write START = 1). An interrupt is generated if ITE = 1. It is cleared by software reading SR1 register followed by writing the address byte in DR register. It is also cleared by hardware when the interface is disabled (PE = 0). 0: No Start condition 1: Start condition generated

16.7.3 I²C status register 2 (SR2)

SR2 Reset value: 0000 0000 (00h)

7	6	5	4	3	2	1	0
Reserved			AF	STOPF	ARLO	BERR	GCAL
-			RO	RO	RO	RO	RO

Table 85. SR2 register description

Bit	Name	Function
7:5	-	Reserved. Forced to 0 by hardware.
4	AF	*Acknowledge failure* This bit is set by hardware when no acknowledge is returned. An interrupt is generated if ITE = 1. It is cleared by software reading SR2 register or by hardware when the interface is disabled (PE = 0). The SCL line is not held low while AF = 1 but by other flags (SB or BTF) that are set at the same time. 0: No acknowledge failure 1: Acknowledge failure *Note: When an AF event occurs, the SCL line is not held low; however, the SDA line can remain low if the last bits transmitted are all 0. It is then necessary to release both lines by software.*
3	STOPF	*Stop detection (Slave mode)* This bit is set by hardware when a Stop condition is detected on the bus after an acknowledge (if ACK = 1). An interrupt is generated if ITE = 1. It is cleared by software reading SR2 register or by hardware when the interface is disabled (PE = 0). The SCL line is not held low while STOPF = 1. 0: No Stop condition detected 1: Stop condition detected

Table 86. CCR register description (continued)

Bit	Name	Function
6:0	CC[6:0]	*7-bit clock divider* These bits select the speed of the bus (f_{SCL}) depending on the I^2C mode. They are not cleared when the interface is disabled (PE = 0). Refer to *Section 20: Electrical characteristics* for the table of values. *Note: The programmed f_{SCL} assumes no load on SCL and SDA lines.*

16.7.5 I^2C data register (DR)

DR — Reset value: 0000 0000 (00h)

7	6	5	4	3	2	1	0
D[7:0]							
RW							

Table 87. DR register description

Bit	Name	Function
7:0	D[7:0]	*8-bit Data Register* These bits contain the byte to be received or transmitted on the bus. **Transmitter mode:** Byte transmission start automatically when the software writes in the DR register. **Receiver mode:** The first data byte is received automatically in the DR register using the least significant bit of the address. Then, the following data bytes are received one by one after reading the DR register.

16.7.6 I^2C own address register (OAR1)

OAR1 — Reset value: 0000 0000 (00h)

7	6	5	4	3	2	1	0
ADD7	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0
RW	RW	RW	RW	RW	RW	RW	RW

20.6 Memory characteristics

20.6.1 RAM and hardware registers

Table 140. RAM supply voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RM}	Data retention mode(1)	Halt mode (or RESET)	1.6			V

1. Minimum V_{DD} supply voltage without losing data stored in RAM (in Halt mode or under RESET) or in hardware registers (only in Halt mode). Not tested in production.

20.6.2 Flash memory

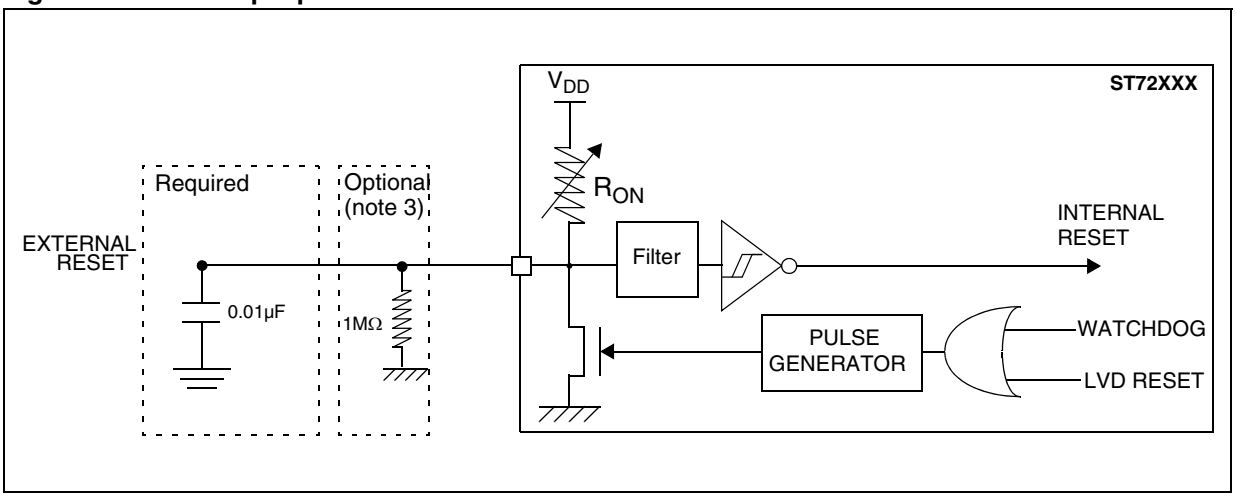
Table 141. Dual voltage HDFlash memory

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
f_{CPU}	Operating frequency	Read mode	0		8	MHz
		Write / Erase mode	1		8	
V_{PP}	Programming voltage(2)	$4.5V \le V_{DD} \le 5.5V$	11.4		12.6	V
I_{DD}	Supply current(3)	Run mode (f_{CPU} = 4 MHz)			3	mA
		Write / Erase		0		
		Power down mode / HALT		1	10	µA
I_{PP}	V_{PP} current(3)	Read (V_{PP} = 12V)			200	
		Write / Erase			30	mA
t_{VPP}	Internal V_{PP} stabilization time			10		µs
t_{RET}	Data retention	T_A = 55°C	20			years
N_{RW}	Write erase cycles	T_A = 85°C	100			cycles
T_{PROG} T_{ERASE}	Programming or erasing temperature range		-40	25	85	°C

1. Data based on characterization results, not tested in production
2. V_{PP} must be applied only during the programming or erasing operation and not permanently for reliability reasons.
3. Data based on simulation results, not tested in production

Warning: Do not connect 12V to V_{PP} before V_{DD} is powered on, as this may damage the device.

Figure 105. $\overline{\text{RESET}}$ pin protection when LVD is enabled



Note: 1 The reset network protects the device against parasitic resets.

The output of the external reset circuit must have an open-drain output to drive the ST7 reset pad. Otherwise the device can be damaged when the ST7 generates an internal reset (LVD or watchdog).

Whether the reset source is internal or external, the user must ensure that the level on the $\overline{\text{RESET}}$ pin can go below the V_{IL} maximum level specified in Section 20.9.1 on page 240. Otherwise the reset will not be taken into account internally.

Because the reset circuit is designed to allow the internal RESET to be output in the $\overline{\text{RESET}}$ pin, the user must ensure that the current sunk on the $\overline{\text{RESET}}$ pin is less than the absolute maximum value specified for $I_{INJ(RESET)}$ in Section 20.2.2 on page 220.

2 When the LVD is enabled, it is recommended not to connect a pull-up resistor or capacitor. A 10nF pull-down capacitor is required to filter noise on the reset line.

3 In case a capacitive power supply is used, it is recommended to connect a 1MΩ pull-down resistor to the $\overline{\text{RESET}}$ pin to discharge any residual voltage induced by the capacitive effect of the power supply (this will add 5µA to the power consumption of the MCU).

4 Tips when using the LVD:

A. Check that all recommendations related to reset circuit have been applied (see notes above).

B. Check that the power supply is properly decoupled (100nF + 10µF close to the MCU). Refer to AN1709 and AN2017. If this cannot be done, it is recommended to put a 100nF + 1MΩ pull-down on the $\overline{\text{RESET}}$ pin.

C. The capacitors connected on the $\overline{\text{RESET}}$ pin and also the power supply are key to avoid any start-up marginality. In most cases, steps A and B above are sufficient for a robust solution. Otherwise, replace 10nF pull-down on the $\overline{\text{RESET}}$ pin with a 5µF to 20µF capacitor.

Figure 118. 64-pin (14x14) low profile quad flat package outline

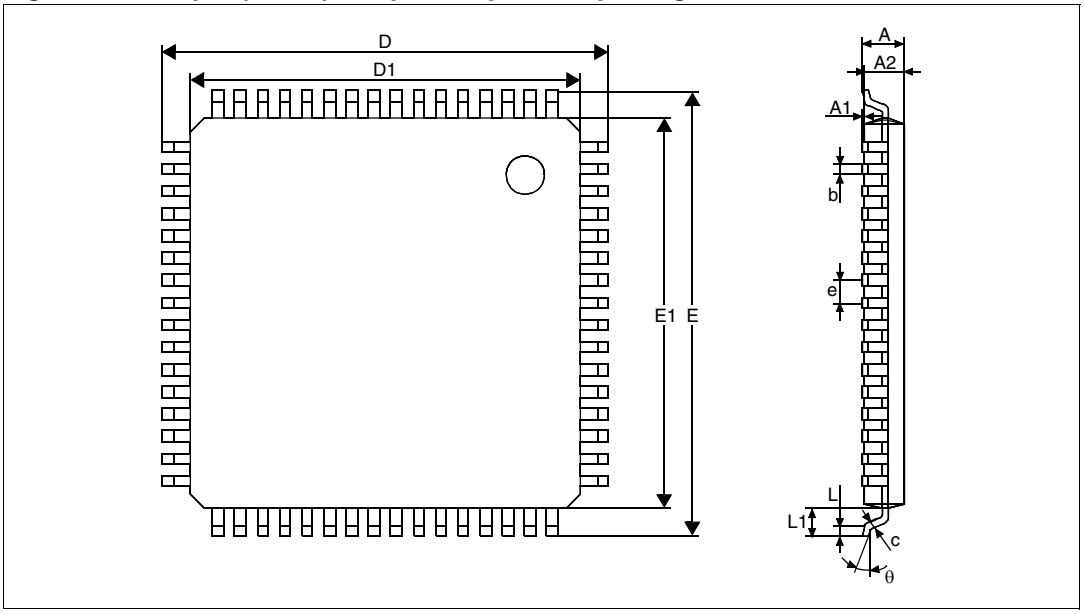


Table 159. 64-pin (14x14) low profile quad flat package mechanical data

Dimension	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.600			0.0630
A1	0.050		0.150	0.0020		0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.300	0.370	0.450	0.0118	0.0146	0.0177
c	0.090		0.200	0.0035		0.0079
D		16.000			0.6299	
D1		14.000			0.5512	
E		16.000			0.6299	
E1		14.000			0.5512	
e		0.800			0.0315	
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1		1.000			0.0394	

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Table 164. Option byte 1 bit description (continued)

Bit	Name	Function
OPT5:4	OSCTYPE[1:0]	Oscillator type These option bits select the ST7 main clock source type. 00: Clock source = Resonator oscillator 01: Reserved 10: Clock source = Internal RC oscillator 11: Clock source = External source
OPT3:1	OSCRANGE[2:0]	Oscillator range When the resonator oscillator type is selected, these option bits select the resonator oscillator current source corresponding to the frequency range of the used resonator. Otherwise, these bits are used to select the normal operating frequency range (see *Table 166: Oscillator frequency range selection (OPT3:1)*).
OPT0	PLLOFF	PLL activation This option bit activates the PLL which allows multiplication by two of the main input clock frequency. The PLL must not be used with the internal RC oscillator or with external clock source. The PLL is guaranteed only with an input frequency between 2 and 4 MHz. 0: PLL x2 enabled 1: PLL x2 disabled **Caution**: The PLL can be enabled only if the “OSCRANGE” (OPT3:1) bits are configured to “MP - 2~4 MHz”. Otherwise, the device functionality is not guaranteed.

Table 165. Package selection (OPT7)

Version	Selected package	PKG1	PKG0
M	LQFP80	1	1
(A)R	LQFP64	1	0

Note: On the chip, each I/O port has eight pads. Pads that are not bonded to external pins are in input pull-up configuration after reset. The configuration of these pads must be kept at reset state to avoid added current consumption.

Table 166. Oscillator frequency range selection (OPT3:1)

Typical frequency range		OSCRANGE		
		2	1	0
LP	1~2 MHz	0	0	0
MP	2~4 MHz	0	0	1
MS	4~8 MHz	0	1	0
HS	8~16 MHz	0	1	1

```
; check for falling edge
cp A,#$02

jrne OUT

TNZ Y

jrne OUT

LD A,#$01

LD sema,A
; set the semaphore to '1' if edge is detected
RIM
 ; reset the interrupt mask
LD A,sema
; check the semaphore status
CP A,#$01

jrne OUT

call call_routine
; call the interrupt routine
RIM

OUT:
RIM
JP while_loop

.call_routine
; entry to call_routine
PUSH A

PUSH X

PUSH CC

.ext1_rt
; entry to interrupt routine
LD A,#$00

LD sema,A

IRET
```