Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	852MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (1)
SATA	SATA 3Gbps (1)
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-40°C ~ 125°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	624-FBGA, FCBGA
Supplier Device Package	624-FCBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6d6avt08aer

1.1 Ordering Information

Table 1 shows examples of orderable part numbers covered by this data sheet. This table does not include all possible orderable part numbers. The latest part numbers are available on nxp.com/imx6series. If your desired part number is not listed in the table, or you have questions about available parts, see nxp.com/imx6series or contact your NXP representative.

Table 1. Example Orderable Part Numbers

Part Number	Quad/Dual CPU	Options	Speed[1] Grade	Temperature Grade	Package
MCIMX6Q6AVT10AC	i.MX 6Quad	Includes VPU, GPU	1 GHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6Q6AVT10AD	i.MX 6Quad	Includes VPU, GPU	1 GHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6Q6AVT10AE	i.MX 6Quad	Includes VPU, GPU	1 GHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6Q4AVT10AC	i.MX 6Quad	Includes GPU, no VPU	1 GHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6Q4AVT10AD	i.MX 6Quad	Includes GPU, no VPU	1 GHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6Q4AVT10AE	i.MX 6Quad	Includes GPU, no VPU	1 GHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6Q6AVT08AC	i.MX 6Quad	Includes VPU, GPU	852 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6Q6AVT08AD	i.MX 6Quad	Includes VPU, GPU	852 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6Q6AVT08AE	i.MX 6Quad	Includes VPU, GPU	852 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6Q4AVT08AC	i.MX 6Quad	Includes GPU, no VPU	852 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6Q4AVT08AD	i.MX 6Quad	Includes GPU, no VPU	852 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6Q4AVT08AE	i.MX 6Quad	Includes GPU, no VPU	852 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6D6AVT10AC	i.MX 6Dual	Includes VPU, GPU	1 GHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6D6AVT10AD	i.MX 6Dual	Includes VPU, GPU	1 GHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6D6AVT10AE	i.MX 6Dual	Includes VPU, GPU	1 GHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6D4AVT10AC	i.MX 6Dual	Includes GPU, no VPU	1 GHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6D4AVT10AD	i.MX 6Dual	Includes GPU, no VPU	1 GHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)

2 Architectural Overview

The following subsections provide an architectural overview of the i.MX 6Dual/6Quad processor system.

2.1 Block Diagram

Figure 2 shows the functional modules in the i.MX 6Dual/6Quad processor system.

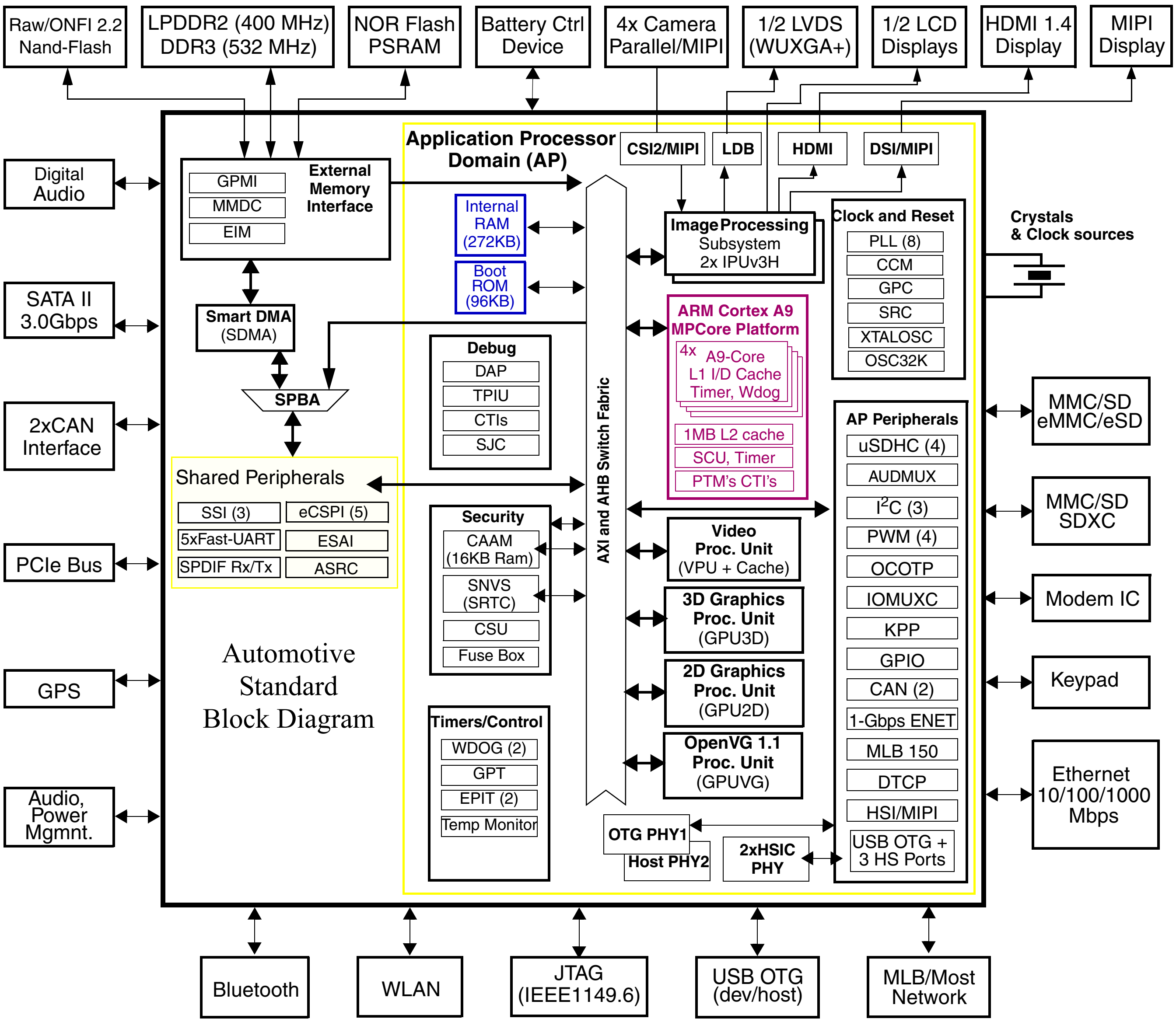


Figure 2. i.MX 6Dual/6Quad Automotive Grade System Block Diagram

NOTE

The numbers in brackets indicate number of module instances. For example, PWM (4) indicates four separate PWM peripherals.

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SSI-1 SSI-2 SSI-3	I2S/SSI/AC97 Interface	Connectivity Peripherals	The SSI is a full-duplex synchronous interface, which is used on the processor to provide connectivity with off-chip audio peripherals. The SSI supports a wide variety of protocols (SSI normal, SSI network, I2S, and AC-97), bit depths (up to 24 bits per word), and clock / frame sync options. The SSI has two pairs of 8x24 FIFOs and hardware support for an external DMA controller to minimize its impact on system performance. The second pair of FIFOs provides hardware interleaving of a second audio stream that reduces CPU overhead in use cases where two time slots are being used simultaneously.
TEMPMON	Temperature Monitor	System Control Peripherals	The temperature monitor/sensor IP module for detecting high temperature conditions. The temperature read out does not reflect case or ambient temperature. It reflects the temperature in proximity of the sensor location on the die. Temperature distribution may not be uniformly distributed; therefore, the read out value may not be the reflection of the temperature value for the entire die.
TZASC	Trust-Zone Address Space Controller	Security	The TZASC (TZC-380 by ARM) provides security address region control functions required for intended application. It is used on the path to the DRAM controller.
UART-1 UART-2 UART-3 UART-4 UART-5	UART Interface	Connectivity Peripherals	Each of the UARTv2 modules support the following serial data transmit/receive protocols and configurations: • 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none) • Programmable baud rates up to 5 MHz • 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud • IrDA 1.0 support (up to SIR speed of 115200 bps) • Option to operate as 8-pins full UART, DCE, or DTE
USBOH3A	USB 2.0 High Speed OTG and 3x HS Hosts	Connectivity Peripherals	USBOH3 contains: • One high-speed OTG module with integrated HS USB PHY • One high-speed Host module with integrated HS USB PHY • Two identical high-speed Host modules connected to HSIC USB ports.

10 All digital I/O supplies (NVCC_xxxx) must be powered under normal conditions whether the associated I/O pins are in use or not, and associated I/O pins need to have a pull-up or pull-down resistor applied to limit any floating gate current.

11 This supply also powers the pre-drivers of the DDR I/O pins; therefore, it must always be provided, even when LVDS is not used.

4.1.4 External Clock Sources

Each i.MX 6Dual/6Quad processor has two external input system clocks: a low frequency (RTC_XTALI) and a high frequency (XTALI).

The RTC_XTALI is used for low-frequency functions. It supplies the clock for wake-up circuit, power-down real time clock operation, and slow system and watchdog counters. The clock input can be connected to either an external oscillator or a crystal using the internal oscillator amplifier. Additionally, there is an internal ring oscillator, that can be used instead of RTC_XTALI when accuracy is not important.

The system clock input XTALI is used to generate the main system clock. It supplies the PLLs and other peripherals. The system clock input can be connected to either an external oscillator or a crystal using the internal oscillator amplifier.

NOTE

The internal RTC oscillator does not provide an accurate frequency and is affected by process, voltage and temperature variations. NXP strongly recommends using an external crystal as the RTC_XTALI reference. If the internal oscillator is used instead, careful consideration should be given to the timing implications on all of the SoC modules dependent on this clock.

Table 7 shows the interface frequency requirements.

Table 7. External Input Clock Frequency

Parameter Description	Symbol	Min	Typ	Max	Unit
RTC_XTALI Oscillator[1,2]	f_{ckil}	—	32.768[3]/32.0	—	kHz
XTALI Oscillator[4,2]	f_{xtal}	—	24	—	MHz

1 External oscillator or a crystal with internal oscillator amplifier.

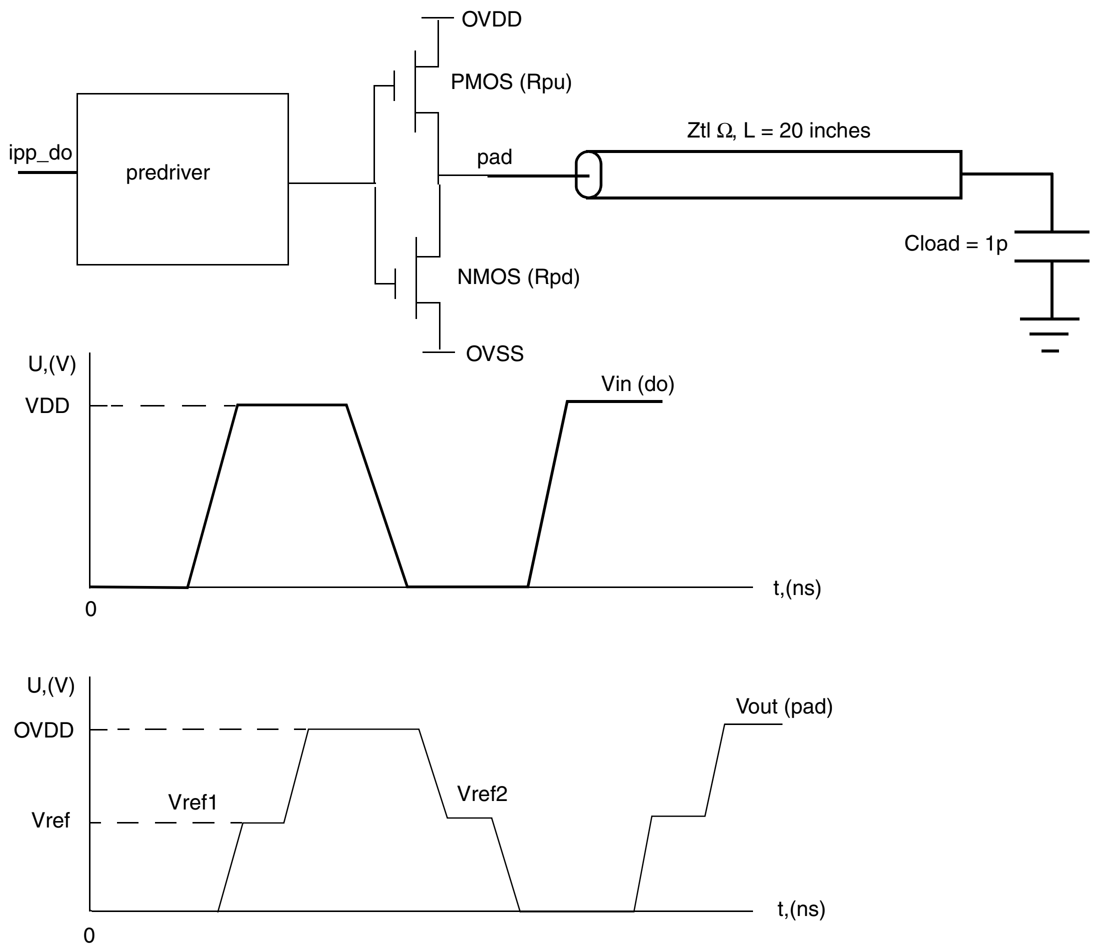
2 The required frequency stability of this clock source is application dependent. For recommendations, see the Hardware Development Guide for i.MX 6Dual, 6Quad, 6Solo, 6DualLite Families of Applications Processors (IMX6DQ6SDLHDG).

3 Recommended nominal frequency 32.768 kHz.

4 External oscillator or a fundamental frequency crystal with internal oscillator amplifier.

The typical values shown in Table 7 are required for use with NXP BSPs to ensure precise time keeping and USB operation. For RTC_XTALI operation, two clock sources are available:

- On-chip 40 kHz ring oscillator: This clock source has the following characteristics:
  - Approximately 25 µA more Idd than crystal oscillator
  - Approximately ±50% tolerance
  - No external component required
  - Starts up quicker than 32 kHz crystal oscillator
- External crystal oscillator with on-chip support circuit



$$\text{Rpu} = \frac{\text{Vovdd} - \text{Vref1}}{\text{Vref1}} \times \text{Ztl}$$

$$\text{Rpd} = \frac{\text{Vref2}}{\text{Vovdd} - \text{Vref2}} \times \text{Ztl}$$

Figure 9. Impedance Matching Load for Measurement

4.9.3.4 General EIM Timing-Asynchronous Mode

Figure 18 through Figure 22 and Table 42 provide timing parameters relative to the chip select (CS) state for asynchronous and DTACK EIM accesses with corresponding EIM bit fields and the timing parameters mentioned above.

Asynchronous read and write access length in cycles may vary from what is shown in Figure 18 through Figure 21 as RWSC, OEN & CSN is configured differently. See the i.MX 6Dual/6Quad reference manual (IMX6DQRM) for the EIM programming model.

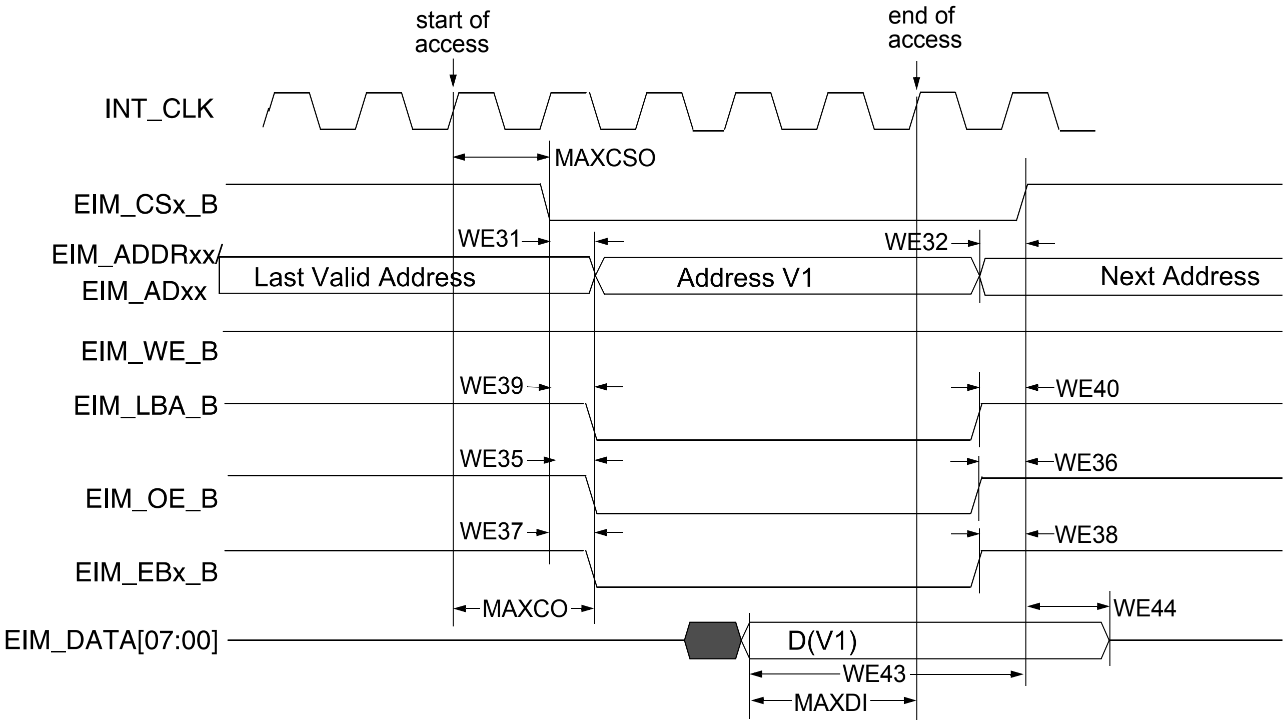


Figure 18. Asynchronous Memory Read Access (RWSC = 5)

Table 44. Asynchronous Mode Timing Parameters[1] (continued)

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min	Max	
NF16	Data setup on read	tDSR	—	(DS × T -0.67)/18.38 [see [5,6]]	ns
NF17	Data hold on read	tDHR	0.82/11.83 [see [5,6]]	—	ns

1 The GPMI asynchronous mode output timing can be controlled by the module's internal registers HW_GPMI_TIMING0_ADDRESS_SETUP, HW_GPMI_TIMING0_DATA_SETUP, and HW_GPMI_TIMING0_DATA_HOLD. This AC timing depends on these registers settings. In the table, AS/DS/DH represents each of these settings.

2 AS minimum value can be 0, while DS/DH minimum value is 1.

3 T = GPMI clock period -0.075ns (half of maximum p-p jitter).

4 NF12 is met automatically by the design.

5 Non-EDO mode.

6 EDO mode, GPMI clock ≈ 100 MHz
(AS=DS=DH=1, GPMI_CTL1 [RDN_DELAY] = 8, GPMI_CTL1 [HALF_PERIOD] = 0).

In EDO mode (Figure 28), NF16/NF17 are different from the definition in non-EDO mode (Figure 27). They are called tREA/tRHOH (NAND_RE_B access time/NAND_RE_B HIGH to output hold). The typical value for them are 16 ns (max for tREA)/15 ns (min for tRHOH) at 50 MB/s EDO mode. In EDO mode, GPMI will sample NAND_DATAxx at rising edge of delayed NAND_RE_B provided by an internal DPLL. The delay value can be controlled by GPMI_CTRL1.RDN_DELAY (see the GPMI chapter of the i.MX 6Dual/6Quad reference manual (IMX6DQRM)). The typical value of this control register is 0x8 at 50 MT/s EDO mode. However, if the board delay is large enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

4.12.4 Ultra High Speed SD/SDIO/MMC Host Interface (uSDHC) AC Timing

This section describes the electrical information of the uSDHC, which includes SD/eMMC4.3 (Single Data Rate) timing and eMMC4.4/4.1 (Dual Date Rate) timing.

4.12.4.1 SD/eMMC4.3 (Single Data Rate) AC Timing

Figure 39 depicts the timing of SD/eMMC4.3, and Table 50 lists the SD/eMMC4.3 timing characteristics.

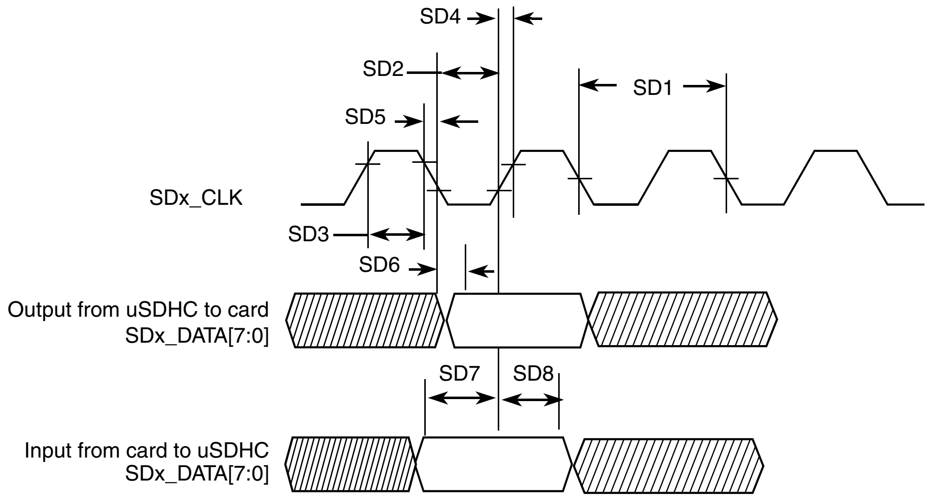


Figure 39. SD/eMMC4.3 Timing

Table 50. SD/eMMC4.3 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (Low Speed)	f_{PP}[1]	0	400	kHz
	Clock Frequency (SD/SDIO Full Speed/High Speed)	f_{PP}[2]	0	25/50	MHz
	Clock Frequency (MMC Full Speed/High Speed)	f_{PP}[3]	0	20/52	MHz
	Clock Frequency (Identification Mode)	f_{OD}	100	400	kHz
SD2	Clock Low Time	t_{WL}	7	—	ns
SD3	Clock High Time	t_{WH}	7	—	ns
SD4	Clock Rise Time	t_{TLH}	—	3	ns
SD5	Clock Fall Time	t_{THL}	—	3	ns
eSDHC Output/Card Inputs SD_CMD, SD_DATAx (Reference to SDx_CLK)					
SD6	eSDHC Output Delay	t_{OD}	–6.6	3.6	ns

Table 61. I2C Module Timing Parameters (continued)

ID	Parameter	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
IC9	Bus free time between a STOP and START condition	4.7	—	1.3	—	µs
IC10	Rise time of both I2Cx_SDA and I2Cx_SCL signals	—	1000	$20 + 0.1C_b$[4]	300	ns
IC11	Fall time of both I2Cx_SDA and I2Cx_SCL signals	—	300	$20 + 0.1C_b$[4]	300	ns
IC12	Capacitive load for each bus line (C_b)	—	400	—	400	pF

1 A device must internally provide a hold time of at least 300 ns for I2Cx_SDA signal to bridge the undefined region of the falling edge of I2Cx_SCL.

2 The maximum hold time has only to be met if the device does not stretch the LOW period (ID no IC5) of the I2Cx_SCL signal.

3 A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement of Set-up time (ID No IC7) of 250 ns must be met. This automatically is the case if the device does not stretch the LOW period of the I2Cx_SCL signal. If such a device does stretch the LOW period of the I2Cx_SCL signal, it must output the next data bit to the I2Cx_SDA line max_rise_time (IC9) + data_setup_time (IC7) = 1000 + 250 = 1250 ns (according to the Standard-mode I2C-bus specification) before the I2Cx_SCL line is released.

4 C_b = total capacitance of one bus line in pF.

4.12.10 Image Processing Unit (IPU) Module Parameters

The purpose of the IPU is to provide comprehensive support for the flow of data from an image sensor and/or to a display device. This support covers all aspects of these activities:

- Connectivity to relevant devices—cameras, displays, graphics accelerators, and TV encoders.
- Related image processing and manipulation: sensor image signal processing, display processing, image conversions, and other related functions.
- Synchronization and control capabilities, such as avoidance of tearing artifacts.

4.12.10.1 IPU Sensor Interface Signal Mapping

The IPU supports a number of sensor input formats. Table 62 defines the mapping of the Sensor Interface Pins used for various supported interface formats.

Table 62. Camera Input Signal Cross Reference, Format, and Bits Per Cycle

Signal Name[1]	RGB565 8 bits 2 cycles	RGB565[2] 8 bits 3 cycles	RGB666[3] 8 bits 3 cycles	RGB888 8 bits 3 cycles	YCbCr[4] 8 bits 2 cycles	RGB565[5] 16 bits 1 cycle	YCbCr[6] 16 bits 1 cycle	YCbCr[7] 16 bits 1 cycle	YCbCr[8] 20 bits 1 cycle
IPUx_CSIx_ DATA00	—	—	—	—	—	—	—	0	C[0]
IPUx_CSIx_ DATA01	—	—	—	—	—	—	—	0	C[1]
IPUx_CSIx_ DATA02	—	—	—	—	—	—	—	C[0]	C[2]
IPUx_CSIx_ DATA03	—	—	—	—	—	—	—	C[1]	C[3]
IPUx_CSIx_ DATA04	—	—	—	—	—	B[0]	C[0]	C[2]	C[4]
IPU2_CSIx_ DATA_05	—	—	—	—	—	B[1]	C[1]	C[3]	C[5]
IPUx_CSIx_ DATA06	—	—	—	—	—	B[2]	C[2]	C[4]	C[6]
IPUx_CSIx_ DATA07	—	—	—	—	—	B[3]	C[3]	C[5]	C[7]
IPUx_CSIx_ DATA08	—	—	—	—	—	B[4]	C[4]	C[6]	C[8]
IPUx_CSIx_ DATA09	—	—	—	—	—	G[0]	C[5]	C[7]	C[9]
IPUx_CSIx_ DATA10	—	—	—	—	—	G[1]	C[6]	0	Y[0]
IPUx_CSIx_ DATA11	—	—	—	—	—	G[2]	C[7]	0	Y[1]
IPUx_CSIx_ DATA12	B[0], G[3]	R[2],G[4],B[2]	R/G/B[4]	R/G/B[0]	Y/C[0]	G[3]	Y[0]	Y[0]	Y[2]
IPUx_CSIx_ DATA13	B[1], G[4]	R[3],G[5],B[3]	R/G/B[5]	R/G/B[1]	Y/C[1]	G[4]	Y[1]	Y[1]	Y[3]
IPUx_CSIx_ DATA14	B[2], G[5]	R[4],G[0],B[4]	R/G/B[0]	R/G/B[2]	Y/C[2]	G[5]	Y[2]	Y[2]	Y[4]
IPUx_CSIx_ DATA15	B[3], R[0]	R[0],G[1],B[0]	R/G/B[1]	R/G/B[3]	Y/C[3]	R[0]	Y[3]	Y[3]	Y[5]
IPUx_CSIx_ DATA16	B[4], R[1]	R[1],G[2],B[1]	R/G/B[2]	R/G/B[4]	Y/C[4]	R[1]	Y[4]	Y[4]	Y[6]
IPUx_CSIx_ DATA17	G[0], R[2]	R[2],G[3],B[2]	R/G/B[3]	R/G/B[5]	Y/C[5]	R[2]	Y[5]	Y[5]	Y[7]
IPUx_CSIx_ DATA18	G[1], R[3]	R[3],G[4],B[3]	R/G/B[4]	R/G/B[6]	Y/C[6]	R[3]	Y[6]	Y[6]	Y[8]
IPUx_CSIx_ DATA19	G[2], R[4]	R[4],G[5],B[4]	R/G/B[5]	R/G/B[7]	Y/C[7]	R[4]	Y[7]	Y[7]	Y[9]

[1] IPU2_CSIx stands for IPU2_CSI1 or IPU2_CSI2.

Table 64. Video Signal Cross-Reference (continued)

i.MX 6Dual/6Quad	LCD							Comment[1,2]
Port Name (x = 0, 1)	RGB, Signal Name (General)	RGB/TV Signal Allocation (Example)						
		16-bit RGB	18-bit RGB	24 Bit RGB	8-bit YCrCb[3]	16-bit YCrCb	20-bit YCrCb	
IPUx_DIx_PIN04	—							Additional frame/row synchronous signals with programmable timing
IPUx_DIx_PIN05	—							
IPUx_DIx_PIN06	—							
IPUx_DIx_PIN07	—							
IPUx_DIx_PIN08	—							
IPUx_DIx_D0_CS	—							—
IPUx_DIx_D1_CS	—							Alternate mode of PWM output for contrast or brightness control
IPUx_DIx_PIN11	—							—
IPUx_DIx_PIN12	—							—
IPUx_DIx_PIN13	—							Register select signal
IPUx_DIx_PIN14	—							Optional RS2
IPUx_DIx_PIN15	DRDY/DV							Data validation/blank, data enable
IPUx_DIx_PIN16	—							Additional data synchronous signals with programmable features/timing
IPUx_DIx_PIN17	Q							

1 Signal mapping (both data and control/synchronization) is flexible. The table provides examples.

2 Restrictions for ports IPUx_DISPx_DAT00 through IPUx_DISPx_DAT23 are as follows:
- A maximum of three continuous groups of bits can be independently mapped to the external bus. Groups must not overlap.
- The bit order is expressed in each of the bit groups, for example, B[0] = least significant blue pixel bit.

3 This mode works in compliance with recommendation ITU-R BT.656. The timing reference signals (frame start, frame end, line start, and line end) are embedded in the 8-bit data bus. Only video data is supported, transmission of non-video related data during blanking intervals is not supported.

NOTE

Table 64 provides information for both the DISP0 and DISP1 ports. However, DISP1 port has reduced pinout depending on IOMUXC configuration and therefore may not support all configurations. See the IOMUXC table for details.

4.12.10.5 IPU Display Interface Timing

The IPU Display Interface supports two kinds of display accesses: synchronous and asynchronous. There are two groups of external interface pins to provide synchronous and asynchronous controls.

4.12.10.5.1 Synchronous Controls

The synchronous control changes its value as a function of a system or of an external clock. This control has a permanent period and a permanent waveform.

4.12.11 LVDS Display Bridge (LDB) Module Parameters

The LVDS interface complies with TIA/EIA 644-A standard. For more details, see TIA/EIA STANDARD 644-A, “Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits.”

Table 67. LVDS Display Bridge (LDB) Electrical Specification

Parameter	Symbol	Test Condition	Min	Max	Units
Differential Voltage Output Voltage	V_{OD}	100 Ω Differential load	250	450	mV
Output Voltage High	Voh	100 Ω differential load (0 V Diff—Output High Voltage static)	1.25	1.6	V
Output Voltage Low	Vol	100 Ω differential load (0 V Diff—Output Low Voltage static)	0.9	1.25	V
Offset Static Voltage	V_{OS}	Two 49.9 Ω resistors in series between N-P terminal, with output in either Zero or One state, the voltage measured between the 2 resistors.	1.15	1.375	V
VOS Differential	V_{OSDIFF}	Difference in V_{OS} between a One and a Zero state	-50	50	mV
Output short-circuited to GND	ISA ISB	With the output common shorted to GND	-24	24	mA
VT Full Load Test	VTLoad	100 Ω Differential load with a 3.74 kΩ load between GND and I/O supply voltage	247	454	mV

4.12.12 MIPI D-PHY Timing Parameters

This section describes MIPI D-PHY electrical specifications, compliant with MIPI CSI-2 version 1.0, D-PHY specification Rev. 1.0 (for MIPI sensor port x4 lanes) and MIPI DSI Version 1.01, and D-PHY specification Rev. 1.0 (and also DPI version 2.0, DBI version 2.0, DSC version 1.0a at protocol layer) (for MIPI display port x2 lanes).

4.12.12.1 Electrical and Timing Information

Table 68. Electrical and Timing Information

Symbol	Parameters	Test Conditions	Min	Typ	Max	Unit
Input DC Specifications—Apply to DSI_CLK_P/_N and DSI_DATA_P/_N Inputs						
V_I	Input signal voltage range	Transient voltage range is limited from -300 mV to 1600 mV	-50	—	1350	mV
V_{LEAK}	Input leakage current	VGNDSH(min) = VI = VGNDSH(max) + VOH(absmax) Lane module in LP Receive Mode	-10	—	10	mA
V_{GNDSH}	Ground Shift	—	-50	—	50	mV
$V_{OH(absmax)}$	Maximum transient output voltage level	—	—	—	1.45	V
$t_{voh(absmax)}$	Maximum transient time above VOH(absmax)	—	—	—	20	ns

4.12.12.9 Low-Power Receiver Timing

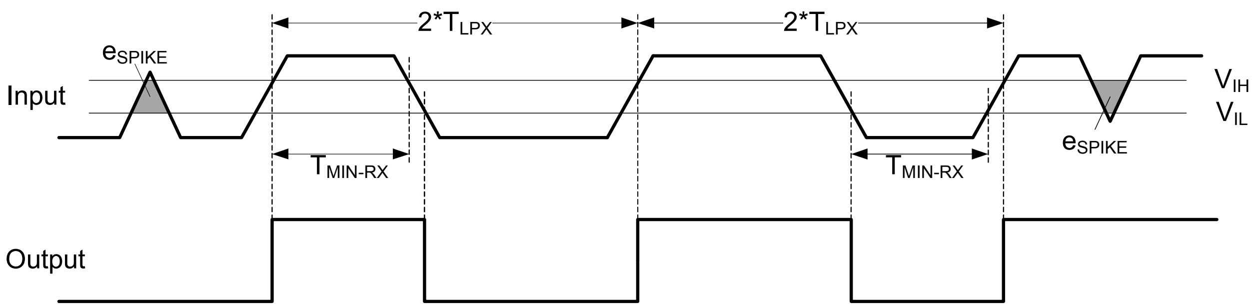


Figure 72. Input Glitch Rejection of Low-Power Receivers

4.12.13 HSI Host Controller Timing Parameters

This section describes the timing parameters of the HSI Host Controller which are compliant with High-Speed Synchronous Serial Interface (HSI) Physical Layer specification version 1.01.

4.12.13.1 Synchronous Data Flow

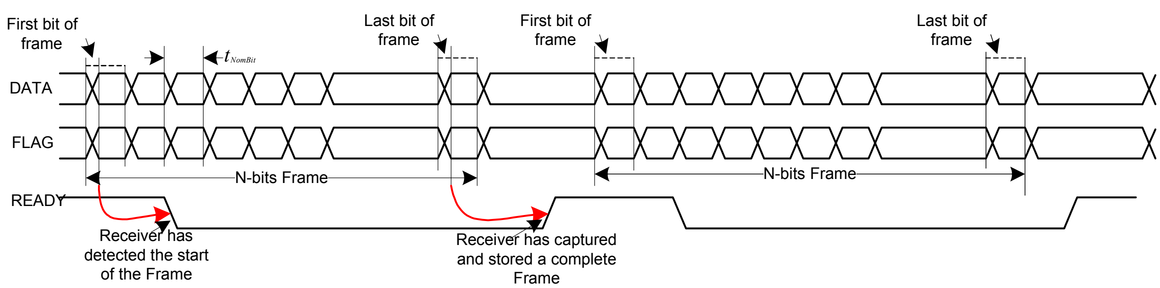


Figure 73. Synchronized Data Flow READY Signal Timing (Frame and Stream Transmission)

4.12.13.2 Pipelined Data Flow

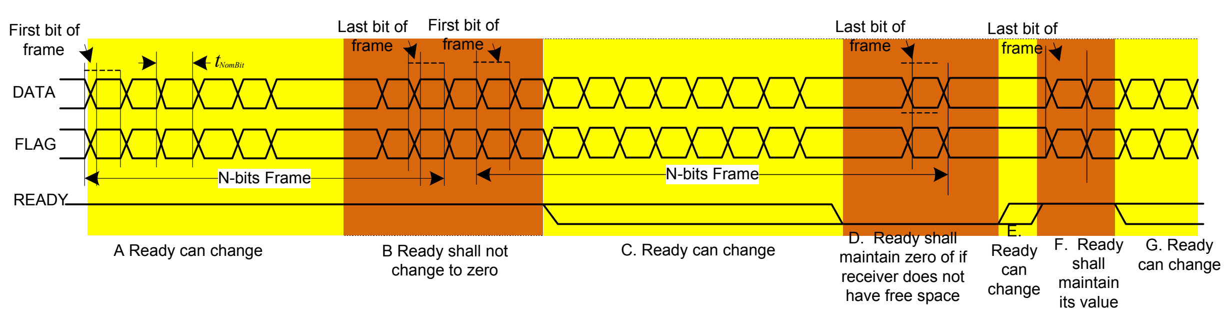


Figure 74. Pipelined Data Flow READY Signal Timing (Frame Transmission Mode)

4.12.21.2.3 UART IrDA Mode Timing

The following subsections give the UART transmit and receive timings in IrDA mode.

UART IrDA Mode Transmitter

Figure 96 depicts the UART IrDA mode transmit timing, with 8 data bit/1 stop bit format. Table 89 lists the transmit timing characteristics.

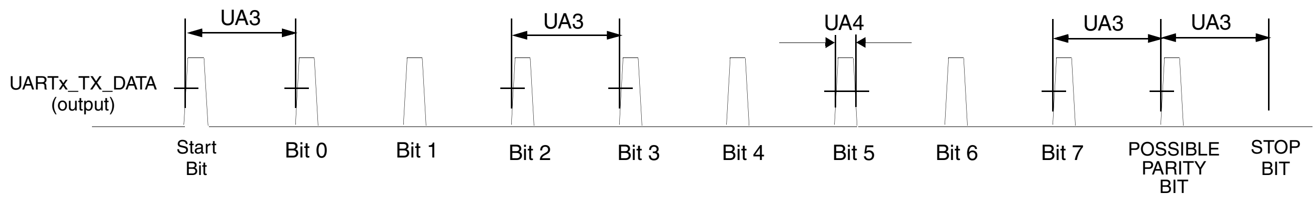


Figure 96. UART IrDA Mode Transmit Timing Diagram

Table 89. IrDA Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA3	Transmit Bit Time in IrDA mode	t_{TIRbit}	$1/F_{baud\_rate}$[1] $- T_{ref\_clk}$[2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—
UA4	Transmit IR Pulse Duration	$t_{TIRpulse}$	$(3/16) \times (1/F_{baud\_rate}) - T_{ref\_clk}$	$(3/16) \times (1/F_{baud\_rate}) + T_{ref\_clk}$	—

1 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.
2 T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

UART IrDA Mode Receiver

Figure 97 depicts the UART IrDA mode receive timing, with 8 data bit/1 stop bit format. Table 90 lists the receive timing characteristics.

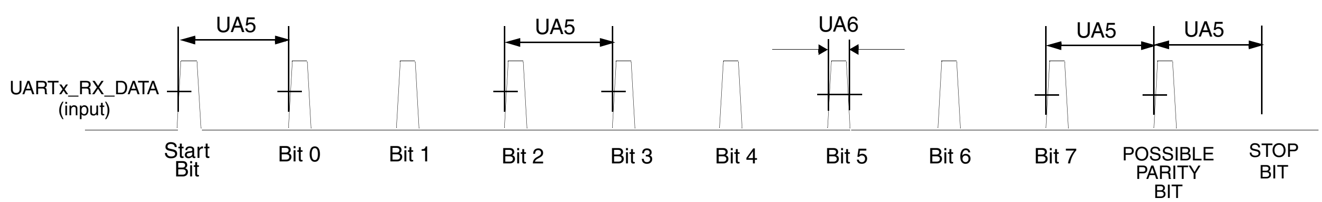


Figure 97. UART IrDA Mode Receive Timing Diagram

Table 90. IrDA Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA5	Receive Bit Time[1] in IrDA mode	t_{RIRbit}	$1/F_{baud\_rate}$[2] $-$ $1/(16 \times F_{baud\_rate})$	$1/F_{baud\_rate} +$ $1/(16 \times F_{baud\_rate})$	—
UA6	Receive IR Pulse Duration	$t_{RIRpulse}$	1.41 µs	$(5/16) \times (1/F_{baud\_rate})$	—

1 The UART receiver can tolerate $1/(16 \times F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud\_rate})$.
2 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

Table 94. Interfaces Allocation During Boot (continued)

Interface	IP Instance	Allocated Pads During Boot	Comment
NAND Flash	GPMI	NANDF_CLE, NANDF_ALE, NANDF_WP_B, SD4_CMD, SD4_CLK, NANDF_RB0, SD4_DAT0, NANDF_CS0, NANDF_CS1, NANDF_CS2, NANDF_CS3, NANDF_D[7:0]	8 bit Only CS0 is supported
SD/MMC	USDHC-1	SD1_CLK, SD1_CMD,SD1_DAT0, SD1_DAT1, SD1_DAT2, SD1_DAT3, NANDF_D0, NANDF_D1, NANDF_D2, NANDF_D3, KEY_COL1	1, 4, or 8 bit
SD/MMC	USDHC-2	SD2_CLK, SD2_CMD, SD2_DAT0, SD2_DAT1, SD2_DAT2, SD2_DAT3, NANDF_D4, NANDF_D5, NANDF_D6, NANDF_D7, KEY_ROW1	1, 4, or 8 bit
SD/MMC	USDHC-3	SD3_CLK, SD3_CMD, SD3_DAT0, SD3_DAT1, SD3_DAT2, SD3_DAT3, SD3_DAT4, SD3_DAT5, SD3_DAT6, SD3_DAT7, GPIO_18	1, 4, or 8 bit
SD/MMC	USDHC-4	SD4_CLK, SD4_CMD, SD4_DAT0, SD4_DAT1, SD4_DAT2, SD4_DAT3, SD4_DAT4, SD4_DAT5, SD4_DAT6, SD4_DAT7, NANDF_CS1	1, 4, or 8 bit
I2C	I2C-1	EIM_D28, EIM_D21	—
I2C	I2C-2	EIM_D16, EIM_EB2	—
I2C	I2C-3	EIM_D18, EIM_D17	—
SATA	SATA_PHY	SATA_TXM, SATA_TXP, SATA_RXP, SATA_RXM, SATA_REXT	—
USB	USB-OTG PHY	USB_OTG_DP USB_OTG_DN USB_OTG_VBUS	—

6 Package Information and Contact Assignments

This section includes the contact assignment information and mechanical package drawing.

6.1 Signal Naming Convention

The signal names of the i.MX6 series of products are standardized to align the signal names within the family and across the documentation. Benefits of this standardization are as follows:

- Signal names are unique within the scope of an SoC and within the series of products
- Searches will return all occurrences of the named signal
- Signal names are consistent between i.MX 6 series products implementing the same modules
- The module instance is incorporated into the signal name

This standardization applies only to signal names. The ball names are preserved to prevent the need to change schematics, BSDL models, IBIS models, and so on.

Throughout this document, the signal names are used except where referenced as a ball name (such as the Functional Contact Assignments table, Ball Map table, and so on). A master list of signal names is in the document, *IMX 6 Series Standardized Signal Name Map* (EB792). This list can be used to map the signal names used in older documentation to the standardized naming conventions.

6.2 21 x 21 mm Package Information

6.2.1 Case FCPBGA, 21 x 21 mm, 0.8 mm Pitch, 25 x 25 Ball Matrix

Table 95. 21 x 21 mm Supplies Contact Assignment (continued)

Supply Rail Name	Ball(s) Position(s)	Remark
NVCC_MIPI	K7	Supply of the MIPI interface
NVCC_NANDF	G15	Supply of the RAW NAND Flash Memories interface
NVCC_PLL_OUT	E8	—
NVCC_RGMII	G18	Supply of the ENET interface
NVCC_SD1	G16	Supply of the SD card interface
NVCC_SD2	G17	Supply of the SD card interface
NVCC_SD3	G14	Supply of the SD card interface
PCIE_VP	H7	—
PCIE_REXT	A2	—
PCIE_VPH	G7	PCI PHY supply
PCIE_VPTX	G8	PCI PHY supply
SATA_REXT	C14	—
SATA_VP	G13	—
SATA_VPH	G12	—
USB_H1_VBUS	D10	—
USB_OTG_VBUS	E9	—
VDD_CACHE_CAP	N12	Cache supply input. This input should be connected to (driven by) VDD_SOC_CAP. The external capacitor used for VDD_SOC_CAP is sufficient for this supply.
VDD_FA	B5	—
VDD_SNVS_CAP	G9	Secondary supply for the SNVS (internal regulator output—requires capacitor if internal regulator is used)
VDD_SNVS_IN	G11	Primary supply for the SNVS regulator
VDDARM_CAP	H13, J13, K13, L13, M13, N13, P13, R13	Secondary supply for the ARM0 and ARM1 cores (internal regulator output—requires capacitor if internal regulator is used)
VDDARM_IN	H14, J14, K14, L14, M14, N14, P14, R14	Primary supply for the ARM0 and ARM1 core regulator
VDDARM23_CAP	H11, J11, K11, L11, M11, N11, P11, R11	Secondary supply for the ARM2 and ARM3 cores (internal regulator output—requires capacitor if internal regulator is used)
VDDARM23_IN	K9, L9, M9, N9, P9, R9, T9, U9	Primary supply for the ARM2 and ARM3 core regulator

Table 95. 21 x 21 mm Supplies Contact Assignment (continued)

Supply Rail Name	Ball(s) Position(s)	Remark
VDDHIGH_CAP	H10, J10	Secondary supply for the 2.5 V domain (internal regulator output—requires capacitor if internal regulator is used)
VDDHIGH_IN	H9, J9	Primary supply for the 2.5 V regulator
VDDPU_CAP	H17, J17, K17, L17, M17, N17, P17	Secondary supply for the VPU and GPU (internal regulator output—requires capacitor if internal regulator is used)
VDDSOC_CAP	R10, T10, T13, T14, U10, U13, U14	Secondary supply for the SoC and PU (internal regulator output—requires capacitor if internal regulator is used)
VDDSOC_IN	H16, J16, K16, L16, M16, N16, P16, R16, T16, U16	Primary supply for the SoC and PU regulators
VDDUSB_CAP	F9	Secondary supply for the 3 V domain (internal regulator output—requires capacitor if internal regulator is used)
ZQPAD	AE17	Connect ZQPAD to an external 240Ω 1% resistor to GND. This is a reference used during DRAM output buffer driver calibration.

6.2.3 21 x 21 mm Functional Contact Assignments

Table 96 displays an alpha-sorted list of the signal assignments including power rails. The table also includes out of reset pad state.

Table 96. 21 x 21 mm Functional Contact Assignments

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function (Signal Name)	Input/Output	Value[2]
BOOT_MODE0	C12	VDD_SNVS_IN	GPIO	ALT0	SRC_BOOT_MODE0	Input	PD (100K)
BOOT_MODE1	F12	VDD_SNVS_IN	GPIO	ALT0	SRC_BOOT_MODE1	Input	PD (100K)
CLK1_N	C7	VDD_HIGH_CAP	—	—	CLK1_N	—	—
CLK1_P	D7	VDD_HIGH_CAP	—	—	CLK1_P	—	—
CLK2_N	C5	VDD_HIGH_CAP	—	—	CLK2_N	—	—
CLK2_P	D5	VDD_HIGH_CAP	—	—	CLK2_P	—	—
CSI_CLK0M	F4	NVCC_MIPI	—	—	CSI_CLK_N	—	—
CSI_CLK0P	F3	NVCC_MIPI	—	—	CSI_CLK_P	—	—
CSI_D0M	E4	NVCC_MIPI	—	—	CSI_DATA0_N	—	—
CSI_D0P	E3	NVCC_MIPI	—	—	CSI_DATA0_P	—	—
CSI_D1M	D1	NVCC_MIPI	—	—	CSI_DATA1_N	—	—

Table 96. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function (Signal Name)	Input/Output	Value[2]
DRAM_DQM7	Y21	NVCC_DRAM	DDR	ALT0	DRAM_DQM7	Output	0
DRAM_RAS	AB15	NVCC_DRAM	DDR	ALT0	DRAM_RAS_B	Output	0
DRAM_RESET	Y6	NVCC_DRAM	DDR	ALT0	DRAM_RESET	Output	0
DRAM_SDBA0	AC15	NVCC_DRAM	DDR	ALT0	DRAM_SDBA0	Output	0
DRAM_SDBA1	Y15	NVCC_DRAM	DDR	ALT0	DRAM_SDBA1	Output	0
DRAM_SDBA2	AB12	NVCC_DRAM	DDR	ALT0	DRAM_SDBA2	Output	0
DRAM_SDCKE0	Y11	NVCC_DRAM	DDR	ALT0	DRAM_SDCKE0	Output	0
DRAM_SDCKE1	AA11	NVCC_DRAM	DDR	ALT0	DRAM_SDCKE1	Output	0
DRAM_SDCLK_0	AD15	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDCLK0_P	Output	0
DRAM_SDCLK_0_B	AE15	NVCC_DRAM	DDRCLK	—	DRAM_SDCLK0_N	—	—
DRAM_SDCLK_1	AD14	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDCLK1_P	Output	0
DRAM_SDCLK_1_B	AE14	NVCC_DRAM	DDRCLK	—	DRAM_SDCLK1_N	—	—
DRAM_SDODT0	AC16	NVCC_DRAM	DDR	ALT0	DRAM_ODT0	Output	0
DRAM_SDODT1	AB17	NVCC_DRAM	DDR	ALT0	DRAM_ODT1	Output	0
DRAM_SDQS0	AE3	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS0_P	Input	Hi-Z
DRAM_SDQS0_B	AD3	NVCC_DRAM	DDRCLK	—	DRAM_SDQS0_N	—	—
DRAM_SDQS1	AD6	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS1_P	Input	Hi-Z
DRAM_SDQS1_B	AE6	NVCC_DRAM	DDRCLK	—	DRAM_SDQS1_N	—	—
DRAM_SDQS2	AD8	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS2_P	Input	Hi-Z
DRAM_SDQS2_B	AE8	NVCC_DRAM	DDRCLK	—	DRAM_SDQS2_N	—	—
DRAM_SDQS3	AC10	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS3_P	Input	Hi-Z
DRAM_SDQS3_B	AB10	NVCC_DRAM	DDRCLK	—	DRAM_SDQS3_N	—	—
DRAM_SDQS4	AD18	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS4_P	Input	Hi-Z
DRAM_SDQS4_B	AE18	NVCC_DRAM	DDRCLK	—	DRAM_SDQS4_N	—	—
DRAM_SDQS5	AD20	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS5_P	Input	Hi-Z
DRAM_SDQS5_B	AE20	NVCC_DRAM	DDRCLK	—	DRAM_SDQS5_N	—	—
DRAM_SDQS6	AD23	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS6_P	Input	Hi-Z
DRAM_SDQS6_B	AE23	NVCC_DRAM	DDRCLK	—	DRAM_SDQS6_N	—	—
DRAM_SDQS7	AA25	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS7_P	Input	Hi-Z
DRAM_SDQS7_B	AA24	NVCC_DRAM	DDRCLK	—	DRAM_SDQS7_N	—	—
DRAM_SDWE	AB16	NVCC_DRAM	DDR	ALT0	DRAM_SDWE_B	Output	0
DSI_CLK0M	H3	NVCC_MIPI	—	—	DSI_CLK_N	—	—
DSI_CLK0P	H4	NVCC_MIPI	—	—	DSI_CLK_P	—	—
DSI_D0M	G2	NVCC_MIPI	—	—	DSI_DATA0_N	—	—
DSI_D0P	G1	NVCC_MIPI	—	—	DSI_DATA0_P	—	—
DSI_D1M	H2	NVCC_MIPI	—	—	DSI_DATA1_N	—	—

Table 96. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function (Signal Name)	Input/Output	Value[2]
SD2_DAT0	A22	NVCC_SD2	GPIO	ALT5	GPIO1_IO15	Input	PU (100K)
SD2_DAT1	E20	NVCC_SD2	GPIO	ALT5	GPIO1_IO14	Input	PU (100K)
SD2_DAT2	A23	NVCC_SD2	GPIO	ALT5	GPIO1_IO13	Input	PU (100K)
SD2_DAT3	B22	NVCC_SD2	GPIO	ALT5	GPIO1_IO12	Input	PU (100K)
SD3_CLK	D14	NVCC_SD3	GPIO	ALT5	GPIO7_IO03	Input	PU (100K)
SD3_CMD	B13	NVCC_SD3	GPIO	ALT5	GPIO7_IO02	Input	PU (100K)
SD3_DAT0	E14	NVCC_SD3	GPIO	ALT5	GPIO7_IO04	Input	PU (100K)
SD3_DAT1	F14	NVCC_SD3	GPIO	ALT5	GPIO7_IO05	Input	PU (100K)
SD3_DAT2	A15	NVCC_SD3	GPIO	ALT5	GPIO7_IO06	Input	PU (100K)
SD3_DAT3	B15	NVCC_SD3	GPIO	ALT5	GPIO7_IO07	Input	PU (100K)
SD3_DAT4	D13	NVCC_SD3	GPIO	ALT5	GPIO7_IO01	Input	PU (100K)
SD3_DAT5	C13	NVCC_SD3	GPIO	ALT5	GPIO7_IO00	Input	PU (100K)
SD3_DAT6	E13	NVCC_SD3	GPIO	ALT5	GPIO6_IO18	Input	PU (100K)
SD3_DAT7	F13	NVCC_SD3	GPIO	ALT5	GPIO6_IO17	Input	PU (100K)
SD3_RST	D15	NVCC_SD3	GPIO	ALT5	GPIO7_IO08	Input	PU (100K)
SD4_CLK	E16	NVCC_NANDF	GPIO	ALT5	GPIO7_IO10	Input	PU (100K)
SD4_CMD	B17	NVCC_NANDF	GPIO	ALT5	GPIO7_IO09	Input	PU (100K)
SD4_DAT0	D18	NVCC_NANDF	GPIO	ALT5	GPIO2_IO08	Input	PU (100K)
SD4_DAT1	B19	NVCC_NANDF	GPIO	ALT5	GPIO2_IO09	Input	PU (100K)
SD4_DAT2	F17	NVCC_NANDF	GPIO	ALT5	GPIO2_IO10	Input	PU (100K)
SD4_DAT3	A20	NVCC_NANDF	GPIO	ALT5	GPIO2_IO11	Input	PU (100K)
SD4_DAT4	E18	NVCC_NANDF	GPIO	ALT5	GPIO2_IO12	Input	PU (100K)
SD4_DAT5	C19	NVCC_NANDF	GPIO	ALT5	GPIO2_IO13	Input	PU (100K)
SD4_DAT6	B20	NVCC_NANDF	GPIO	ALT5	GPIO2_IO14	Input	PU (100K)
SD4_DAT7	D19	NVCC_NANDF	GPIO	ALT5	GPIO2_IO15	Input	PU (100K)
TAMPER	E11	VDD_SNVS_IN	GPIO	ALT0	SNVS_TAMPER	Input	PD (100K)
TEST_MODE	E12	VDD_SNVS_IN	—	—	TCU_TEST_MODE	Input	PD (100K)
USB_H1_DN	F10	VDD_USB_CAP	—	—	USB_H1_DN	—	—
USB_H1_DP	E10	VDD_USB_CAP	—	—	USB_H1_DP	—	—
USB_OTG_CHD_B	B8	VDD_USB_CAP	—	—	USB_OTG_CHD_B	—	—
USB_OTG_DN	B6	VDD_USB_CAP	—	—	USB_OTG_DN	—	—
USB_OTG_DP	A6	VDD_USB_CAP	—	—	USB_OTG_DP	—	—
XTALI	A7	NVCC_PLL	—	—	XTALI	—	—
XTALO	B7	NVCC_PLL	—	—	XTALO	—	—

1 The state immediately after reset and before ROM firmware or software has executed.