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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	4 Core, 32-Bit
Speed	852MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (1)
SATA	SATA 3Gbps (1)
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-40°C ~ 125°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	624-FBGA, FCBGA
Supplier Device Package	624-FCBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6q4avt08aer

- Graphics rendering for Human Machine Interfaces (HMI)
- High-performance speech processing with large databases
- Audio playback

The i.MX 6Dual/6Quad processors offers numerous advanced features, such as:

- Multilevel memory system—The multilevel memory system of each processor is based on the L1 instruction and data caches, L2 cache, and internal and external memory. The processors support many types of external memory devices, including DDR3, DDR3L, LPDDR2, NOR Flash, PSRAM, cellular RAM, NAND Flash (MLC and SLC), OneNAND™, and managed NAND, including eMMC up to rev 4.4/4.41.
- Smart speed technology—The processors have power management throughout the device that enables the rich suite of multimedia features and peripherals to consume minimum power in both active and various low power modes. Smart speed technology enables the designer to deliver a feature-rich product, requiring levels of power far lower than industry expectations.
- Dynamic voltage and frequency scaling—The processors improve the power efficiency of devices by scaling the voltage and frequency to optimize performance.
- Multimedia powerhouse—The multimedia performance of each processor is enhanced by a multilevel cache system, Neon® MPE (Media Processor Engine) co-processor, a multi-standard hardware video codec, 2 autonomous and independent image processing units (IPU), and a programmable smart DMA (SDMA) controller.
- Powerful graphics acceleration—Each processor provides three independent, integrated graphics processing units: an OpenGL® ES 2.0 3D graphics accelerator with four shaders (up to 200 MTri/s and OpenCL support), 2D graphics accelerator, and dedicated OpenVG™ 1.1 accelerator.
- Interface flexibility—Each processor supports connections to a variety of interfaces: LCD controller for up to four displays (including parallel display, HDMI1.4, MIPI display, and LVDS display), dual CMOS sensor interface (parallel or through MIPI), high-speed USB on-the-go with PHY, high-speed USB host with PHY, multiple expansion card ports (high-speed MMC/SDIO host and other), 10/100/1000 Mbps Gigabit Ethernet controller, and a variety of other popular interfaces (such as UART, I^2C, and I^2S serial audio, SATA-II, and PCIe-II).
- Automotive environment support—Each processor includes interfaces, such as two CAN ports, an MLB150/50 port, an ESAI audio interface, and an asynchronous sample rate converter for multichannel/multisource audio.
- Advanced security—The processors deliver hardware-enabled security features that enable secure e-commerce, digital rights management (DRM), information encryption, secure boot, and secure software downloads. The security features are discussed in detail in the i.MX 6Dual/6Quad security reference manual (IMX6DQ6SDLSRM).
- Integrated power management—The processors integrate linear regulators and internally generate voltage levels for different domains. This significantly simplifies system power management structure.

2 Architectural Overview

The following subsections provide an architectural overview of the i.MX 6Dual/6Quad processor system.

2.1 Block Diagram

Figure 2 shows the functional modules in the i.MX 6Dual/6Quad processor system.

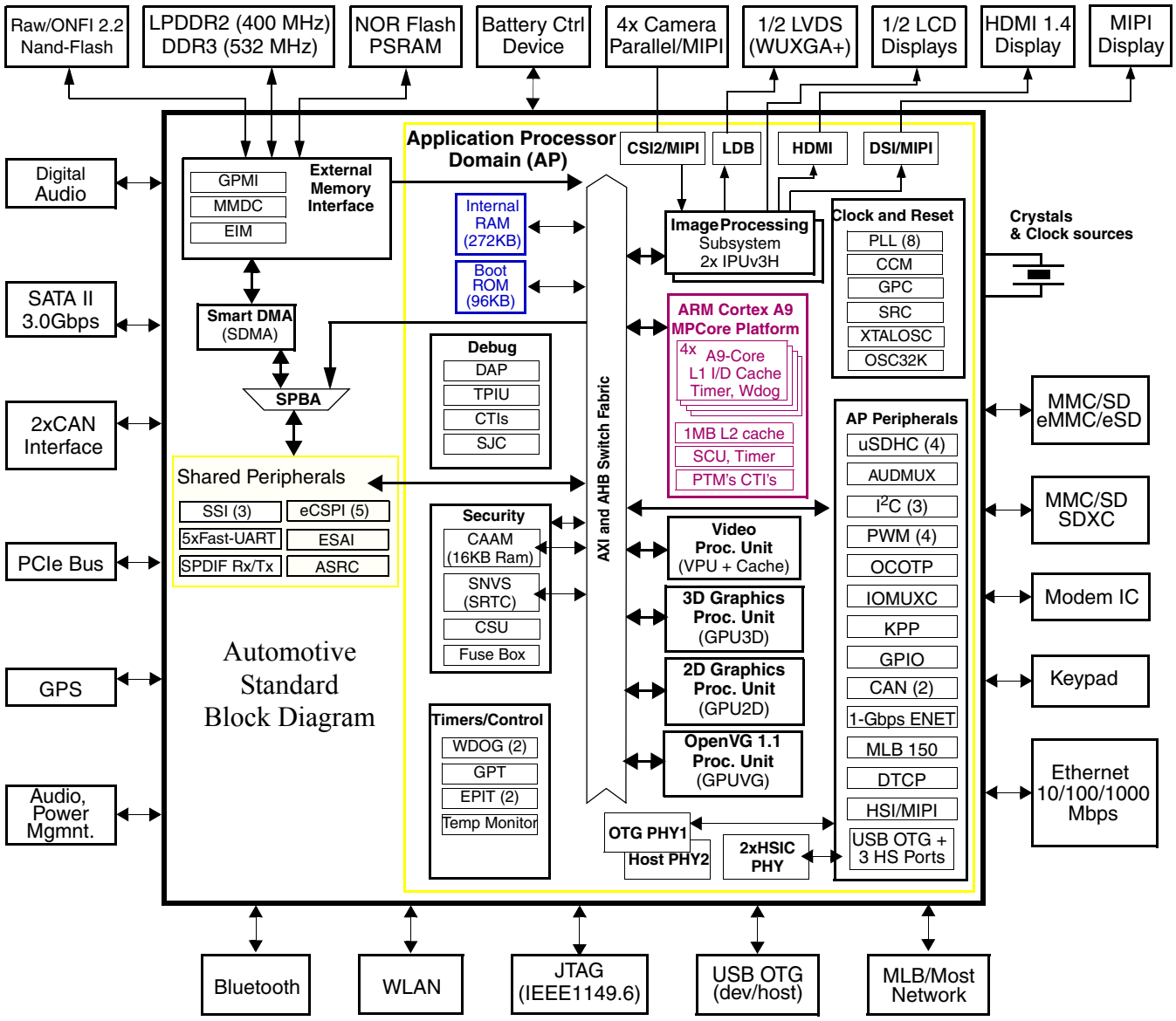


Figure 2. i.MX 6Dual/6Quad Automotive Grade System Block Diagram

NOTE

The numbers in brackets indicate number of module instances. For example, PWM (4) indicates four separate PWM peripherals.

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SSI-1 SSI-2 SSI-3	I2S/SSI/AC97 Interface	Connectivity Peripherals	The SSI is a full-duplex synchronous interface, which is used on the processor to provide connectivity with off-chip audio peripherals. The SSI supports a wide variety of protocols (SSI normal, SSI network, I2S, and AC-97), bit depths (up to 24 bits per word), and clock / frame sync options. The SSI has two pairs of 8x24 FIFOs and hardware support for an external DMA controller to minimize its impact on system performance. The second pair of FIFOs provides hardware interleaving of a second audio stream that reduces CPU overhead in use cases where two time slots are being used simultaneously.
TEMPMON	Temperature Monitor	System Control Peripherals	The temperature monitor/sensor IP module for detecting high temperature conditions. The temperature read out does not reflect case or ambient temperature. It reflects the temperature in proximity of the sensor location on the die. Temperature distribution may not be uniformly distributed; therefore, the read out value may not be the reflection of the temperature value for the entire die.
TZASC	Trust-Zone Address Space Controller	Security	The TZASC (TZC-380 by ARM) provides security address region control functions required for intended application. It is used on the path to the DRAM controller.
UART-1 UART-2 UART-3 UART-4 UART-5	UART Interface	Connectivity Peripherals	Each of the UARTv2 modules support the following serial data transmit/receive protocols and configurations: • 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none) • Programmable baud rates up to 5 MHz • 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud • IrDA 1.0 support (up to SIR speed of 115200 bps) • Option to operate as 8-pins full UART, DCE, or DTE
USBOH3A	USB 2.0 High Speed OTG and 3x HS Hosts	Connectivity Peripherals	USBOH3 contains: • One high-speed OTG module with integrated HS USB PHY • One high-speed Host module with integrated HS USB PHY • Two identical high-speed Host modules connected to HSIC USB ports.

4.1.2 Thermal Resistance

NOTE

Per JEDEC JESD51-2, the intent of thermal resistance measurements is solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment.

4.1.2.1 FCPBGA Package Thermal Resistance

Table 5 provides the FCPBGA package thermal resistance data for the *lidded* package type.

Table 5. FCPBGA Package Thermal Resistance Data (Lidded)

Thermal Parameter	Test Conditions	Symbol	Value	Unit
Junction to Ambient[1]	Single-layer board (1s); natural convection[2]	$R_{\theta JA}$	24	°C/W
	Four-layer board (2s2p); natural convection[2]	$R_{\theta JA}$	15	°C/W
Junction to Ambient[1]	Single-layer board (1s); air flow 200 ft/min[3]	$R_{\theta JMA}$	17	°C/W
	Four-layer board (2s2p); air flow 200 ft/min[4]	$R_{\theta JMA}$	12	°C/W
Junction to Board[1,4]	—	$R_{\theta JB}$	5	°C/W
Junction to Case (top)[1,5]	—	$R_{\theta JCtop}$	1	°C/W

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per JEDEC JESD51-3 with the single layer board horizontal. Thermal test board meets JEDEC specification for the specified package.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1). The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

Table 27. MLB I/O DC Parameters

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output Differential Voltage	V_{OD}	Rload = 50 Ω between padP and padN	300	500	mV
Output High Voltage	V_{OH}		1.15	1.75	V
Output Low Voltage	V_{OL}		0.75	1.35	V
Common-mode Output Voltage ((Vpad_P + Vpad_N) / 2))	V_{OCM}		1	1.5	V
Differential Output Impedance	Z_O	—	1.6	—	kΩ

4.7 I/O AC Parameters

This section includes the AC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2 and DDR3/DDR3L modes
- LVDS I/O
- MLB I/O

The GPIO and DDR I/O load circuit and output transition time waveforms are shown in Figure 4 and Figure 5.

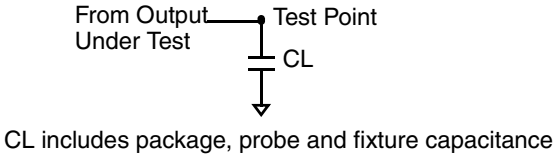


Figure 4. Load Circuit for Output

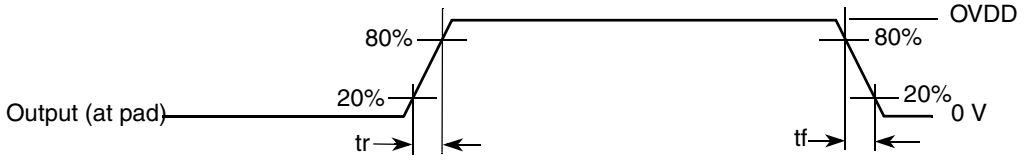


Figure 5. Output Transition Time Waveform

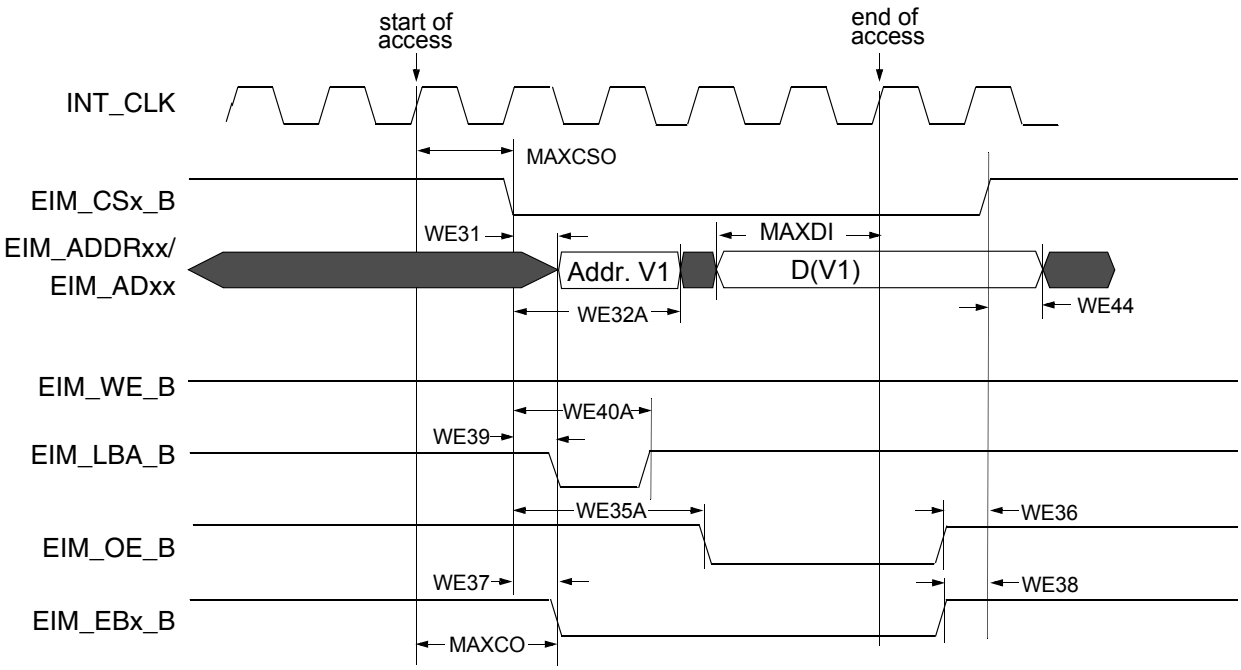


Figure 19. Asynchronous A/D Muxed Read Access (RWSC = 5)

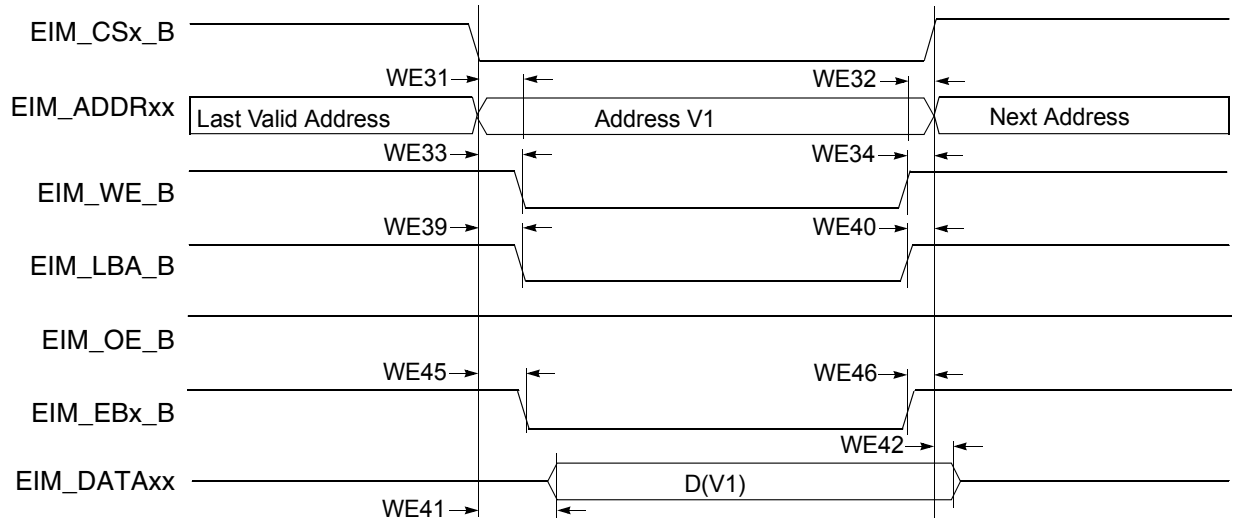


Figure 20. Asynchronous Memory Write Access

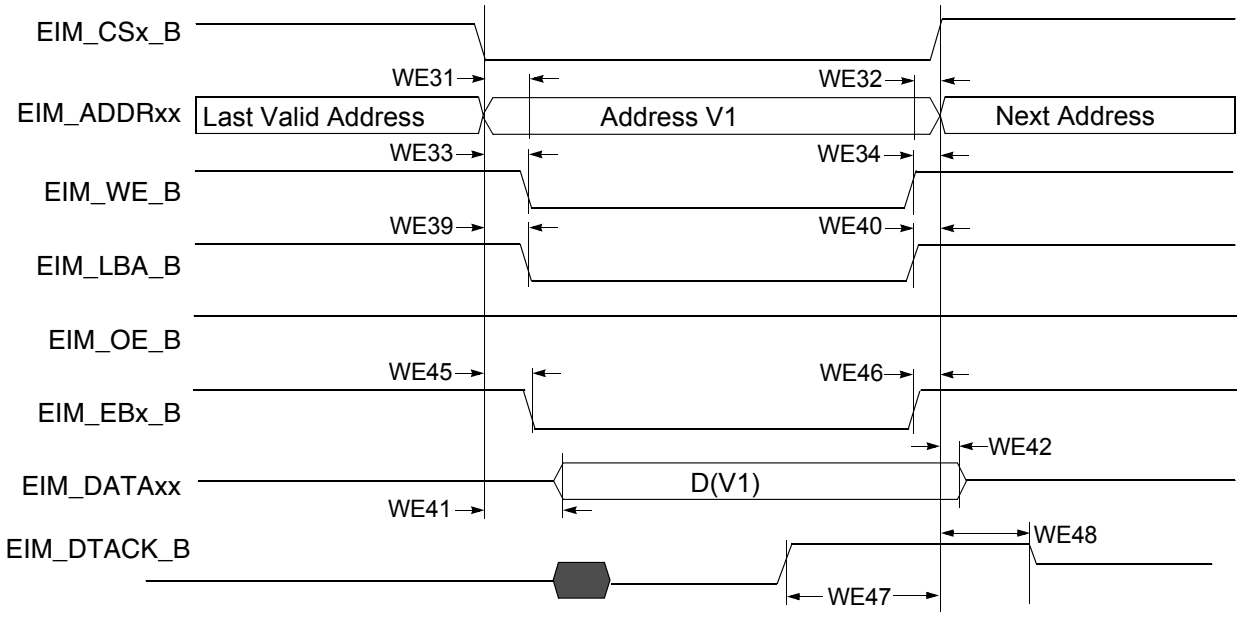


Figure 23. DTACK Mode Write Access (DAP=0)

Table 42. EIM Asynchronous Timing Parameters Relative to Chip Select[1, 2]

Ref No.	Parameter	Determination by Synchronous measured parameters	Min	Max	Unit
WE31	EIM_CSx_B valid to Address Valid	WE4-WE6-CSA×t	-3.5-CSA×t	3.5-CSA×t	ns
WE32	Address Invalid to EIM_CSx_B Invalid	WE7-WE5-CSN×t	-3.5-CSN×t	3.5-CSN×t	ns
WE32A (muxed A/D)	EIM_CSx_B valid to Address Invalid	t+WE4-WE7+ (ADVN+ADVA+1-CSA)×t	t - 3.5+(ADVN+ADVA+1-CSA)×t	t + 3.5+(ADVN+ADVA+1-CSA)×t	ns
WE33	EIM_CSx_B Valid to EIM_WE_B Valid	WE8-WE6+(WEA-WCSA)×t	-3.5+(WEA-WCSA)×t	3.5+(WEA-WCSA)×t	ns
WE34	EIM_WE_B Invalid to EIM_CSx_B Invalid	WE7-WE9+(WEN-WCSN)×t	-3.5+(WEN-WCSN)×t	3.5+(WEN-WCSN)×t	ns
WE35	EIM_CSx_B Valid to EIM_OE_B Valid	WE10- WE6+(OEA-RCSA)×t	-3.5+(OEA-RCSA)×t	3.5+(OEA-RCSA)×t	ns
WE35A (muxed A/D)	EIM_CSx_B Valid to EIM_OE_B Valid	WE10-WE6+(OEA+RADVN+RADVA+ADH+1-RCSA)×t	-3.5+(OEA+RADVN+RADVA+ADH+1-RCSA)×t	3.5+(OEA+RADVN+RADVA+ADH+1-RCSA)×t	ns
WE36	EIM_OE_B Invalid to EIM_CSx_B Invalid	WE7-WE11+(OEN-RCSN)×t	-3.5+(OEN-RCSN)×t	3.5+(OEN-RCSN)×t	ns
WE37	EIM_CSx_B Valid to EIM_EBx_B Valid (Read access)	WE12-WE6+(RBEA-RCSA)× t	-3.5+(RBEA- RCSA)×t	3.5+(RBEA - RCSA)×t	ns
WE38	EIM_EBx_B Invalid to EIM_CSx_B Invalid (Read access)	WE7-WE13+(RBEN-RCSN)×t	-3.5+ (RBEN-RCSN)×t	3.5+(RBEN-RCSN)×t	ns
WE39	EIM_CSx_B Valid to EIM_LBA_B Valid	WE14-WE6+(ADVA-CSA)×t	-3.5+ (ADVA-CSA)×t	3.5+(ADVA-CSA)×t	ns

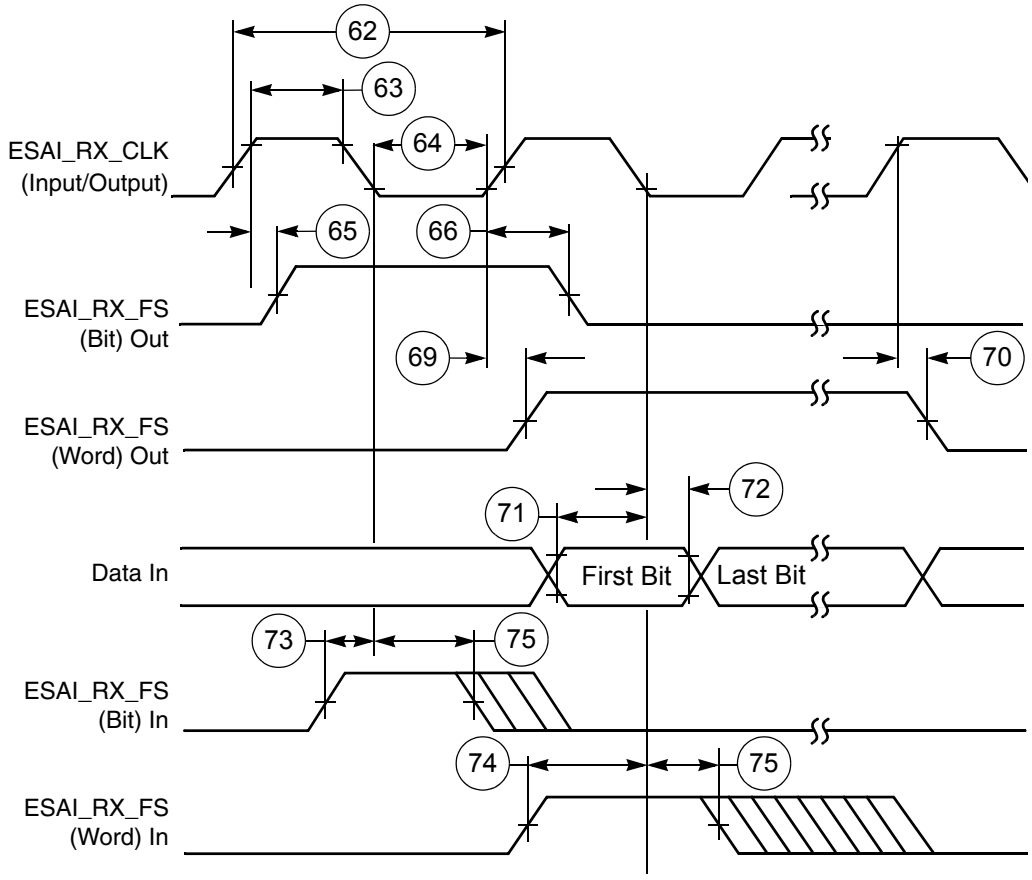


Figure 38. ESAI Receiver Timing

4.12.5.1.2 MII Transmit Signal Timing (ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER, and ENET_TX_CLK)

The transmitter functions correctly up to an ENET_TX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. Additionally, the processor clock frequency must exceed twice the ENET_TX_CLK frequency.

Figure 43 shows MII transmit signal timings. Table 54 describes the timing parameters (M5–M8) shown in the figure.

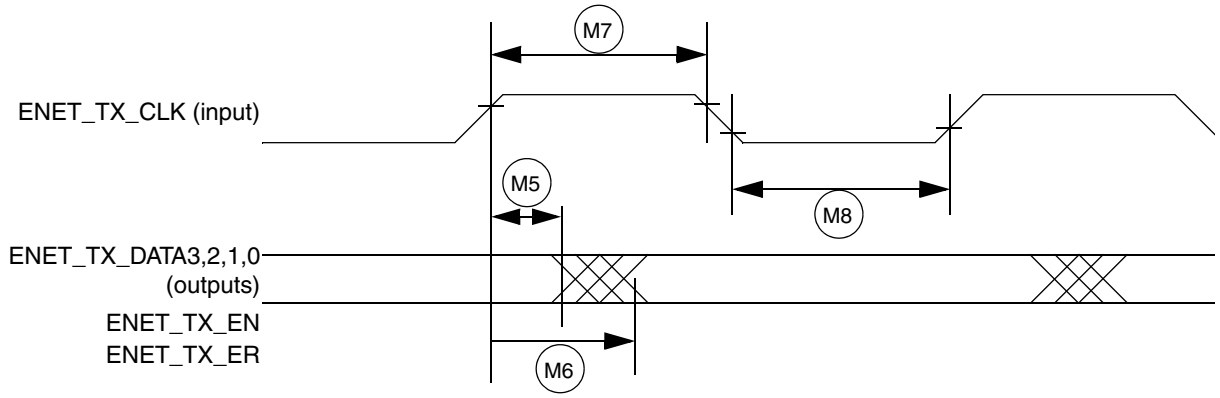


Figure 43. MII Transmit Signal Timing Diagram

Table 54. MII Transmit Signal Timing

ID	Characteristic[1]	Min	Max	Unit
M5	ENET_TX_CLK to ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER invalid	5	—	ns
M6	ENET_TX_CLK to ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER valid	—	20	ns
M7	ENET_TX_CLK pulse width high	35%	65%	ENET_TX_CLK period
M8	ENET_TX_CLK pulse width low	35%	65%	ENET_TX_CLK period

[1] ENET_TX_EN, ENET_TX_CLK, and ENET0_TXD0 have the same timing in 10-Mbps 7-wire interface mode.

4.12.5.1.3 MII Asynchronous Inputs Signal Timing (ENET_CRS and ENET_COL)

Figure 44 shows MII asynchronous input timings. Table 55 describes the timing parameter (M9) shown in the figure.

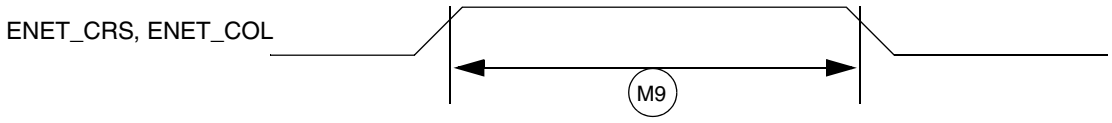


Figure 44. MII Async Inputs Timing Diagram

4.12.5.3 RGMII Signal Switching Specifications

The following timing specifications meet the requirements for RGMII interfaces for a range of transceiver devices.

Table 58. RGMII Signal Switching Specifications[1]

Symbol	Description	Min	Max	Unit
T_{cyc}[2]	Clock cycle duration	7.2	8.8	ns
T_{skewT}[3]	Data to clock output skew at transmitter	-100	900	ps
T_{skewR}[3]	Data to clock input skew at receiver	1	2.6	ns
Duty_G[4]	Duty cycle for Gigabit	45	55	%
Duty_T[4]	Duty cycle for 10/100T	40	60	%
Tr/Tf	Rise/fall time (20–80%)	—	0.75	ns

1 The timings assume the following configuration:
DDR_SEL = (11)b
DSE (drive-strength) = (111)b

2 For 10 Mbps and 100 Mbps, T_{cyc} will scale to 400 ns ±40 ns and 40 ns ±4 ns respectively.

3 For all versions of RGMII prior to 2.0; This implies that PC board design will require clocks to be routed such that an additional delay of greater than 1.2 ns and less than 1.7 ns will be added to the associated clock signal. For 10/100, the max value is unspecified.

4 Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest speed transitioned between.

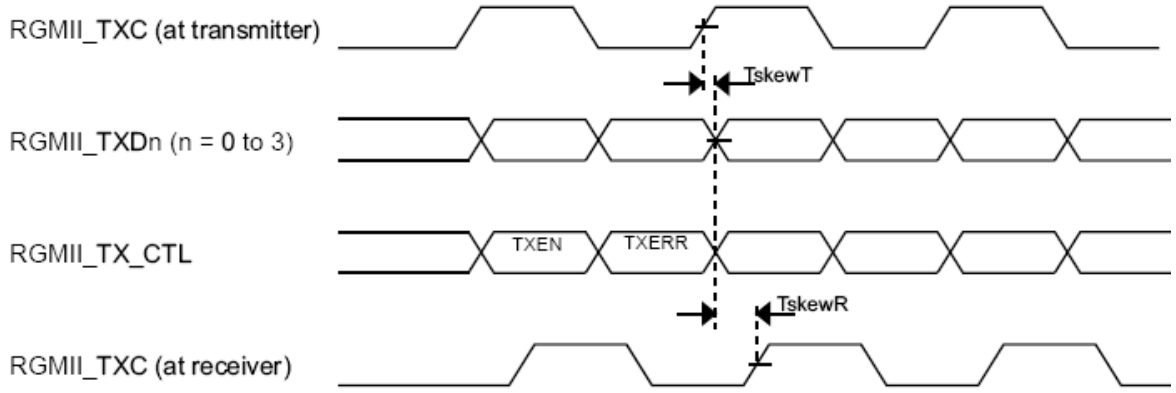


Figure 47. RGMII Transmit Signal Timing Diagram Original

Power-up time for the HDMI 3D Tx PHY while operating with the fastest input reference clock supported (340 MHz) is 133 µs.

4.12.7.2 Electrical Characteristics

The table below provides electrical characteristics for the HDMI 3D Tx PHY. The following three figures illustrate various definitions and measurement conditions specified in the table below.

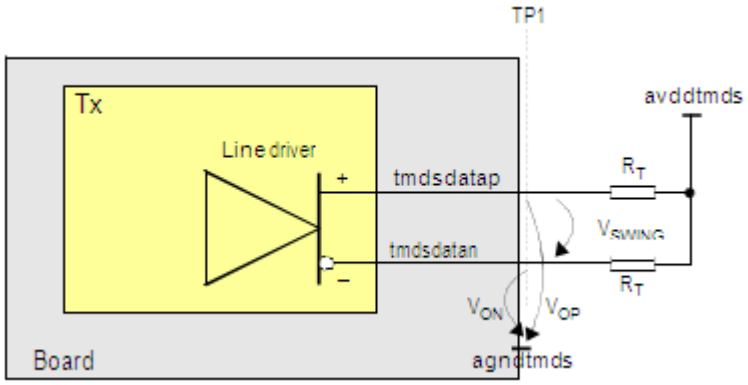


Figure 50. Driver Measuring Conditions

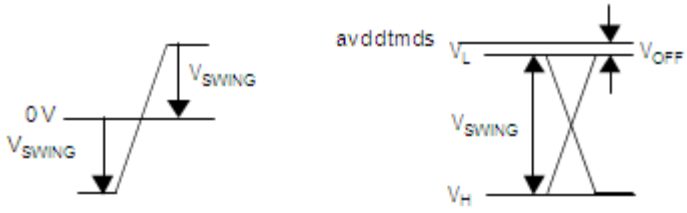


Figure 51. Driver Definitions

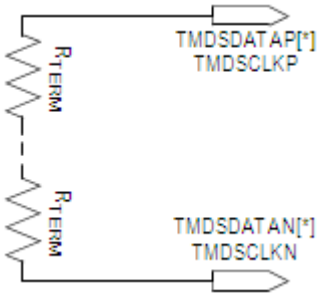


Figure 52. Source Termination

Table 59. Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Operating conditions for HDMI						
avddtmds	Termination supply voltage	—	3.15	3.3	3.45	V

2 The MSB bits are duplicated on LSB bits implementing color extension.
3 The two MSB bits are duplicated on LSB bits implementing color extension.
4 YCbCr, 8 bits—Supported within the BT.656 protocol (sync embedded within the data stream).
5 RGB, 16 bits—Supported in two ways: (1) As a “generic data” input—with no on-the-fly processing; (2) With on-the-fly processing, but only under some restrictions on the control protocol.
6 YCbCr, 16 bits—Supported as a “generic-data” input—with no on-the-fly processing.
7 YCbCr, 16 bits—Supported as a sub-case of the YCbCr, 20 bits, under the same conditions (BT.1120 protocol).
8 YCbCr, 20 bits—Supported only within the BT.1120 protocol (syncs embedded within the data stream).

4.12.10.2 Sensor Interface Timings

There are three camera timing modes supported by the IPU.

4.12.10.2.1 BT.656 and BT.1120 Video Mode

Smart camera sensors, which include imaging processing, usually support video mode transfer. They use an embedded timing syntax to replace the IPU2_CSIx_VSYNC and IPU2_CSIx_HSYNC signals. The timing syntax is defined by the BT.656/BT.1120 standards.

This operation mode follows the recommendations of ITU BT.656/ ITU BT.1120 specifications. The only control signal used is IPU2_CSIx_PIX_CLK. Start-of-frame and active-line signals are embedded in the data stream. An active line starts with a SAV code and ends with a EAV code. In some cases, digital blanking is inserted in between EAV and SAV code. The CSI decodes and filters out the timing-coding from the data stream, thus recovering IPU2_CSIx_VSYNC and IPU2_CSIx_HSYNC signals for internal use. On BT.656 one component per cycle is received over the IPU2_CSIx_DATA_EN bus. On BT.1120 two components per cycle are received over the IPU2_CSIx_DATA_EN bus.

4.12.10.2.2 Gated Clock Mode

The IPU2_CSIx_VSYNC, IPU2_CSIx_HSYNC, and IPU2_CSIx_PIX_CLK signals are used in this mode. See Figure 59.

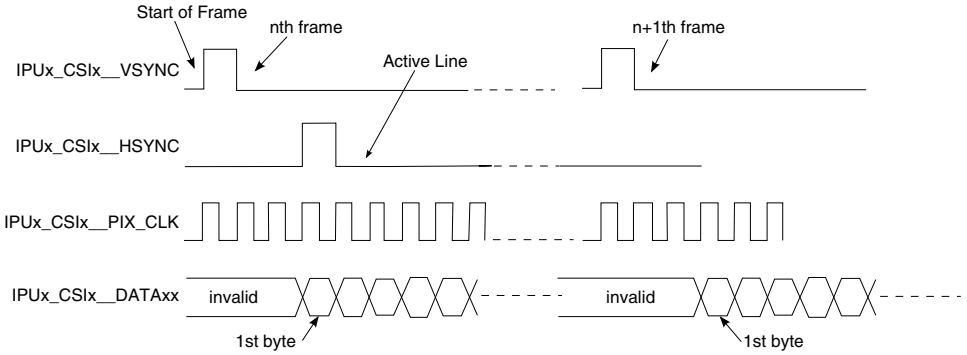


Figure 59. Gated Clock Mode Timing Diagram

A frame starts with a rising edge on IPU2_CSIx_VSYNC (all the timings correspond to straight polarity of the corresponding signals). Then IPU2_CSIx_HSYNC goes to high and hold for the entire line. Pixel clock is valid as long as IPU2_CSIx_HSYNC is high. Data is latched at the rising edge of the valid pixel clocks. IPU2_CSIx_HSYNC goes to low at the end of line. Pixel clocks then become invalid and the CSI

Table 64. Video Signal Cross-Reference (continued)

i.MX 6Dual/6Quad	LCD						Comment[1,2]
Port Name (x = 0, 1)	RGB, Signal Name (General)	RGB/TV Signal Allocation (Example)					
		16-bit RGB	18-bit RGB	24 Bit RGB	8-bit YCrCb[3]	16-bit YCrCb	20-bit YCrCb	
IPUx_DIx_PIN04	—						Additional frame/row synchronous signals with programmable timing
IPUx_DIx_PIN05	—						
IPUx_DIx_PIN06	—						
IPUx_DIx_PIN07	—						
IPUx_DIx_PIN08	—						
IPUx_DIx_D0_CS	—						—
IPUx_DIx_D1_CS	—						Alternate mode of PWM output for contrast or brightness control
IPUx_DIx_PIN11	—						—
IPUx_DIx_PIN12	—						—
IPUx_DIx_PIN13	—						Register select signal
IPUx_DIx_PIN14	—						Optional RS2
IPUx_DIx_PIN15	DRDY/DV						Data validation/blank, data enable
IPUx_DIx_PIN16	—						Additional data synchronous signals with programmable features/timing
IPUx_DIx_PIN17	Q						

1 Signal mapping (both data and control/synchronization) is flexible. The table provides examples.

2 Restrictions for ports IPUx_DISPx_DAT00 through IPUx_DISPx_DAT23 are as follows:
- A maximum of three continuous groups of bits can be independently mapped to the external bus. Groups must not overlap.
- The bit order is expressed in each of the bit groups, for example, B[0] = least significant blue pixel bit.

3 This mode works in compliance with recommendation ITU-R BT.656. The timing reference signals (frame start, frame end, line start, and line end) are embedded in the 8-bit data bus. Only video data is supported, transmission of non-video related data during blanking intervals is not supported.

NOTE

Table 64 provides information for both the DISP0 and DISP1 ports. However, DISP1 port has reduced pinout depending on IOMUXC configuration and therefore may not support all configurations. See the IOMUXC table for details.

4.12.10.5 IPU Display Interface Timing

The IPU Display Interface supports two kinds of display accesses: synchronous and asynchronous. There are two groups of external interface pins to provide synchronous and asynchronous controls.

4.12.10.5.1 Synchronous Controls

The synchronous control changes its value as a function of a system or of an external clock. This control has a permanent period and a permanent waveform.

4.12.13.9 DATA and FLAG Signal Timing

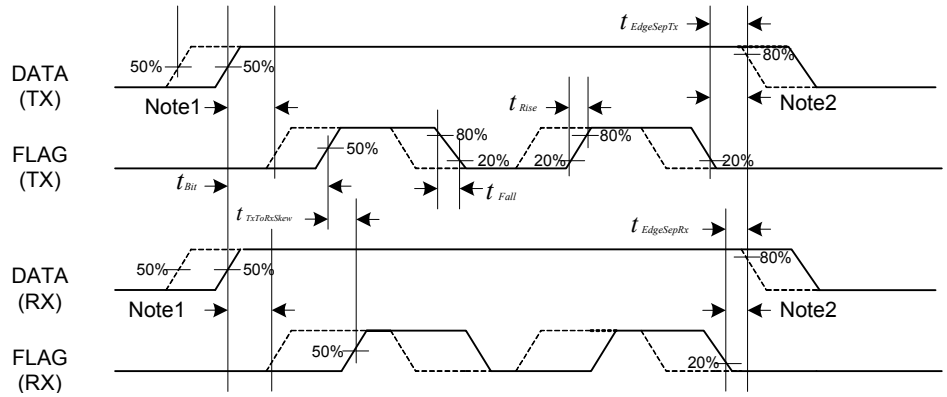


Figure 80. DATA and FLAG Signal Timing

4.12.14 MediaLB (MLB) Characteristics

4.12.14.1 MediaLB (MLB) DC Characteristics

Table 71 lists the MediaLB 3-pin interface electrical characteristics.

Table 71. MediaLB 3-Pin Interface Electrical DC Specifications

Parameter	Symbol	Test Conditions	Min	Max	Unit
Maximum input voltage	—	—	—	3.6	V
Low level input threshold	V_{IL}	—	—	0.7	V
High level input threshold	V_{IH}	See Note[1]	1.8	—	V
Low level output threshold	V_{OL}	I_{OL} = 6 mA	—	0.4	V
High level output threshold	V_{OH}	I_{OH} = –6 mA	2.0	—	V
Input leakage current	I_L	0 < V_{in} < VDD	—	±10	µA

[1] Higher V_{IH} thresholds can be used; however, the risks associated with less noise margin in the system must be evaluated and assumed by the customer.

Table 72 lists the MediaLB 6-pin interface electrical characteristics.

Table 72. MediaLB 6-Pin Interface Electrical DC Specifications

Parameter	Symbol	Test Conditions	Min	Max	Unit
Driver Characteristics					
Differential output voltage (steady-state): I V_{O+} - V_{O-} I	V_{OD}	See Note[1]	300	500	mV
Difference in differential output voltage between (high/low) steady-states: I $V_{OD, high}$ - $V_{OD, low}$ I	ΔV_{OD}	—	-50	50	mV

4.12.14.2 MediaLB (MLB) Controller AC Timing Electrical Specifications

This section describes the timing electrical information of the MediaLB module. Figure 81 show the timing of MediaLB 3-pin interface, and Table 73 and Table 74 lists the MediaLB 3-pin interface timing characteristics.

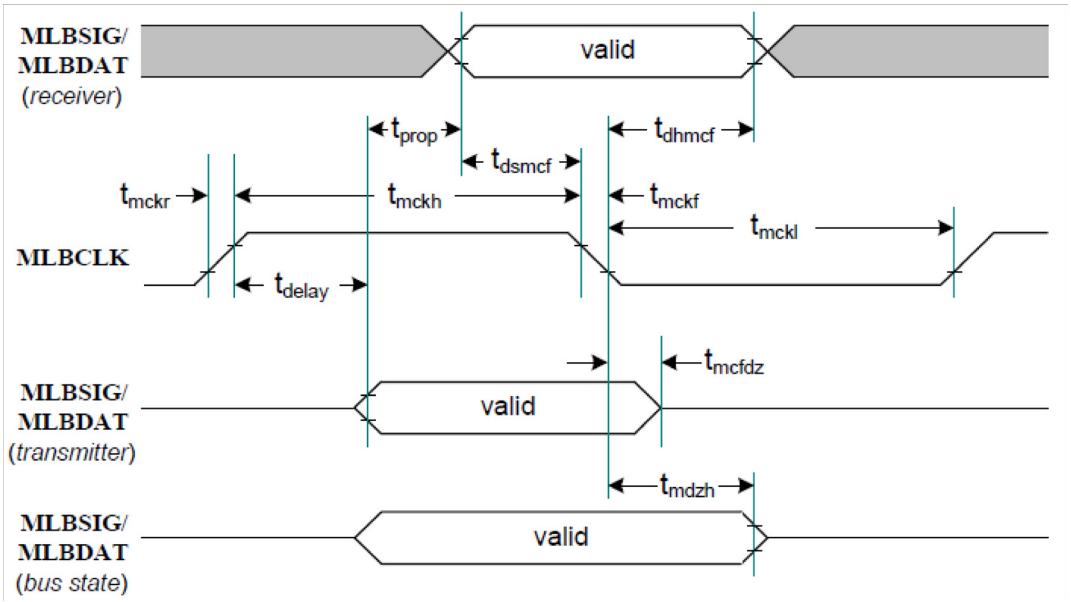


Figure 81. MediaLB 3-Pin Timing

Ground = 0.0 V; Load Capacitance = 60 pF; MediaLB speed = 256/512 Fs; Fs = 48 kHz; all timing parameters specified from the valid voltage threshold as listed below; unless otherwise noted.

Table 73. MLB 256/512 Fs Timing Parameters

Parameter	Symbol	Min	Max	Unit	Comment
MLB_CLK operating frequency[1]	f_{mck}	11.264	 25.6	MHz	256xFs at 44.0 kHz 512xFs at 50.0 kHz
MLB_CLK rise time	t_{mckr}	—	3	ns	V_{IL} TO V_{IH}
MLB_CLK fall time	t_{mckf}	—	3	ns	V_{IH} TO V_{IL}
MLB_CLK low time[2]	t_{mckl}	30 14	—	ns	256xFs 512xFs
MLB_CLK high time	t_{mckh}	30 14	—	ns	256xFs 512xFs
MLB_SIG/MLB_DATA receiver input valid to MLB_CLK falling	t_{dsmcf}	1	—	ns	—
MLB_SIG/MLB_DATA receiver input hold from MLB_CLK low	t_{dhmcf}	t_{mdzh}	—	ns	—
MLB_SIG/MLB_DATA output high impedance from MLB_CLK low	t_{mcfdz}	0	t_{mckl}	ns	(see [3])

Table 80. SPDIF Timing Parameters

Parameter	Symbol	Timing Parameter Range		Unit
		Min	Max	
SPDIF_IN Skew: asynchronous inputs, no specs apply	—	—	0.7	ns
SPDIF_OUT output (Load = 50pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 24.2 31.3	ns
SPDIF_OUT output (Load = 30pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 13.6 18.0	ns
Modulating Rx clock (SPDIF_SR_CLK) period	srckp	40.0	—	ns
SPDIF_SR_CLK high period	srckph	16.0	—	ns
SPDIF_SR_CLK low period	srckpl	16.0	—	ns
Modulating Tx clock (SPDIF_ST_CLK) period	stclkp	40.0	—	ns
SPDIF_ST_CLK high period	stclkph	16.0	—	ns
SPDIF_ST_CLK low period	stclkpl	16.0	—	ns

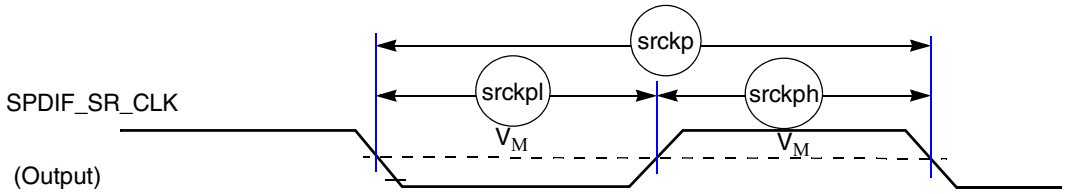


Figure 88. SPDIF_SR_CLK Timing Diagram

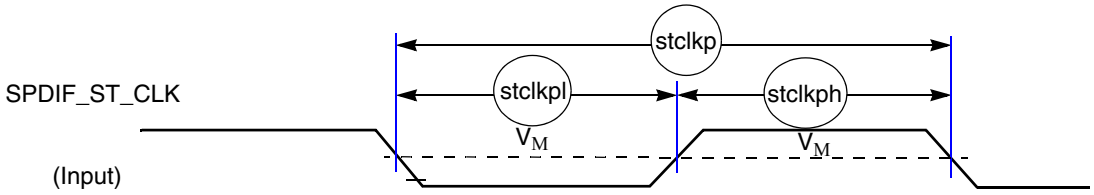


Figure 89. SPDIF_ST_CLK Timing Diagram

Table 82. SSI Transmitter Timing with Internal Clock

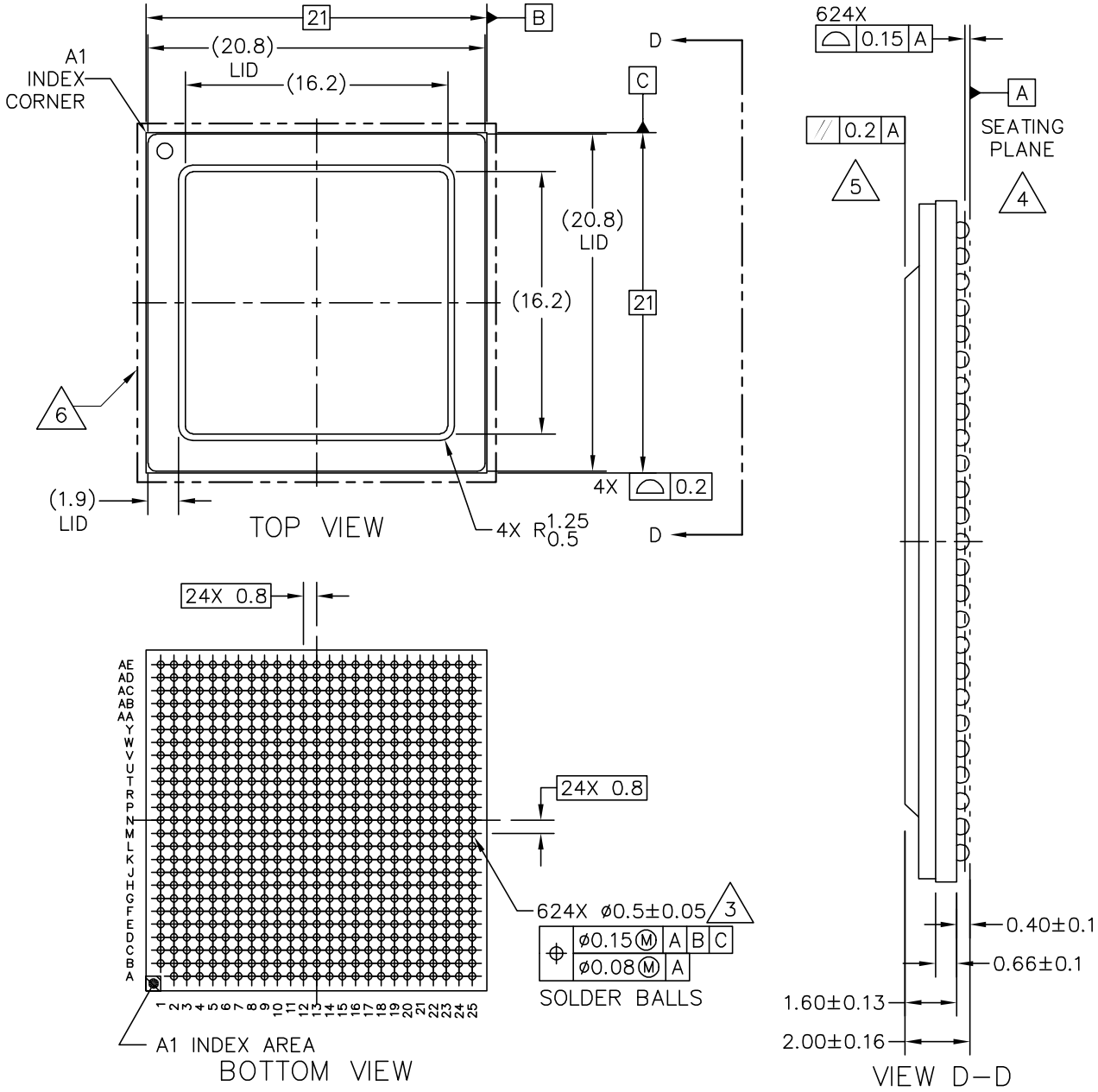
ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	AUDx_TXC/AUDx_RXC clock period	81.4	—	ns
SS2	AUDx_TXC/AUDx_RXC clock high period	36.0	—	ns
SS4	AUDx_TXC/AUDx_RXC clock low period	36.0	—	ns
SS6	AUDx_TXC high to AUDx_TXFS (bl) high	—	15.0	ns
SS8	AUDx_TXC high to AUDx_TXFS (bl) low	—	15.0	ns
SS10	AUDx_TXC high to AUDx_TXFS (wl) high	—	15.0	ns
SS12	AUDx_TXC high to AUDx_TXFS (wl) low	—	15.0	ns
SS14	AUDx_TXC/AUDx_RXC Internal AUDx_TXFS rise time	—	6.0	ns
SS15	AUDx_TXC/AUDx_RXC Internal AUDx_TXFS fall time	—	6.0	ns
SS16	AUDx_TXC high to AUDx_TXD valid from high impedance	—	15.0	ns
SS17	AUDx_TXC high to AUDx_TXD high/low	—	15.0	ns
SS18	AUDx_TXC high to AUDx_TXD high impedance	—	15.0	ns
Synchronous Internal Clock Operation				
SS42	AUDx_RXD setup before AUDx_TXC falling	10.0	—	ns
SS43	AUDx_RXD hold after AUDx_TXC falling	0.0	—	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal AUDx_TXC/AUDx_RXC and/or the frame sync AUDx_TXFS/AUDx_RXFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- The terms, WL and BL, refer to Word Length(WL) and Bit Length(BL).
- For internal Frame Sync operation using external clock, the frame sync timing is the same as that of transmit data (for example, during AC97 mode of operation).

6.2.1.1 21 x 21 mm Lidded Package

Figure 100 and Figure 101 show the top, bottom, and side views of the 21 × 21 mm lidded package.



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TITLE: 624 I/O FC PBGA, 21 X 21 X 2 PKG, 0.8 MM PITCH, STAMPED LID	DOCUMENT NO: 98ASA00330D	REV: E
	STANDARD: NON–JEDEC	
	SOT1643–1	07 JAN 2016

Figure 100. 21 x 21 mm Lidded Package Top, Bottom, and Side Views (Sheet 1 of 2)

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.
6. 21.2MM MAXIMUM PACKAGE ASSEMBLY (LID + LAMINATE) X AND Y.

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TITLE: 624 I/O FC PBGA, 21 X 21 X 2 PKG, 0.8 MM PITCH, STAMPED LID	DOCUMENT NO: 98ASA00330D	REV: E
	STANDARD: NON–JEDEC	
	SOT1643–1	07 JAN 2016

Figure 101. 21 x 21 mm Lidded Package Top, Bottom, and Side Views (Sheet 2 of 2)

7 Revision History

Table 99 provides a revision history for the i.MX 6Dual/6Quad data sheet.

Table 99. i.MX 6Dual/6Quad Data Sheet Document Revision History

Rev. Number	Date	Substantive Change(s)
5	09/2017	Rev. 5 changes include the following: • Changed throughout: – Changed terminology from “floating” to “not connected”. – Removed VADC feature from 19mm x 19mm package. Contact NXP sales and marketing with enablement options. • Section 1, “Introduction” on page 1: Corrected typo in last sentence of first paragraph “aut1omotive”. • Section 1.2, “Features” on page 5: Changed Internal/external peripheral item from “LVDS serial ports—One port up to 165 MPixels/sec…” to: “…—One port up to 170 MPixels/sec…”. • Table 1, “Example Orderable Part Numbers”: Added part numbers for silicon revision 1.4 with suffix “E”. • Section 1.3, “Signal Naming Convention” on page 8” and Section 6.1, “Signal Naming Convention”: changed wording from *updated* or *changed signal naming,* to *standard signal naming*. • Table 2, “i.MX 6Dual/6Quad Modules List,” on page 11: – Added bullet to uSDHC row: “Conforms to the SD Host Controller Standard Specification v3.0” • Section 4, “Electrical Characteristics” on page 20: Changed several references from JESD and JEDEC standards to cross references to the Section 4.10, “Multi-Mode DDR Controller (MMDC). • Table 4, “Absolute Maximum Ratings,” on page 21: Multiple changes: – Core supply voltages: Separated rows by LDO enabled and LDO bypass. For LDO enabled, changed maximum value from 1.5 to 1.6V. – Renamed Internal supply voltages to Core supply output voltage (LDO enabled) and changed maximum value from 1.3 to 1.4V. Added symbol NVCC_PLL_OUT. – Reordered VDD_HIGH_IN row and changed maximum value from 3.6 to 3.7V. – DDR I/O supply voltage row changes: — Changed Symbols from “Supplies denoted as I/O supply” to: “NVCC_DRAM” — Added footnote. – GPIO I/O supply voltage: Added symbols. Changed maximum value from 3.6 to 3.7V. – Resequenced: HDMI, PCIe, and SATA PHY high (VPH) supply voltage to precede low (VP) – Added row: RGMII I/O supply voltage – Added row, V_{in}/V_{out} input/output voltage range (non-DDR pins) distinguishing between DDR pins. – Changed maximum value for V_{in}/V_{out} input/output voltage range DDR pins to OVDD+0.4. – Added footnotes to both maximum values of V_{in}/V_{out} input/output voltage range. – Added row: USB_OTG_CHD_B • Section 4.1.2, “Thermal Resistance” on page 22: Added NOTE: “Per JEDEC JESD51-2, the intent of thermal resistance measurements…”. • Section 4.1.5, “Maximum Measured Supply Currents” on page 26: Clarified language throughout this section regarding the use case to estimate the maximum supply current. • Section 4.2.1, “Power-Up Sequence” on page 33: – Removed content about calculating the proper current limiting resistor for a coin cell. – Removed inference to internal POR. • Section 4.5.2, “OSC32K” on page 37: Removed content about calculating the proper current limiting resistor for a coin cell. • Section 4.6.1, “XTALI and RTC_XTALI (Clock Inputs) DC Parameters” on page 39: – Added “NOTE: The Vil and Vih specifications only apply when an external clock source is used…”. *(Revision History table continues on next page.)*