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Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Active
Core Processor	ARM® Cortex® -A9
Number of Cores/Bus Width	4 Core, 32-Bit
Speed	852MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (1)
SATA	SATA 3Gbps (1)
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-40°C ~ 125°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	624-FBGA, FCBGA
Supplier Device Package	624-FCBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6q6avt08ae

Table 1. Example Orderable Part Numbers (continued)

Part Number	Quad/Dual CPU	Options	Speed ¹ Grade	Temperature Grade	Package
MCIMX6D4AVT10AE	i.MX 6Dual	Includes GPU, no VPU	1 GHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6D6AVT08AC	i.MX 6Dual	Includes VPU, GPU	852 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6D6AVT08AD	i.MX 6Dual	Includes VPU, GPU	852 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6D6AVT08AE	i.MX 6Dual	Includes VPU, GPU	852 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6D4AVT08AC	i.MX 6Dual	Includes GPU, no VPU	852 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6D4AVT08AD	i.MX 6Dual	Includes GPU, no VPU	852 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6D4AVT08AE	i.MX 6Dual	Includes GPU, no VPU	852 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)

¹ If a 24 MHz input clock is used (required for USB), the maximum SoC speed is limited to 996 MHz.

Figure 1 describes the part number nomenclature to identify the characteristics of the specific part number you have (for example, cores, frequency, temperature grade, fuse options, silicon revision). Figure 1 applies to the i.MX 6Dual/6Quad.

The two characteristics that identify which data sheet a specific part applies to are the part number series field and the temperature grade (junction) field:

- The i.MX 6Dual/6Quad Automotive and Infotainment Applications Processors data sheet (IMX6DQAECE) covers parts listed with “A (Automotive temp)”
- The i.MX 6Dual/6Quad Applications Processors for Consumer Products data sheet (IMX6DQCEC) covers parts listed with “D (Commercial temp)” or “E (Extended Commercial temp)”
- The i.MX 6Dual/6Quad Applications Processors for Industrial Products data sheet (IMX6DQIEC) covers parts listed with “C (Industrial temp)”

The Ensure that you have the right data sheet for your specific part by checking the temperature grade (junction) field and matching it to the right data sheet. If you have questions, see nxp.com/imx6series or contact your NXP representative.

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
LDB	LVDS Display Bridge	Connectivity Peripherals	LVDS Display Bridge is used to connect the IPU (Image Processing Unit) to External LVDS Display Interface. LDB supports two channels; each channel has following signals: • One clock pair • Four data pairs Each signal pair contains LVDS special differential pad (PadP, PadM).
MLB150	MediaLB	Connectivity / Multimedia Peripherals	The MLB interface module provides a link to a MOST® data network, using the standardized MediaLB protocol (up to 150 Mbps). The module is backward compatible to MLB-50.
MMDC	Multi-Mode DDR Controller	Connectivity Peripherals	DDR Controller has the following features: • Supports 16/32/64-bit DDR3 / DDR3L or LPDDR2 • Supports both dual x32 for LPDDR2 and x64 DDR3 / LPDDR2 configurations (including 2x32 interleaved mode) • Supports up to 4 GByte DDR memory space
OCOTP_CTRL	OTP Controller	Security	The On-Chip OTP controller (OCOTP_CTRL) provides an interface for reading, programming, and/or overriding identification and control information stored in on-chip fuse elements. The module supports electrically-programmable poly fuses (eFUSES). The OCOTP_CTRL also provides a set of volatile software-accessible signals that can be used for software control of hardware elements, not requiring non-volatility. The OCOTP_CTRL provides the primary user-visible mechanism for interfacing with on-chip fuse elements. Among the uses for the fuses are unique chip identifiers, mask revision numbers, cryptographic keys, JTAG secure mode, boot characteristics, and various control signals, requiring permanent non-volatility.
OCRAM	On-Chip Memory Controller	Data Path	The On-Chip Memory controller (OCRAM) module is designed as an interface between system's AXI bus and internal (on-chip) SRAM memory module. In i.MX 6Dual/6Quad processors, the OCRM is used for controlling the 256 KB multimedia RAM through a 64-bit AXI bus.
OSC 32 kHz	OSC 32 kHz	Clocking	Generates 32.768 kHz clock from an external crystal.
PCIe	PCI Express 2.0	Connectivity Peripherals	The PCIe IP provides PCI Express Gen 2.0 functionality.
PMU	Power-Management Functions	Data Path	Integrated power management unit. Used to provide power to various SoC domains.
PWM-1 PWM-2 PWM-3 PWM-4	Pulse Width Modulation	Connectivity Peripherals	The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images and it can also generate tones. It uses 16-bit resolution and a 4x16 data FIFO to generate sound.
RAM 16 KB	Secure/non-secure RAM	Secured Internal Memory	Secure/non-secure Internal RAM, interfaced through the CAAM.
RAM 256 KB	Internal RAM	Internal Memory	Internal RAM, which is accessed through OCRM memory controllers.

4.4 PLL Electrical Characteristics

4.4.1 Audio/Video PLL Electrical Parameters

Table 14. Audio/Video PLL Electrical Parameters

Parameter	Value
Clock output range	650 MHz ~1.3 GHz
Reference clock	24 MHz
Lock time	<11250 reference cycles

4.4.2 528 MHz PLL

Table 15. 528 MHz PLL Electrical Parameters

Parameter	Value
Clock output range	528 MHz PLL output
Reference clock	24 MHz
Lock time	<11250 reference cycles

4.4.3 Ethernet PLL

Table 16. Ethernet PLL Electrical Parameters

Parameter	Value
Clock output range	500 MHz
Reference clock	24 MHz
Lock time	<11250 reference cycles

4.4.4 480 MHz PLL

Table 17. 480 MHz PLL Electrical Parameters

Parameter	Value
Clock output range	480 MHz PLL output
Reference clock	24 MHz
Lock time	<383 reference cycles

4.8.1 GPIO Output Buffer Impedance

Table 34 shows the GPIO output buffer impedance (OVDD 1.8 V).

Table 34. GPIO Output Buffer Average Impedance (OVDD 1.8 V)

Parameter	Symbol	Drive Strength (DSE)	Typ Value	Unit
Output Driver Impedance	Rdrv	001	260	Ω
		010	130	
		011	90	
		100	60	
		101	50	
		110	40	
		111	33	

Table 35 shows the GPIO output buffer impedance (OVDD 3.3 V).

Table 35. GPIO Output Buffer Average Impedance (OVDD 3.3 V)

Parameter	Symbol	Drive Strength (DSE)	Typ Value	Unit
Output Driver Impedance	Rdrv	001	150	Ω
		010	75	
		011	50	
		100	37	
		101	30	
		110	25	
		111	20	

4.9.3 External Interface Module (EIM)

The following subsections provide information on the EIM. Maximum operating frequency for EIM data transfer is 104 MHz. Timing parameters in this section that are given as a function of register settings or clock periods are valid for the entire range of allowed frequencies (0–104 MHz).

4.9.3.1 EIM Interface Pads Allocation

EIM supports 32-bit, 16-bit and 8-bit devices operating in address/data separate or multiplexed modes. Table 40 provides EIM interface pads allocation in different modes.

Table 40. EIM Internal Module Multiplexing¹

Setup	Non Multiplexed Address/Data Mode							Multiplexed Address/Data mode	
	8 Bit				16 Bit		32 Bit	16 Bit	32 Bit
	MUM = 0, DSZ = 100	MUM = 0, DSZ = 101	MUM = 0, DSZ = 110	MUM = 0, DSZ = 111	MUM = 0, DSZ = 001	MUM = 0, DSZ = 010	MUM = 0, DSZ = 011	MUM = 1, DSZ = 001	MUM = 1, DSZ = 011
EIM_ADDR [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]
EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_DATA [09:00]
EIM_DATA [07:00], EIM_EB0_B	EIM_DATA [07:00]	—	—	—	EIM_DATA [07:00]	—	EIM_DATA [07:00]	EIM_AD [07:00]	EIM_AD [07:00]
EIM_DATA [15:08], EIM_EB1_B	—	EIM_DATA [15:08]	—	—	EIM_DATA [15:08]	—	EIM_DATA [15:08]	EIM_AD [15:08]	EIM_AD [15:08]
EIM_DATA [23:16], EIM_EB2_B	—	—	EIM_DATA [23:16]	—	—	EIM_DATA [23:16]	EIM_DATA [23:16]	—	EIM_DATA [07:00]
EIM_DATA [31:24], EIM_EB3_B	—	—	—	EIM_DATA [31:24]	—	EIM_DATA [31:24]	EIM_DATA [31:24]	—	EIM_DATA [15:08]

¹ For more information on configuration ports mentioned in this table, see the i.MX 6Dual/6Quad reference manual (IMX6DQRM).

Table 42. EIM Asynchronous Timing Parameters Relative to Chip Select^{1, 2} (continued)

Ref No.	Parameter	Determination by Synchronous measured parameters	Min	Max	Unit
WE40	EIM_LBA_B Invalid to EIM_CSx_B Invalid (ADVL is asserted)	WE7-WE15-CSN×t	-3.5-CSN×t	3.5-CSN×t	ns
WE40A (muxed A/D)	EIM_CSx_B Valid to EIM_LBA_B Invalid	WE14-WE6+(ADV _N +ADV _A +1-CSA)×t	-3.5+(ADV _N +ADV _A +1-CSA)×t	3.5+(ADV _N +ADV _A +1-CSA)×t	ns
WE41	EIM_CSx_B Valid to Output Data Valid	WE16-WE6-WCSA×t	-3.5-WCSA×t	3.5-WCSA×t	ns
WE41A (muxed A/D)	EIM_CSx_B Valid to Output Data Valid	WE16-WE6+(WADV _N +WADV _A +ADH+1-WCSA)×t	-3.5+(WADV _N +WADV _A +ADH+1-WCSA)×t	3.5+(WADV _N +WADV _A +ADH+1-WCSA)×t	ns
WE42	Output Data Invalid to EIM_CSx_B Invalid	WE17-WE7-CSN×t	-3.5-CSN×t	3.5-CSN×t	ns
MAXCO	Output maximum delay from internal driving EIM_ADDRxx/control flip-flops to chip outputs.	10	—	10	ns
MAXCSO	Output maximum delay from internal chip selects driving flip-flops to EIM_CSx_B out.	10	—	10	ns
MAXDI	EIM_DATAxx MAXIMUM delay from chip input data to its internal flip-flop	5	—	5	ns
WE43	Input Data Valid to EIM_CSx_B Invalid	MAXCO-MAXCSO+MAXDI	MAXCO-MAXCSO+MAXDI	—	ns
WE44	EIM_CSx_B Invalid to Input Data Invalid	0	0	—	ns
WE45	EIM_CSx_B Valid to EIM_EBx_B Valid (Write access)	WE12-WE6+(WBEA-WCSA)×t	-3.5+(WBEA-WCSA)×t	3.5+(WBEA-WCSA)×t	ns
WE46	EIM_EBx_B Invalid to EIM_CSx_B Invalid (Write access)	WE7-WE13+(WBEN-WCSN)×t	-3.5+(WBEN-WCSN)×t	3.5+(WBEN-WCSN)×t	ns
MAXDTI	Maximum delay from EIM_DTACK_B input to its internal flip-flop + 2 cycles for synchronization	10	—	10	ns
WE47	EIM_DTACK_B Active to EIM_CSx_B Invalid	MAXCO-MAXCSO+MAXDTI	MAXCO-MAXCSO+MAXDTI	—	ns
WE48	EIM_CSx_B Invalid to EIM_DTACK_B invalid	0	0	—	ns

¹ For more information on configuration parameters mentioned in this table, see the i.MX 6Dual/6Quad reference manual (IMX6DQRM).

² In this table:

- t means clock period from axi_clk frequency.
- CSA means register setting for WCSA when in write operations or RCSA when in read operations.
- CSN means register setting for WCSN when in write operations or RCSN when in read operations.
- ADVN means register setting for WADV when in write operations or RADVN when in read operations.
- ADVA means register setting for WADVA when in write operations or RADVA when in read operations.

4.10 Multi-Mode DDR Controller (MMDC)

The Multi-mode DDR Controller is a dedicated interface to DDR3/DDR3L/LPDDR2 SDRAM.

4.10.1 MMDC Compatibility with JEDEC-Compliant SDRAMs

The i.MX 6Dual/6Quad MMDC supports the following memory types:

- LPDDR2 SDRAM compliant to JESD209-2B LPDDR2 JEDEC standard release June, 2009
- DDR3/DDR3L SDRAM compliant to JESD79-3D DDR3 JEDEC standard release April, 2008

MMDC operation with the standards stated above is contingent upon the board DDR design adherence to the DDR design and layout requirements stated in the *Hardware Development Guide for i.MX 6Quad, 6Dual, 6DualLite, 6Solo Families of Applications Processors* (IMX6DQ6SDLHDG).

4.10.2 MMDC Supported DDR3/DDR3L/LPDDR2 Configurations

The table below shows the supported DDR3/DDR3L/LPDDR2 configurations:

Table 43. i.MX 6Dual/6Quad Supported DDR3/DDR3L/LPDDR2 Configurations

Parameter	LPDDR2	DDR3	DDR3L
Clock frequency	400 MHz	532 MHz	532 MHz
Bus width	32-bit per channel	16/32/64-bit	16/32/64-bit
Channel	Dual	Single	Single
Chip selects	2 per channel	2	2

4.11 General-Purpose Media Interface (GPMI) Timing

The i.MX 6Dual/6Quad GPMI controller is a flexible interface NAND Flash controller with 8-bit data width, up to 200 MB/s I/O speed and individual chip select. It supports Asynchronous timing mode, Source Synchronous timing mode, and Samsung Toggle timing mode separately described in the following subsections.

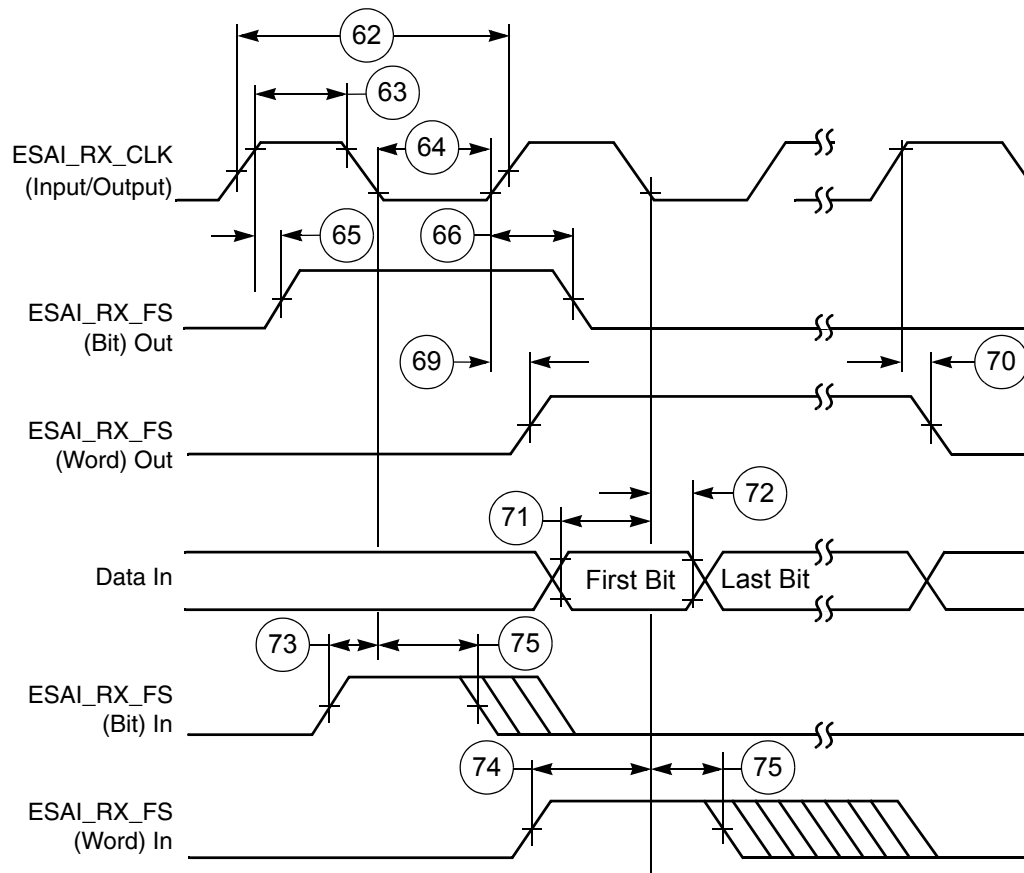


Figure 38. ESAI Receiver Timing

4.12.4.3 SDR50/SDR104 AC Timing

Figure 41 depicts the timing of SDR50/SDR104, and Table 52 lists the SDR50/SDR104 timing characteristics.

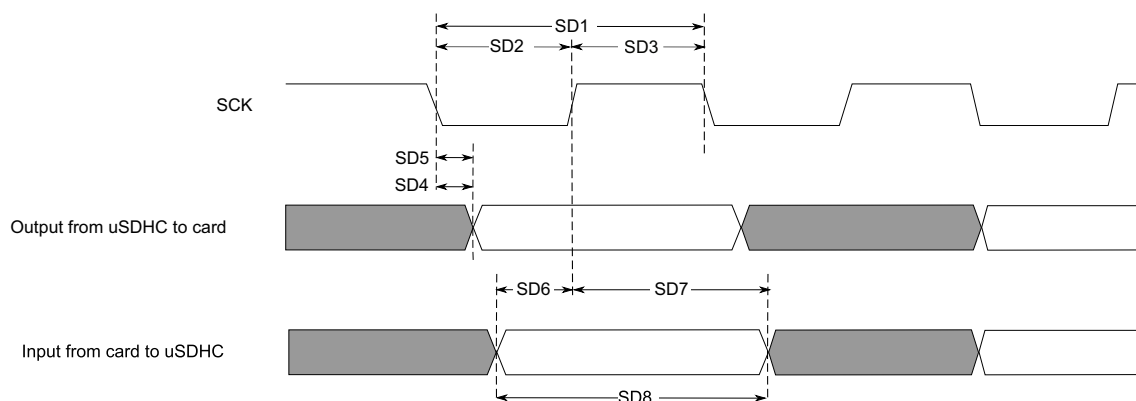


Figure 41. SDR50/SDR104 Timing

Table 52. SDR50/SDR104 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency Period	t_{CLK}	4.8	—	ns
SD2	Clock Low Time	t_{CL}	$0.46 \times t_{CLK}$	$0.54 \times t_{CLK}$	ns
SD3	Clock High Time	t_{CH}	$0.46 \times t_{CLK}$	$0.54 \times t_{CLK}$	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR50 (Reference to SDx_CLK)					
SD4	uSDHC Output Delay	t_{OD}	-3	1	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR104 (Reference to SDx_CLK)					
SD5	uSDHC Output Delay	t_{OD}	-1.6	0.74	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR50 (Reference to SDx_CLK)					
SD6	uSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD7	uSDHC Input Hold Time	t_{IH}	1.5	—	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR104 (Reference to SDx_CLK)¹					
SD8	Card Output Data Window	t_{ODW}	$0.5 \times t_{CLK}$	—	ns

¹Data window in SDR100 mode is variable.

Table 59. Electrical Characteristics (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_T	Termination resistance	—	45	50	55	Ω
TMDS drivers DC specifications						
V_{OFF}	Single-ended standby voltage	$R_T = 50 \Omega$	$avddtmds \pm 10 \text{ mV}$			mV
V_{SWING}	Single-ended output swing voltage	For measurement conditions and definitions, see the first two figures above. Compliance point TP1 as defined in the HDMI specification, version 1.3a, section 4.2.4.	400	—	600	mV
V_H	Single-ended output high voltage For definition, see the second figure above.	If attached sink supports TMDSClk < or = 165 MHz	$avddtmds \pm 10 \text{ mV}$			mV
		If attached sink supports TMDSClk > 165 MHz	$avddtmds - 200 \text{ mV}$	—	$avddtmds + 10 \text{ mV}$	mV
V_L	Single-ended output low voltage For definition, see the second figure above.	If attached sink supports TMDSClk < or = 165 MHz	$avddtmds - 600 \text{ mV}$	—	$avddtmds - 400 \text{ mV}$	mV
		If attached sink supports TMDSClk > 165 MHz	$avddtmds - 700 \text{ mV}$	—	$avddtmds - 400 \text{ mV}$	mV
R_{TERM}	Differential source termination load (inside HDMI 3D Tx PHY) Although the HDMI 3D Tx PHY includes differential source termination, the user-defined value is set for each single line (for illustration, see the third figure above). Note: R_{TERM} can also be configured to be open and not present on TMDS channels.	—	50	—	200	Ω
Hot plug detect specifications						
HPD^{VH}	Hot plug detect high range	—	2.0	—	5.3	V
$VHPD_{VL}$	Hot plug detect low range	—	0	—	0.8	V
HPD_Z	Hot plug detect input impedance	—	10	—	—	k Ω
HPD_t	Hot plug detect time delay	—	—	—	100	μs

4.12.8 Switching Characteristics

Table 60 describes switching characteristics for the HDMI 3D Tx PHY. Figure 53 to Figure 57 illustrate various parameters specified in table.

NOTE

All dynamic parameters related to the TMDS line drivers' performance imply the use of assembly guidelines.

stops receiving data from the stream. For the next line, the IPU2_CSIx_HSYNC timing repeats. For the next frame, the IPU2_CSIx_VSYNC timing repeats.

4.12.10.2.3 Non-Gated Clock Mode

The timing is the same as the gated-clock mode (described in [Section 4.12.10.2.2, “Gated Clock Mode,”](#)) except for the IPU2_CSIx_HSYNC signal, which is not used (see [Figure 60](#)). All incoming pixel clocks are valid and cause data to be latched into the input FIFO. The IPU2_CSIx_PIX_CLK signal is inactive (states low) until valid data is going to be transmitted over the bus.

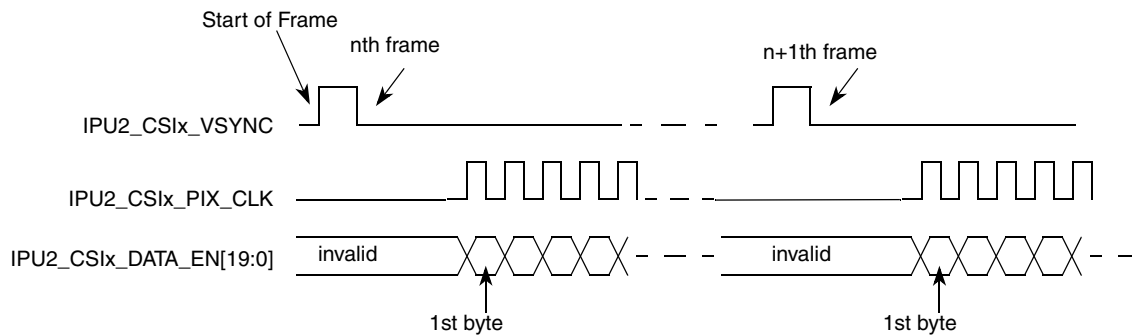


Figure 60. Non-Gated Clock Mode Timing Diagram

The timing described in [Figure 60](#) is that of a typical sensor. Some other sensors may have a slightly different timing. The CSI can be programmed to support rising/falling-edge triggered IPU2_CSIx_VSYNC; active-high/low IPU2_CSIx_HSYNC; and rising/falling-edge triggered IPU2_CSIx_PIX_CLK.

Table 64. Video Signal Cross-Reference (continued)

i.MX 6Dual/6Quad	LCD							Comment ^{1,2}
Port Name (x = 0, 1)	RGB, Signal Name (General)	RGB/TV Signal Allocation (Example)						
		16-bit RGB	18-bit RGB	24 Bit RGB	8-bit YCrCb ³	16-bit YCrCb	20-bit YCrCb	
IPUx_DISPx_DAT05	DAT[5]	G[0]	B[5]	B[5]	Y/C[5]	C[5]	C[5]	—
IPUx_DISPx_DAT06	DAT[6]	G[1]	G[0]	B[6]	Y/C[6]	C[6]	C[6]	—
IPUx_DISPx_DAT07	DAT[7]	G[2]	G[1]	B[7]	Y/C[7]	C[7]	C[7]	—
IPUx_DISPx_DAT08	DAT[8]	G[3]	G[2]	G[0]	—	Y[0]	C[8]	—
IPUx_DISPx_DAT09	DAT[9]	G[4]	G[3]	G[1]	—	Y[1]	C[9]	—
IPUx_DISPx_DAT10	DAT[10]	G[5]	G[4]	G[2]	—	Y[2]	Y[0]	—
IPUx_DISPx_DAT11	DAT[11]	R[0]	G[5]	G[3]	—	Y[3]	Y[1]	—
IPUx_DISPx_DAT12	DAT[12]	R[1]	R[0]	G[4]	—	Y[4]	Y[2]	—
IPUx_DISPx_DAT13	DAT[13]	R[2]	R[1]	G[5]	—	Y[5]	Y[3]	—
IPUx_DISPx_DAT14	DAT[14]	R[3]	R[2]	G[6]	—	Y[6]	Y[4]	—
IPUx_DISPx_DAT15	DAT[15]	R[4]	R[3]	G[7]	—	Y[7]	Y[5]	—
IPUx_DISPx_DAT16	DAT[16]	—	R[4]	R[0]	—	—	Y[6]	—
IPUx_DISPx_DAT17	DAT[17]	—	R[5]	R[1]	—	—	Y[7]	—
IPUx_DISPx_DAT18	DAT[18]	—	—	R[2]	—	—	Y[8]	—
IPUx_DISPx_DAT19	DAT[19]	—	—	R[3]	—	—	Y[9]	—
IPUx_DISPx_DAT20	DAT[20]	—	—	R[4]	—	—	—	—
IPUx_DISPx_DAT21	DAT[21]	—	—	R[5]	—	—	—	—
IPUx_DISPx_DAT22	DAT[22]	—	—	R[6]	—	—	—	—
IPUx_DISPx_DAT23	DAT[23]	—	—	R[7]	—	—	—	—
IPUx_Dlx_DISP_CLK	PixCLK							—
IPUx_Dlx_PIN01	—							May be required for anti-tearing
IPUx_Dlx_PIN02	HSYNC							—
IPUx_Dlx_PIN03	VSYNC							VSYNC out

4.12.12.9 Low-Power Receiver Timing

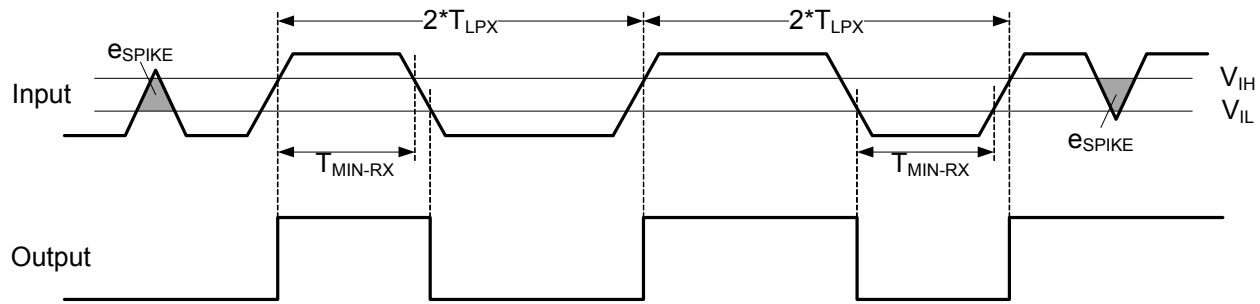


Figure 72. Input Glitch Rejection of Low-Power Receivers

4.12.13 HSI Host Controller Timing Parameters

This section describes the timing parameters of the HSI Host Controller which are compliant with High-Speed Synchronous Serial Interface (HSI) Physical Layer specification version 1.01.

4.12.13.1 Synchronous Data Flow

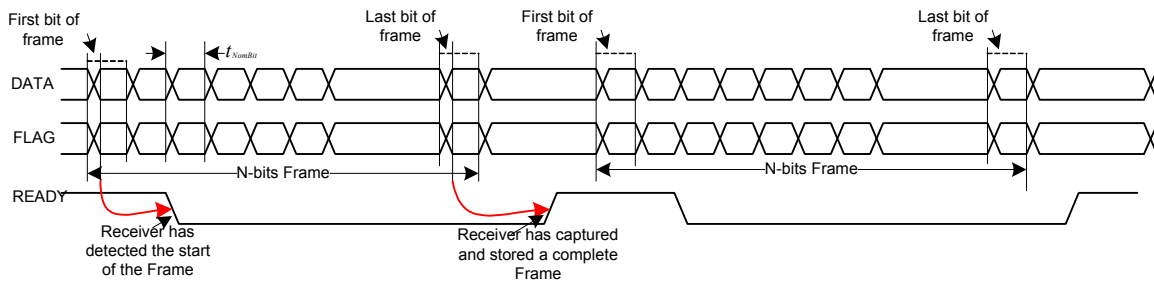


Figure 73. Synchronized Data Flow READY Signal Timing (Frame and Stream Transmission)

4.12.13.2 Pipelined Data Flow

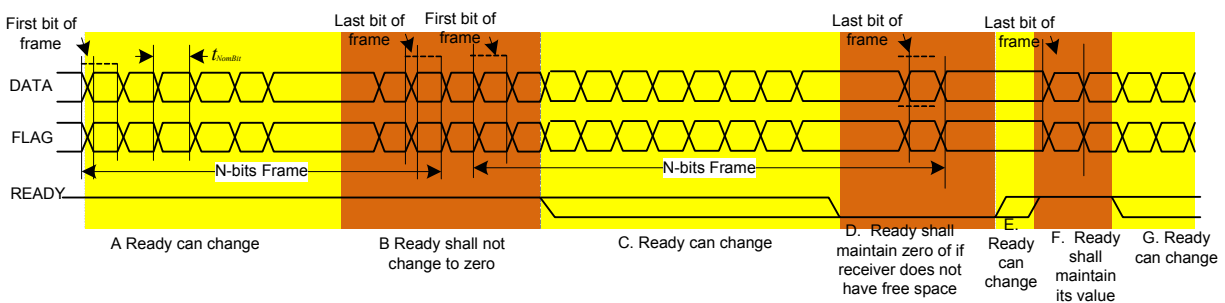


Figure 74. Pipelined Data Flow READY Signal Timing (Frame Transmission Mode)

4.12.20 SSI Timing Parameters

This section describes the timing parameters of the SSI module. The connectivity of the serial synchronous interfaces are summarized in [Table 81](#).

Table 81. AUDMUX Port Allocation

Port	Signal Nomenclature	Type and Access
AUDMUX port 1	SSI 1	Internal
AUDMUX port 2	SSI 2	Internal
AUDMUX port 3	AUD3	External – AUD3 I/O
AUDMUX port 4	AUD4	External – EIM or CSPI1 I/O through IOMUXC
AUDMUX port 5	AUD5	External – EIM or SD1 I/O through IOMUXC
AUDMUX port 6	AUD6	External – EIM or DISP2 through IOMUXC
AUDMUX port 7	SSI 3	Internal

NOTE

The terms WL and BL used in the timing diagrams and tables refer to Word Length (WL) and Bit Length (BL).

4.12.20.1 SSI Transmitter Timing with Internal Clock

[Figure 90](#) depicts the SSI transmitter internal clock timing and [Table 82](#) lists the timing parameters for the SSI transmitter internal clock.

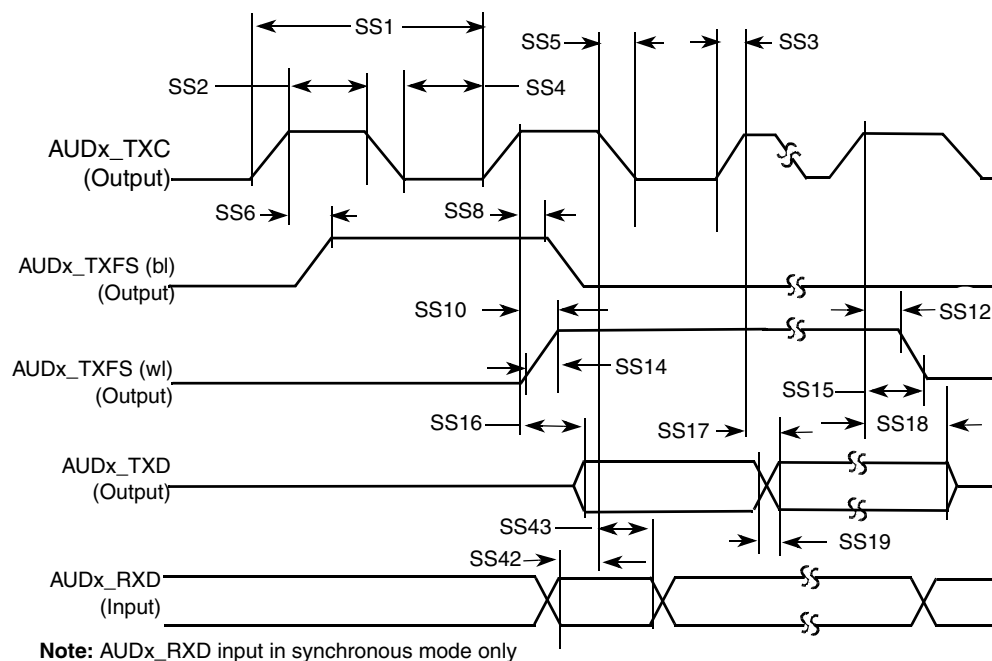


Figure 90. SSI Transmitter Internal Clock Timing Diagram

Table 93. Fuses and Associated Pins Used for Boot (continued)

Pin	Direction at Reset	eFuse Name
EIM_A18	Input	BOOT_CFG3[2]
EIM_A19	Input	BOOT_CFG3[3]
EIM_A20	Input	BOOT_CFG3[4]
EIM_A21	Input	BOOT_CFG3[5]
EIM_A22	Input	BOOT_CFG3[6]
EIM_A23	Input	BOOT_CFG3[7]
EIM_A24	Input	BOOT_CFG4[0]
EIM_WAIT	Input	BOOT_CFG4[1]
EIM_LBA	Input	BOOT_CFG4[2]
EIM_EB0	Input	BOOT_CFG4[3]
EIM_EB1	Input	BOOT_CFG4[4]
EIM_RW	Input	BOOT_CFG4[5]
EIM_EB2	Input	BOOT_CFG4[6]
EIM_EB3	Input	BOOT_CFG4[7]

¹ Pin value overrides fuse settings for BT_FUSE_SEL = '0'. Signal Configuration as Fuse Override Input at Power Up. These are special I/O lines that control the boot up configuration during product development. In production, the boot configuration can be controlled by fuses.

5.2 Boot Devices Interfaces Allocation

Table 94 lists the interfaces that can be used by the boot process in accordance with the specific boot mode configuration. The table also describes the interface's specific modes and IOMUXC allocation, which are configured during boot when appropriate.

Table 94. Interfaces Allocation During Boot

Interface	IP Instance	Allocated Pads During Boot	Comment
SPI	ECSPI-1	EIM_D17, EIM_D18, EIM_D16, EIM_EB2, EIM_D19, EIM_D24, EIM_D25	—
SPI	ECSPI-2	CSIO_DAT10, CSIO_DAT9, CSIO_DAT8, CSIO_DAT11, EIM_LBA, EIM_D24, EIM_D25	—
SPI	ECSPI-3	DISP0_DAT2, DISP0_DAT1, DISP0_DAT0, DISP0_DAT3, DISP0_DAT4, DISP0_DAT5, DISP0_DAT6	—
SPI	ECSPI-4	EIM_D22, EIM_D28, EIM_D21, EIM_D20, EIM_A25, EIM_D24, EIM_D25	—
SPI	ECSPI-5	SD1_DAT0, SD1_CMD, SD1_CLK, SD1_DAT1, SD1_DAT2, SD1_DAT3, SD2_DAT3	—
EIM	EIM	EIM_DA[15:0], EIM_D[31:16], CSIO_DAT[19:4], CSIO_DATA_EN, CSIO_VSYNC	Used for NOR, OneNAND boot Only CS0 is supported

Table 95. 21 x 21 mm Supplies Contact Assignment (continued)

Supply Rail Name	Ball(s) Position(s)	Remark
VDDHIGH_CAP	H10, J10	Secondary supply for the 2.5 V domain (internal regulator output—requires capacitor if internal regulator is used)
VDDHIGH_IN	H9, J9	Primary supply for the 2.5 V regulator
VDDPU_CAP	H17, J17, K17, L17, M17, N17, P17	Secondary supply for the VPU and GPU (internal regulator output—requires capacitor if internal regulator is used)
VDDSOC_CAP	R10, T10, T13, T14, U10, U13, U14	Secondary supply for the SoC and PU (internal regulator output—requires capacitor if internal regulator is used)
VDDSOC_IN	H16, J16, K16, L16, M16, N16, P16, R16, T16, U16	Primary supply for the SoC and PU regulators
VDDUSB_CAP	F9	Secondary supply for the 3 V domain (internal regulator output—requires capacitor if internal regulator is used)
ZQPAD	AE17	Connect ZQPAD to an external 240Ω 1% resistor to GND. This is a reference used during DRAM output buffer driver calibration.

6.2.3 21 x 21 mm Functional Contact Assignments

Table 96 displays an alpha-sorted list of the signal assignments including power rails. The table also includes out of reset pad state.

Table 96. 21 x 21 mm Functional Contact Assignments

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition ¹			
				Default Mode (Reset Mode)	Default Function (Signal Name)	Input/Output	Value ²
BOOT_MODE0	C12	VDD_SNVS_IN	GPIO	ALT0	SRC_BOOT_MODE0	Input	PD (100K)
BOOT_MODE1	F12	VDD_SNVS_IN	GPIO	ALT0	SRC_BOOT_MODE1	Input	PD (100K)
CLK1_N	C7	VDD_HIGH_CAP	—	—	CLK1_N	—	—
CLK1_P	D7	VDD_HIGH_CAP	—	—	CLK1_P	—	—
CLK2_N	C5	VDD_HIGH_CAP	—	—	CLK2_N	—	—
CLK2_P	D5	VDD_HIGH_CAP	—	—	CLK2_P	—	—
CSI_CLK0M	F4	NVCC_MIPI	—	—	CSI_CLK_N	—	—
CSI_CLK0P	F3	NVCC_MIPI	—	—	CSI_CLK_P	—	—
CSI_D0M	E4	NVCC_MIPI	—	—	CSI_DATA0_N	—	—
CSI_D0P	E3	NVCC_MIPI	—	—	CSI_DATA0_P	—	—
CSI_D1M	D1	NVCC_MIPI	—	—	CSI_DATA1_N	—	—

Table 96. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition ¹			
				Default Mode (Reset Mode)	Default Function (Signal Name)	Input/Output	Value ²
DRAM_CS1	AD17	NVCC_DRAM	DDR	ALT0	DRAM_CS1_B	Output	0
DRAM_D0	AD2	NVCC_DRAM	DDR	ALT0	DRAM_DATA00	Input	PU (100K)
DRAM_D1	AE2	NVCC_DRAM	DDR	ALT0	DRAM_DATA01	Input	PU (100K)
DRAM_D10	AA6	NVCC_DRAM	DDR	ALT0	DRAM_DATA10	Input	PU (100K)
DRAM_D11	AE7	NVCC_DRAM	DDR	ALT0	DRAM_DATA11	Input	PU (100K)
DRAM_D12	AB5	NVCC_DRAM	DDR	ALT0	DRAM_DATA12	Input	PU (100K)
DRAM_D13	AC5	NVCC_DRAM	DDR	ALT0	DRAM_DATA13	Input	PU (100K)
DRAM_D14	AB6	NVCC_DRAM	DDR	ALT0	DRAM_DATA14	Input	PU (100K)
DRAM_D15	AC7	NVCC_DRAM	DDR	ALT0	DRAM_DATA15	Input	PU (100K)
DRAM_D16	AB7	NVCC_DRAM	DDR	ALT0	DRAM_DATA16	Input	PU (100K)
DRAM_D17	AA8	NVCC_DRAM	DDR	ALT0	DRAM_DATA17	Input	PU (100K)
DRAM_D18	AB9	NVCC_DRAM	DDR	ALT0	DRAM_DATA18	Input	PU (100K)
DRAM_D19	Y9	NVCC_DRAM	DDR	ALT0	DRAM_DATA19	Input	PU (100K)
DRAM_D2	AC4	NVCC_DRAM	DDR	ALT0	DRAM_DATA02	Input	PU (100K)
DRAM_D20	Y7	NVCC_DRAM	DDR	ALT0	DRAM_DATA20	Input	PU (100K)
DRAM_D21	Y8	NVCC_DRAM	DDR	ALT0	DRAM_DATA21	Input	PU (100K)
DRAM_D22	AC8	NVCC_DRAM	DDR	ALT0	DRAM_DATA22	Input	PU (100K)
DRAM_D23	AA9	NVCC_DRAM	DDR	ALT0	DRAM_DATA23	Input	PU (100K)
DRAM_D24	AE9	NVCC_DRAM	DDR	ALT0	DRAM_DATA24	Input	PU (100K)
DRAM_D25	Y10	NVCC_DRAM	DDR	ALT0	DRAM_DATA25	Input	PU (100K)
DRAM_D26	AE11	NVCC_DRAM	DDR	ALT0	DRAM_DATA26	Input	PU (100K)
DRAM_D27	AB11	NVCC_DRAM	DDR	ALT0	DRAM_DATA27	Input	PU (100K)
DRAM_D28	AC9	NVCC_DRAM	DDR	ALT0	DRAM_DATA28	Input	PU (100K)
DRAM_D29	AD9	NVCC_DRAM	DDR	ALT0	DRAM_DATA29	Input	PU (100K)
DRAM_D3	AA5	NVCC_DRAM	DDR	ALT0	DRAM_DATA03	Input	PU (100K)
DRAM_D30	AD11	NVCC_DRAM	DDR	ALT0	DRAM_DATA30	Input	PU (100K)
DRAM_D31	AC11	NVCC_DRAM	DDR	ALT0	DRAM_DATA31	Input	PU (100K)
DRAM_D32	AA17	NVCC_DRAM	DDR	ALT0	DRAM_DATA32	Input	PU (100K)
DRAM_D33	AA18	NVCC_DRAM	DDR	ALT0	DRAM_DATA33	Input	PU (100K)
DRAM_D34	AC18	NVCC_DRAM	DDR	ALT0	DRAM_DATA34	Input	PU (100K)
DRAM_D35	AE19	NVCC_DRAM	DDR	ALT0	DRAM_DATA35	Input	PU (100K)
DRAM_D36	Y17	NVCC_DRAM	DDR	ALT0	DRAM_DATA36	Input	PU (100K)
DRAM_D37	Y18	NVCC_DRAM	DDR	ALT0	DRAM_DATA37	Input	PU (100K)
DRAM_D38	AB19	NVCC_DRAM	DDR	ALT0	DRAM_DATA38	Input	PU (100K)
DRAM_D39	AC19	NVCC_DRAM	DDR	ALT0	DRAM_DATA39	Input	PU (100K)
DRAM_D4	AC1	NVCC_DRAM	DDR	ALT0	DRAM_DATA04	Input	PU (100K)

6.2.5 21 x 21 mm, 0.8 mm Pitch Ball Map

Table 98 shows the FCPBGA 21 x 21 mm, 0.8 mm pitch ball map.

Table 98. 21 x 21 mm, 0.8 mm Pitch Ball Map

G	F	E	D	C	B	A	
DSI_D0P	CSI_D3P	CSI_D2M	CSI_D1M	GND	PCIE_RXM		1
DSI_D0M	CSI_D3M	CSI_D2P	CSI_D1P	JTAG_TRSTB	PCIE_RXP	PCIE_REXT	2
GND	CSI_CLK0P	CSI_D0P	GND	JTAG_TMS	PCIE_TXP	PCIE_TXM	3
DSI_REXT	CSI_CLK0M	CSI_D0M	CSI_REXT	GND	GND	GND	4
JTAG_TDI	GND	GND	CLK2_P	CLK2_N	VDD_FA	FA_ANA	5
JTAG_TDO	GND	GND	GND	GND	USB_OTG_DN	USB_OTG_DP	6
PCIE_VPH	GND	GND	CLK1_P	CLK1_N	XTALO	XTALI	7
PCIE_VPTX	GND	NVCC_PLL_OUT	GND	GPANAIO	USB_OTG_CHD_B	GND	8
VDD_SNV5_CAP	VDDUSB_CAP	USB_OTG_VBUS	RTC_XTALI	RTC_XTALO	MLB_SP	MLB_SN	9
GND	USB_H1_DN	USB_H1_DP	USB_H1_VBUS	GND	MLB_DN	MLB_DP	10
VDD_SNV5_IN	PMIC_STBY_REQ	TAMPER	PMIC_ON_REQ	POR_B	MLB_CP	MLB_CN	11
SATA_VPH	BOOT_MODE1	TEST_MODE	ONOFF	BOOT_MODE0	SATA_TXM	SATA_TXP	12
SATA_VP	SD3_DAT7	SD3_DAT6	SD3_DAT4	SD3_DAT5	SD3_CMD	GND	13
NVCC_SD3	SD3_DAT1	SD3_DAT0	SD3_CLK	SATA_REXT	SATA_RXP	SATA_RXM	14
NVCC_NANDF	NANDF_CS0	NANDF_WP_B	SD3_RST	NANDF_CLE	SD3_DAT3	SD3_DAT2	15
NVCC_SD1	NANDF_D2	SD4_CLK	NANDF_CS3	NANDF_CS1	NANDF_RB0	NANDF_ALE	16
NVCC_SD2	SD4_DAT2	NANDF_D6	NANDF_D3	NANDF_D1	SD4_CMD	NANDF_CS2	17
NVCC_RGMII	SD1_DAT3	SD4_DAT4	SD4_DAT0	NANDF_D7	NANDF_D5	NANDF_D0	18
GND	SD2_CMD	SD1_DAT2	SD4_DAT7	SD4_DAT5	SD4_DAT1	NANDF_D4	19
EIM_D20	RGMII_TD1	SD2_DAT1	SD1_CLK	SD1_DAT1	SD4_DAT6	SD4_DAT3	20
EIM_D19	EIM_D17	RGMII_TD2	RGMII_TXC	SD2_CLK	SD1_CMD	SD1_DAT0	21
EIM_D25	EIM_D24	EIM_EB2	RGMII_RX_CTL	RGMII_TD0	SD2_DAT3	SD2_DAT0	22
EIM_D28	EIM_EB3	EIM_D22	RGMII_RD3	RGMII_TX_CTL	RGMII_RD1	SD2_DAT2	23
EIM_A17	EIM_A22	EIM_D26	EIM_D18	RGMII_RD0	RGMII_RD2	RGMII_TD3	24
EIM_A19	EIM_A24	EIM_D27	EIM_D23	EIM_D16	RGMII_RXC	GND	25

Table 99. i.MX 6Dual/6Quad Data Sheet Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
4	07/2015	- Added footnote to Table 1, "Example Orderable Part Numbers," on page 3: If a 24 MHz input clock is used (required for USB), the maximum SoC speed is limited to 996 MHz. Section 1.2, "Features" changed Five UARTs, from <i>up to 4.0 Mbps</i>, to <i>up to 5.0 Mbps</i>. Table 6, "Operating Ranges," on page 23: Row: VDD_HIGH internal regulator, changed minimum parameter value from 2.8 to 2.7V. Table 6, "Operating Ranges," on page 23: Removed footnote: <i>VDDSOC and VDDPU output voltages must be set according to this rule: VDDARM-VDDSOC/PU<50mV</i>. This was a duplicate footnote, renumbered footnotes accordingly. Table 6, "Operating Ranges," on page 23: Changed value: <i>Standby/DSM Mode, VDD_SOC_IN, minimum voltage, from 0.9V to 1.05V</i>. Table 8, "Maximum Supply Currents," on page 27, Differentiated VDD_ARM_IN, VDD_ARM23_IN, and VDD_SOC_IN by frequency and by Power Virus/CoreMark maximum current. Table 21, "XTALI and RTC_XTALI DC Parameters," on page 39, Added rows: <i>Input capacitance; Startup current; and DC input current</i> and their values. Table 41, "EIM Bus Timing Parameters," on page 55, Changed WE4–WE17 minimum and maximum parameter values from, $0.5 t(k+1)/2 - 1.25$, to $0.5 \times t \times (k+1) - 1.25$. Table 42, "EIM Asynchronous Timing Parameters Relative to Chip Select," on page 62 Added to end of formulas in the minimum, typical, and maximum parameter values for WE31–WE42 and WE45–WE46, $\times t$. For example from 3-CSN, to 3-CSN$\times t$. Also added maximum value to MAXDTI of 10. Table 58, "DDR3/DDR3L Write Cycle," on page 90, Changed minimum parameter value of DDR17 from 240 to 125; and of DDR18 from 240 to 150. Figure 29, "LPDDR2 Command and Address Timing Diagram," on page 91, LP2 signal cycle reduced. Table 62, "LPDDR2 Write Cycle," on page 93, Changed LP21 minimum and maximum parameter value from -0.25/+0.25 to 0.8/1.2. Figure 35, "ECSPI Master Mode Timing Diagram," on page 74, Added footnote: <i>Note: ECSPi_x_MOSI is always driven (not tri-stated) between actual data transmissions. This limits the ECSPi to be connected between a single master and a single slave.</i> Figure 36, "ECSPI Slave Mode Timing Diagram," on page 75, Added footnote: <i>Note: ECSPi_x_MISO is always driven (not tri-stated) between actual data transmissions. This limits the ECSPi to be connected between a single master and a single slave.</i> Figure 59, "Gated Clock Mode Timing Diagram," on page 96, Corrected IPU2_CSi_x_HSYNC trace drawing. Section 4.12.23, "USB PHY Parameters" Specified <i>Battery Charging Specification</i> applies to portable devices only. (Revision History table continues on next page.)



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