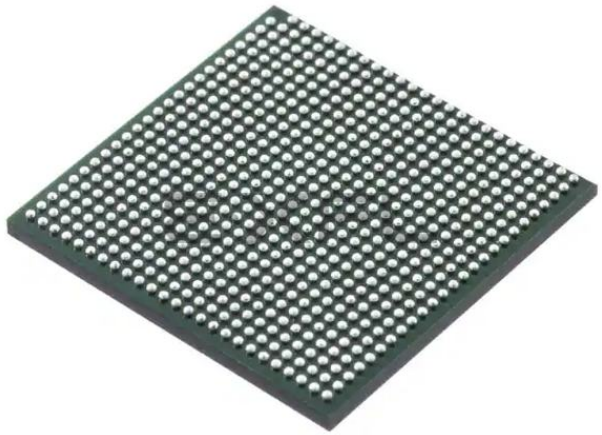

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	4 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (1)
SATA	SATA 3Gbps (1)
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-40°C ~ 125°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	624-FBGA, FCBGA
Supplier Device Package	624-FCBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6q6avt10ae

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
CSI	MIPI CSI-2 Interface	Multimedia Peripherals	The CSI IP provides MIPI CSI-2 standard camera interface port. The CSI-2 interface supports up to 1 Gbps for up to 3 data lanes and up to 800 Mbps for 4 data lanes.
CSU	Central Security Unit	Security	The Central Security Unit (CSU) is responsible for setting comprehensive security policy within the i.MX 6Dual/6Quad platform. The Security Control Registers (SCR) of the CSU are set during boot time by the HAB and are locked to prevent further writing.
CTI-0 CTI-1 CTI-2 CTI-3 CTI-4	Cross Trigger Interfaces	Debug / Trace	Cross Trigger Interfaces allows cross-triggering based on inputs from masters attached to CTIs. The CTI module is internal to the Cortex-A9 Core Platform.
CTM	Cross Trigger Matrix	Debug / Trace	Cross Trigger Matrix IP is used to route triggering events between CTIs. The CTM module is internal to the Cortex-A9 Core Platform.
DAP	Debug Access Port	System Control Peripherals	The DAP provides real-time access for the debugger without halting the core to: • System memory and peripheral registers • All debug configuration registers The DAP also provides debugger access to JTAG scan chains. The DAP module is internal to the Cortex-A9 Core Platform.
DCIC-0 DCIC-1	Display Content Integrity Checker	Automotive IP	The DCIC provides integrity check on portion(s) of the display. Each i.MX 6Dual/6Quad processor has two such modules, one for each IPU.
DSI	MIPI DSI interface	Multimedia Peripherals	The MIPI DSI IP provides DSI standard display port interface. The DSI interface support 80 Mbps to 1 Gbps speed per data lane.
DTCP	DTCP	MM	Provides encryption function according to Digital Transmission Content Protection standard for traffic over MLB150.
eCSPI1-5	Configurable SPI	Connectivity Peripherals	Full-duplex enhanced Synchronous Serial Interface. It is configurable to support Master/Slave modes, four chip selects to support multiple peripherals.
ENET	Ethernet Controller	Connectivity Peripherals	The Ethernet Media Access Controller (MAC) is designed to support 10/100/1000 Mbps Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The i.MX 6Dual/6Quad processors also consist of hardware assist for IEEE 1588 standard. For details, see the ENET chapter of the i.MX 6Dual/6Quad reference manual (IMX6DQRM). **Note:** The theoretical maximum performance of 1 Gbps ENET is limited to 470 Mbps (total for Tx and Rx) due to internal bus throughput limitations. The actual measured performance in optimized environment is up to 400 Mbps. For details, see the ERR004512 erratum in the i.MX 6Dual/6Quad errata document (IMX6DQCE).

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
LDB	LVDS Display Bridge	Connectivity Peripherals	LVDS Display Bridge is used to connect the IPU (Image Processing Unit) to External LVDS Display Interface. LDB supports two channels; each channel has following signals: • One clock pair • Four data pairs Each signal pair contains LVDS special differential pad (PadP, PadM).
MLB150	MediaLB	Connectivity / Multimedia Peripherals	The MLB interface module provides a link to a MOST® data network, using the standardized MediaLB protocol (up to 150 Mbps). The module is backward compatible to MLB-50.
MMDC	Multi-Mode DDR Controller	Connectivity Peripherals	DDR Controller has the following features: • Supports 16/32/64-bit DDR3 / DDR3L or LPDDR2 • Supports both dual x32 for LPDDR2 and x64 DDR3 / LPDDR2 configurations (including 2x32 interleaved mode) • Supports up to 4 GByte DDR memory space
OCOTP_CTRL	OTP Controller	Security	The On-Chip OTP controller (OCOTP_CTRL) provides an interface for reading, programming, and/or overriding identification and control information stored in on-chip fuse elements. The module supports electrically-programmable poly fuses (eFUSEs). The OCOTP_CTRL also provides a set of volatile software-accessible signals that can be used for software control of hardware elements, not requiring non-volatility. The OCOTP_CTRL provides the primary user-visible mechanism for interfacing with on-chip fuse elements. Among the uses for the fuses are unique chip identifiers, mask revision numbers, cryptographic keys, JTAG secure mode, boot characteristics, and various control signals, requiring permanent non-volatility.
OCRAM	On-Chip Memory Controller	Data Path	The On-Chip Memory controller (OCRAM) module is designed as an interface between system's AXI bus and internal (on-chip) SRAM memory module. In i.MX 6Dual/6Quad processors, the OCRAM is used for controlling the 256 KB multimedia RAM through a 64-bit AXI bus.
OSC 32 kHz	OSC 32 kHz	Clocking	Generates 32.768 kHz clock from an external crystal.
PCIe	PCI Express 2.0	Connectivity Peripherals	The PCIe IP provides PCI Express Gen 2.0 functionality.
PMU	Power-Management Functions	Data Path	Integrated power management unit. Used to provide power to various SoC domains.
PWM-1 PWM-2 PWM-3 PWM-4	Pulse Width Modulation	Connectivity Peripherals	The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images and it can also generate tones. It uses 16-bit resolution and a 4x16 data FIFO to generate sound.
RAM 16 KB	Secure/non-secure RAM	Secured Internal Memory	Secure/non-secure Internal RAM, interfaced through the CAAM.
RAM 256 KB	Internal RAM	Internal Memory	Internal RAM, which is accessed through OCRAM memory controllers.

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
uSDHC-1 uSDHC-2 uSDHC-2 uSDHC-4	SD/MMC and SDXC Enhanced Multi-Media Card / Secure Digital Host Controller	Connectivity Peripherals	i.MX 6Dual/6Quad specific SoC characteristics: All four MMC/SD/SDIO controller IPs are identical and are based on the uSDHC IP. They are: • Conforms to the SD Host Controller Standard Specification version 3.0 • Fully compliant with MMC command/response sets and Physical Layer as defined in the Multimedia Card System Specification, v4.2/4.3/4.4/4.41 including high-capacity (size > 2 GB) cards HC MMC. Hardware reset as specified for eMMC cards is supported at ports #3 and #4 only. • Fully compliant with SD command/response sets and Physical Layer as defined in the SD Memory Card Specifications, v3.0 including high-capacity SDHC cards up to 32 GB and SDXC cards up to 2TB. • Fully compliant with SDIO command/response sets and interrupt/read-wait mode as defined in the SDIO Card Specification, Part E1, v1.10 • Fully compliant with SD Card Specification, Part A2, SD Host Controller Standard Specification, v2.00 All four ports support: • 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR104 mode (104 MB/s max) • 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max) However, the SoC-level integration and I/O muxing logic restrict the functionality to the following: • Instances #1 and #2 are primarily intended to serve as external slots or interfaces to on-board SDIO devices. These ports are equipped with “Card Detection” and “Write Protection” pads and do not support hardware reset. • Instances #3 and #4 are primarily intended to serve interfaces to embedded MMC memory or interfaces to on-board SDIO devices. These ports do not have “Card detection” and “Write Protection” pads and do support hardware reset. • All ports can work with 1.8 V and 3.3 V cards. There are two completely independent I/O power domains for Ports #1 and #2 in four bit configuration (SD interface). Port #3 is placed in his own independent power domain and port #4 shares power domain with some other interfaces.
VDOA	VDOA	Multimedia Peripherals	The Video Data Order Adapter (VDOA) is used to re-order video data from the “tiled” order used by the VPU to the conventional raster-scan order needed by the IPU.
VPU	Video Processing Unit	Multimedia Peripherals	A high-performing video processing unit (VPU), which covers many SD-level and HD-level video decoders and SD-level encoders as a multi-standard video codec engine as well as several important video processing, such as rotation and mirroring. See the i.MX 6Dual/6Quad reference manual (IMX6DQRM) for complete list of VPU’s decoding/encoding capabilities.
WDOG-1	Watchdog	Timer Peripherals	The Watchdog Timer supports two comparison points during each counting period. Each of the comparison points is configurable to evoke an interrupt to the ARM core, and a second point evokes an external event on the WDOG line.

4 Electrical Characteristics

This section provides the device and module-level electrical characteristics for the i.MX 6Dual/6Quad processors.

4.1 Chip-Level Conditions

This section provides the device-level electrical characteristics for the SoC. See Table 3 for a quick reference to the individual tables and sections.

Table 3. i.MX 6Dual/6Quad Chip-Level Conditions

For these characteristics, …	Topic appears …
Absolute Maximum Ratings	on page 21
FCPBGA Package Thermal Resistance	on page 22
Operating Ranges	on page 23
External Clock Sources	on page 25
Maximum Measured Supply Currents	on page 27
Low Power Mode Supply Currents	on page 28
USB PHY Current Consumption	on page 30
SATA Typical Power Consumption	on page 30
PCIe 2.0 Maximum Power Consumption	on page 31
HDMI Maximum Power Consumption	on page 32

4.1.1 Absolute Maximum Ratings

CAUTION

Stresses beyond those listed under Table 4 may affect reliability or cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the Operating Ranges or Parameters tables is not implied.

Table 8. Maximum Supply Currents (continued)

Power Supply	Conditions	Maximum Current		Unit
		Power Virus	CoreMark	
NVCC_LVDS2P5	—	NVCC_LVDS2P5 is connected to VDD_HIGH_CAP at the board level. VDD_HIGH_CAP is capable of handing the current required by NVCC_LVDS2P5.		
MISC				
DRAM_VREF	—	1		mA

1 The actual maximum current drawn from VDD_HIGH_IN will be as shown plus any additional current drawn from the VDD_HIGH_CAP outputs, depending upon actual application configuration (for example, NVCC_LVDS_2P5, NVCC_MIPI, or HDMI, PCIe, and SATA VPH supplies).

2 Under normal operating conditions, the maximum current on VDD_SNVS_IN is shown Table 8. The maximum VDD_SNVS_IN current may be higher depending on specific operating configurations, such as BOOT_MODE[1:0] not equal to 00, or use of the Tamper feature. During initial power on, VDD_SNVS_IN can draw up to 1 mA if the supply is capable of sourcing that current. If less than 1 mA is available, the VDD_SNVS_CAP charge time will increase.

3 This is the maximum current per active USB physical interface.

4 The DRAM power consumption is dependent on several factors such as external signal termination. DRAM power calculators are typically available from memory vendors which take into account factors such as signal termination.
See the *i.MX 6Dual/6Quad Power Consumption Measurement Application Note* (AN4509) for examples of DRAM power consumption during specific use case scenarios.

5 General equation for estimated, maximum power consumption of an IO power supply:
Imax = N x C x V x (0.5 x F)
Where:
N—Number of IO pins supplied by the power line
C—Equivalent external capacitive load
V—IO voltage
(0.5 xF)—Data change rate. Up to 0.5 of the clock rate (F)
In this equation, Imax is in Amps, C in Farads, V in Volts, and F in Hertz.

4.1.6 Low Power Mode Supply Currents

Table 9 shows the current core consumption (not including I/O) of the i.MX 6Dual/6Quad processors in selected low power modes.

Table 9. Stop Mode Current and Power Consumption

Mode	Test Conditions	Supply	Typical[1]	Unit
WAIT	• ARM, SoC, and PU LDOs are set to 1.225 V • HIGH LDO set to 2.5 V • Clocks are gated • DDR is in self refresh • PLLs are active in bypass (24 MHz) • Supply voltages remain ON	VDD_ARM_IN (1.4 V)	6	mA
		VDD_SOC_IN (1.4 V)	23	mA
		VDD_HIGH_IN (3.0 V)	3.7	mA
		Total	52	mW

CAUTION

The internal RTC oscillator does not provide an accurate frequency and is affected by process, voltage, and temperature variations. NXP strongly recommends using an external crystal as the RTC_XTALI reference. If the internal oscillator is used instead, careful consideration must be given to the timing implications on all of the SoC modules dependent on this clock.

The OSC32k runs from VDD_SNVS_CAP, which comes from the VDD_HIGH_IN/VDD_SNVS_IN power mux.

Table 20. OSC32K Main Characteristics

Parameter	Min	Typ	Max	Comments
Fosc	—	32.768 kHz	—	This frequency is nominal and determined mainly by the crystal selected. 32.0 K would work as well.
Current consumption	—	4 μA	—	The typical value shown is only for the oscillator, driven by an external crystal. If the internal ring oscillator is used instead of an external crystal, then approximately 25 μA must be added to this value.
Bias resistor	—	14 MΩ	—	This the integrated bias resistor that sets the amplifier into a high gain state. Any leakage through the ESD network, external board leakage, or even a scope probe that is significant relative to this value will debias the amplifier. The debiasing will result in low gain, and will impact the circuit's ability to start up and maintain oscillations.
Target Crystal Properties				
Cload	—	10 pF	—	Usually crystals can be purchased tuned for different Cloads. This Cload value is typically 1/2 of the capacitances realized on the PCB on either side of the quartz. A higher Cload will decrease oscillation margin, but increases current oscillating through the crystal.
ESR	—	50 kΩ	100 kΩ	Equivalent series resistance of the crystal. Choosing a crystal with a higher value will decrease the oscillating margin.

4.6 I/O DC Parameters

This section includes the DC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2 and DDR3/DDR3L modes
- LVDS I/O
- MLB I/O

NOTE

The term ‘OVDD’ in this section refers to the associated supply rail of an input or output.

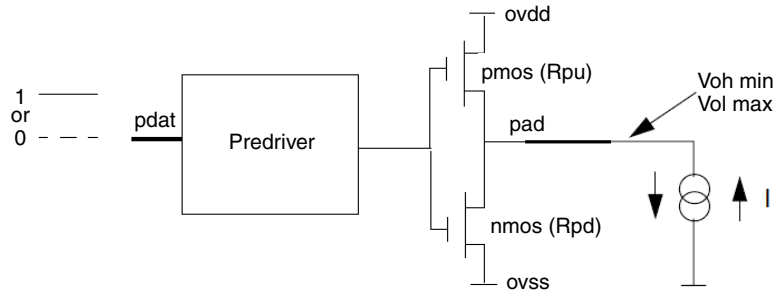

Figure 3. Circuit for Parameters Voh and Vol for I/O Cells

4.6.1 XTALI and RTC_XTALI (Clock Inputs) DC Parameters

Table 21 shows the DC parameters for the clock inputs.

Table 21. XTALI and RTC_XTALI DC Parameters

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
XTALI high-level DC input voltage	Vih	—	0.8 x NVCC_PLL_OUT	—	NVCC_PLL_ OUT	V
XTALI low-level DC input voltage	Vil	—	0	—	0.2	V
RTC_XTALI high-level DC input voltage	Vih	—	0.8	—	1.1 (See note 1)	V
RTC_XTALI low-level DC input voltage	Vil	—	0	—	0.2	V
Input capacitance	C_{IN}	Simulated data	—	5	—	pF
XTALI input leakage current at startup	$I_{XTALI\_STARTUP}$	Power-on startup for 0.15 msec with a driven 32 KHz RTC clock @ 1.1 V. [2]	—	—	600	µA
DC input current	I_{XTALI_DC}	—	—	—	2.5	µA

[1] This voltage specification must not be exceeded and, as such, is an absolute maximum specification.

[2] This current draw is present even if an external clock source directly drives XTALI.

NOTE

The Vil and Vih specifications only apply when an external clock source is used. If a crystal is used, Vil and Vih do not apply.

4.6.2 General Purpose I/O (GPIO) DC Parameters

Table 22 shows DC parameters for GPIO pads. The parameters in Table 22 are guaranteed per the operating ranges in Table 6, unless otherwise noted.

4.7.1 General Purpose I/O AC Parameters

The I/O AC parameters for GPIO in slow and fast modes are presented in the Table 28 and Table 29, respectively. Note that the fast or slow I/O behavior is determined by the appropriate control bits in the IOMUXC control registers.

Table 28. General Purpose I/O AC Parameters 1.8 V Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times, rise/fall (Max Drive, DSE=111)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	2.72/2.79 1.51/1.54	ns
Output Pad Transition Times, rise/fall (High Drive, DSE=101)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.20/3.36 1.96/2.07	
Output Pad Transition Times, rise/fall (Medium Drive, DSE=100)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.64/3.88 2.27/2.53	
Output Pad Transition Times, rise/fall (Low Drive. DSE=011)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	4.32/4.50 3.16/3.17	
Input Transition Times[1]	trm	—	—	—	25	ns

1 Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

Table 29. General Purpose I/O AC Parameters 3.3 V Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times, rise/fall (Max Drive, DSE=101)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	1.70/1.79 1.06/1.15	ns
Output Pad Transition Times, rise/fall (High Drive, DSE=011)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	2.35/2.43 1.74/1.77	
Output Pad Transition Times, rise/fall (Medium Drive, DSE=010)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.13/3.29 2.46/2.60	
Output Pad Transition Times, rise/fall (Low Drive. DSE=001)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	5.14/5.57 4.77/5.15	
Input Transition Times[1]	trm	—	—	—	25	ns

1 Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

4.11.1 Asynchronous Mode AC Timing (ONFI 1.0 Compatible)

Asynchronous mode AC timings are provided as multiplications of the clock cycle and fixed delay. The Maximum I/O speed of GPMI in Asynchronous mode is about 50 MB/s. Figure 24 through Figure 27 depict the relative timing between GPMI signals at the module level for different operations under Asynchronous mode. Table 44 describes the timing parameters (NF1–NF17) that are shown in the figures.

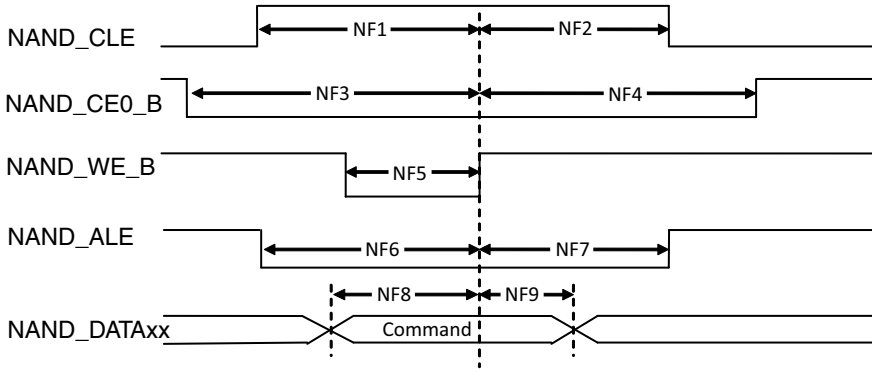

Figure 24. Command Latch Cycle Timing Diagram

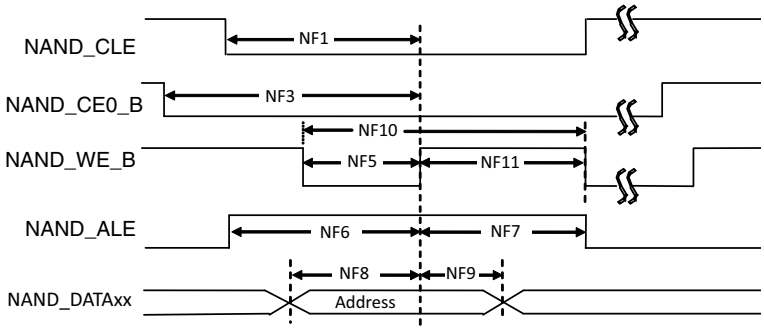

Figure 25. Address Latch Cycle Timing Diagram

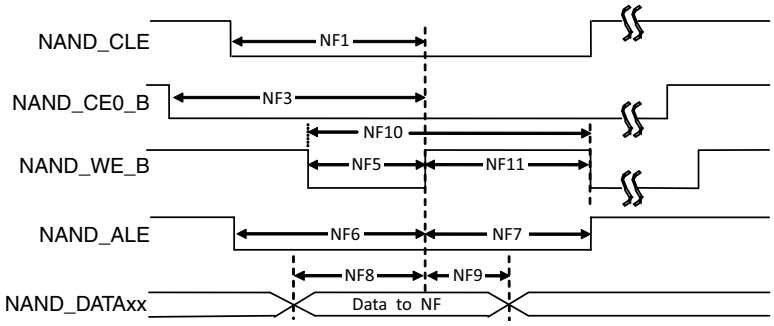

Figure 26. Write Data Latch Cycle Timing Diagram

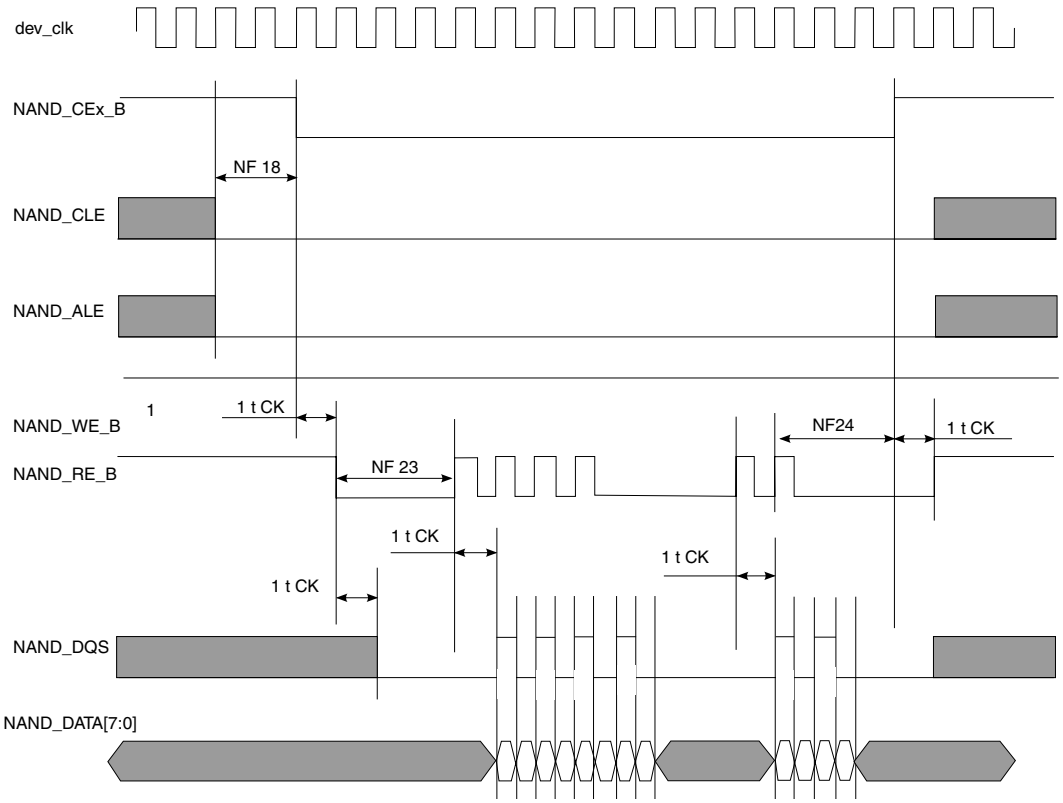

Figure 34. Samsung Toggle Mode Data Read Timing

Table 46. Samsung Toggle Mode Timing Parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min	Max	
NF1	NAND_CLE setup time	tCLS	(AS + DS) × T - 0.12 [see 2,3]		—
NF2	NAND_CLE hold time	tCLH	DH × T - 0.72 [see 2]		—
NF3	NAND_CEx_B setup time	tCS	(AS + DS) × T - 0.58 [see 3,2]		—
NF4	NAND_CEx_B hold time	tCH	DH × T - 1 [see 2]		—
NF5	NAND_WE_B pulse width	tWP	DS × T [see 2]		—
NF6	NAND_ALE setup time	tALS	(AS + DS) × T - 0.49 [see 3,2]		—
NF7	NAND_ALE hold time	tALH	DH × T - 0.42 [see 2]		—
NF8	Command/address NAND_DATAxx setup time	tCAS	DS × T - 0.26 [see 2]		—
NF9	Command/address NAND_DATAxx hold time	tCAH	DH × T - 1.37 [see 2]		—
NF18	NAND_CEx_B access time	tCE	CE_DELAY × T [see 4,2]	—	ns
NF22	clock period	tCK	—	—	ns
NF23	preamble delay	tPRE	PRE_DELAY × T [see 5,2]	—	ns
NF24	postamble delay	tPOST	POST_DELAY × T +0.43 [see 2]	—	ns

4.12.4 Ultra High Speed SD/SDIO/MMC Host Interface (uSDHC) AC Timing

This section describes the electrical information of the uSDHC, which includes SD/eMMC4.3 (Single Data Rate) timing and eMMC4.4/4.1 (Dual Date Rate) timing.

4.12.4.1 SD/eMMC4.3 (Single Data Rate) AC Timing

Figure 39 depicts the timing of SD/eMMC4.3, and Table 50 lists the SD/eMMC4.3 timing characteristics.

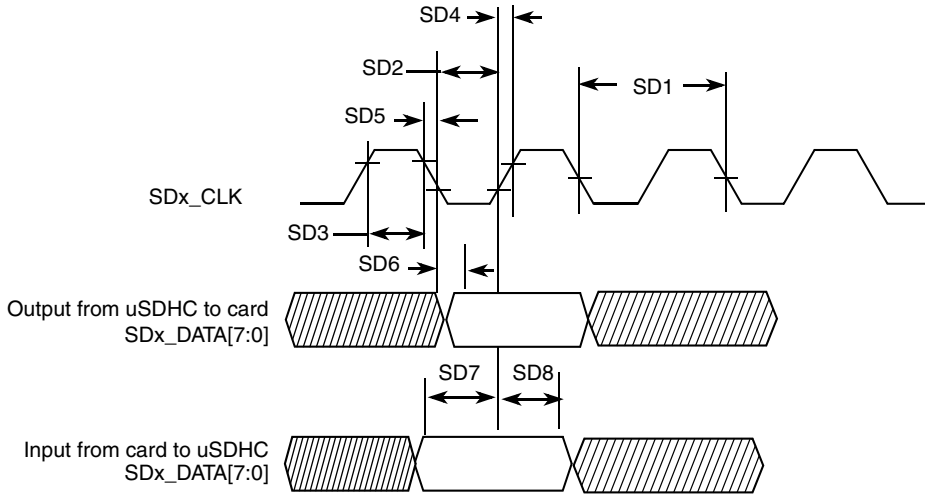

Figure 39. SD/eMMC4.3 Timing

Table 50. SD/eMMC4.3 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (Low Speed)	f_{PP}[1]	0	400	kHz
	Clock Frequency (SD/SDIO Full Speed/High Speed)	f_{PP}[2]	0	25/50	MHz
	Clock Frequency (MMC Full Speed/High Speed)	f_{PP}[3]	0	20/52	MHz
	Clock Frequency (Identification Mode)	f_{OD}	100	400	kHz
SD2	Clock Low Time	t_{WL}	7	—	ns
SD3	Clock High Time	t_{WH}	7	—	ns
SD4	Clock Rise Time	t_{TLH}	—	3	ns
SD5	Clock Fall Time	t_{THL}	—	3	ns
eSDHC Output/Card Inputs SD_CMD, SD_DATAx (Reference to SDx_CLK)					
SD6	eSDHC Output Delay	t_{OD}	–6.6	3.6	ns

Table 50. SD/eMMC4.3 Interface Timing Specification (continued)

ID	Parameter	Symbols	Min	Max	Unit
eSDHC Input/Card Outputs SD_CMD, SD_DATAx (Reference to SDx_CLK)					
SD7	eSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD8	eSDHC Input Hold Time[4]	t_{IH}	1.5	—	ns

1 In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

2 In normal (full) speed mode for SD/SDIO card, clock frequency can be any value between 0—25 MHz. In high-speed mode, clock frequency can be any value between 0—50 MHz.

3 In normal (full) speed mode for MMC card, clock frequency can be any value between 0—20 MHz. In high-speed mode, clock frequency can be any value between 0—52 MHz.

4 To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

4.12.4.2 eMMC4.4/4.41 (Dual Data Rate) eSDHCv3 AC Timing

Figure 40 depicts the timing of eMMC4.4/4.41. Table 51 lists the eMMC4.4/4.41 timing characteristics. Be aware that only SDx_DATAx is sampled on both edges of the clock (not applicable to SD_CMD).

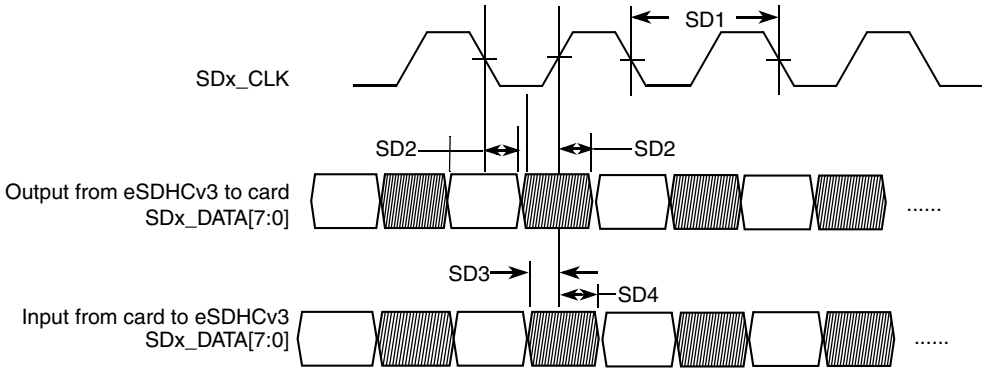

Figure 40. eMMC4.4/4.41 Timing

Table 51. eMMC4.4/4.41 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock[1]					
SD1	Clock Frequency (EMMC4.4 DDR)	f_{PP}	0	52	MHz
SD1	Clock Frequency (SD3.0 DDR)	f_{PP}	0	50	MHz
uSDHC Output / Card Inputs SD_CMD, SD_DATAx (Reference to SD_CLK)					
SD2	uSDHC Output Delay	t_{OD}	2.5	7.1	ns
uSDHC Input / Card Outputs SD_CMD, SD_DATAx (Reference to SD_CLK)					
SD3	uSDHC Input Setup Time	t_{ISU}	1.7	—	ns
SD4	uSDHC Input Hold Time	t_{IH}	1.5	—	ns

1 Clock duty cycle will be in the range of 47% to 53%.

4.12.5.3 RGMII Signal Switching Specifications

The following timing specifications meet the requirements for RGMII interfaces for a range of transceiver devices.

Table 58. RGMII Signal Switching Specifications[1]

Symbol	Description	Min	Max	Unit
T_{cyc}[2]	Clock cycle duration	7.2	8.8	ns
T_{skewT}[3]	Data to clock output skew at transmitter	-100	900	ps
T_{skewR}[3]	Data to clock input skew at receiver	1	2.6	ns
Duty_G[4]	Duty cycle for Gigabit	45	55	%
Duty_T[4]	Duty cycle for 10/100T	40	60	%
Tr/Tf	Rise/fall time (20–80%)	—	0.75	ns

1 The timings assume the following configuration:
DDR_SEL = (11)b
DSE (drive-strength) = (111)b

2 For 10 Mbps and 100 Mbps, T_{cyc} will scale to 400 ns ±40 ns and 40 ns ±4 ns respectively.

3 For all versions of RGMII prior to 2.0; This implies that PC board design will require clocks to be routed such that an additional delay of greater than 1.2 ns and less than 1.7 ns will be added to the associated clock signal. For 10/100, the max value is unspecified.

4 Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest speed transitioned between.

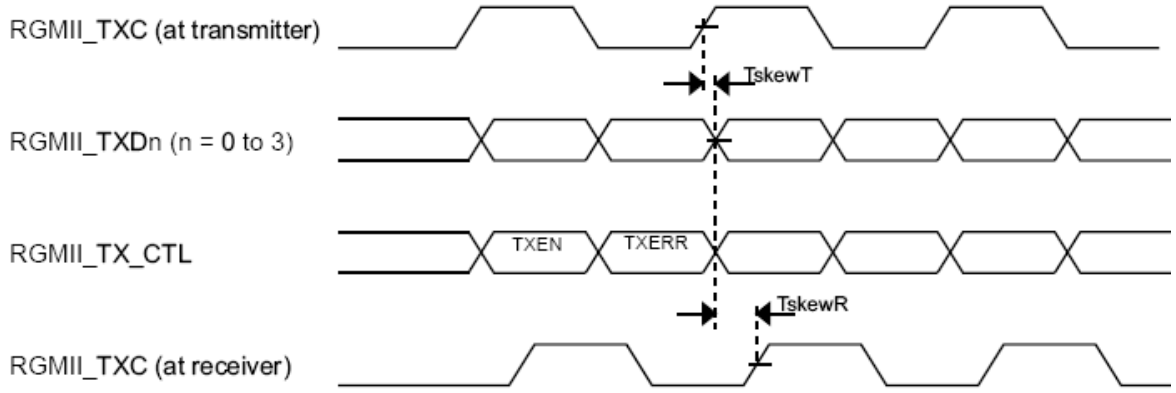

Figure 47. RGMII Transmit Signal Timing Diagram Original

4.12.12.3 HS Line Driver Characteristics

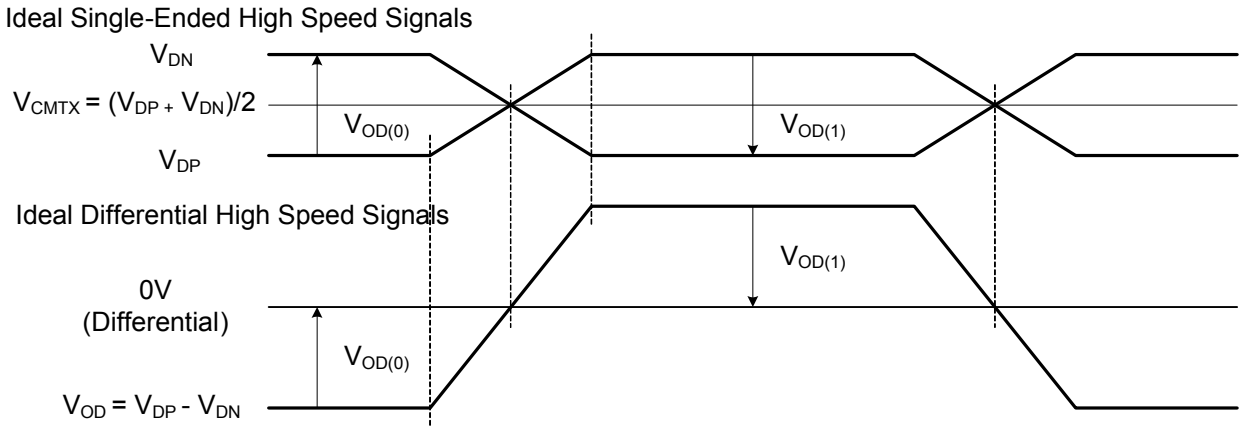

Figure 67. Ideal Single-ended and Resulting Differential HS Signals

4.12.12.4 Possible ΔVCMTX and ΔVOD Distortions of the Single-ended HS Signals

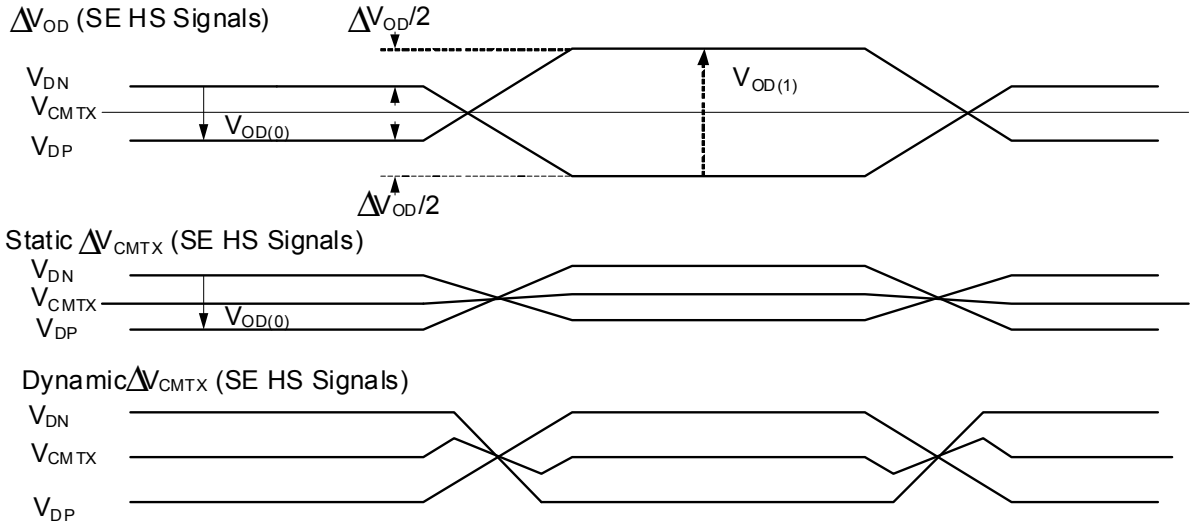

Figure 68. Possible ΔVCMTX and ΔVOD Distortions of the Single-ended HS Signals

4.12.12.5 D-PHY Switching Characteristics

Table 69. Electrical and Timing Information

Symbol	Parameters	Test Conditions	Min	Typ	Max	Unit
HS Line Drivers AC Specifications						
—	Maximum serial data rate (forward direction)	On DATAP/N outputs. 80 Ω <= RL <= 125 Ω	80	—	1000	Mbps
F_{DDRCLK}	DDR CLK frequency	On DATAP/N outputs.	40	—	500	MHz
P_{DDRCLK}	DDR CLK period	80 Ω <= RL< = 125 Ω	2	—	25	ns

Table 96. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function (Signal Name)	Input/Output	Value[2]
NANDF_WP_B	E15	NVCC_NANDF	GPIO	ALT5	GPIO6_IO09	Input	PU (100K)
ONOFF	D12	VDD_SNVS_IN	GPIO	—	SRC_ONOFF	Input	PU (100K)
PCIE_RXM	B1	PCIE_VPH	—	—	PCIE_RX_N	—	—
PCIE_RXP	B2	PCIE_VPH	—	—	PCIE_RX_P	—	—
PCIE_TXM	A3	PCIE_VPH	—	—	PCIE_TX_N	—	—
PCIE_TXP	B3	PCIE_VPH	—	—	PCIE_TX_P	—	—
PMIC_ON_REQ	D11	VDD_SNVS_IN	GPIO	ALT0	SNVS_PMIC_ON_REQ	Output	Open Drain with PU (100K)
PMIC_STBY_REQ	F11	VDD_SNVS_IN	GPIO	ALT0	CCM_PMIC_STBY_REQ	Output	0
POR_B	C11	VDD_SNVS_IN	GPIO	ALT0	SRC_POR_B	Input	PU (100K)
RGMII_RD0	C24	NVCC_RGMII	DDR	ALT5	GPIO6_IO25	Input	PU (100K)
RGMII_RD1	B23	NVCC_RGMII	DDR	ALT5	GPIO6_IO27	Input	PU (100K)
RGMII_RD2	B24	NVCC_RGMII	DDR	ALT5	GPIO6_IO28	Input	PU (100K)
RGMII_RD3	D23	NVCC_RGMII	DDR	ALT5	GPIO6_IO29	Input	PU (100K)
RGMII_RX_CTL	D22	NVCC_RGMII	DDR	ALT5	GPIO6_IO24	Input	PD (100K)
RGMII_RXC	B25	NVCC_RGMII	DDR	ALT5	GPIO6_IO30	Input	PD (100K)
RGMII_TD0	C22	NVCC_RGMII	DDR	ALT5	GPIO6_IO20	Input	PU (100K)
RGMII_TD1	F20	NVCC_RGMII	DDR	ALT5	GPIO6_IO21	Input	PU (100K)
RGMII_TD2	E21	NVCC_RGMII	DDR	ALT5	GPIO6_IO22	Input	PU (100K)
RGMII_TD3	A24	NVCC_RGMII	DDR	ALT5	GPIO6_IO23	Input	PU (100K)
RGMII_TX_CTL	C23	NVCC_RGMII	DDR	ALT5	GPIO6_IO26	Input	PD (100K)
RGMII_TXC	D21	NVCC_RGMII	DDR	ALT5	GPIO6_IO19	Input	PD (100K)
RTC_XTALI	D9	VDD_SNVS_CAP	—	—	RTC_XTALI	—	—
RTC_XTALO	C9	VDD_SNVS_CAP	—	—	RTC_XTALO	—	—
SATA_RXM	A14	SATA_VPH	—	—	SATA_PHY_RX_N	—	—
SATA_RXP	B14	SATA_VPH	—	—	SATA_PHY_RX_P	—	—
SATA_TXM	B12	SATA_VPH	—	—	SATA_PHY_TX_N	—	—
SATA_TXP	A12	SATA_VPH	—	—	SATA_PHY_TX_P	—	—
SD1_CLK	D20	NVCC_SD1	GPIO	ALT5	GPIO1_IO20	Input	PU (100K)
SD1_CMD	B21	NVCC_SD1	GPIO	ALT5	GPIO1_IO18	Input	PU (100K)
SD1_DAT0	A21	NVCC_SD1	GPIO	ALT5	GPIO1_IO16	Input	PU (100K)
SD1_DAT1	C20	NVCC_SD1	GPIO	ALT5	GPIO1_IO17	Input	PU (100K)
SD1_DAT2	E19	NVCC_SD1	GPIO	ALT5	GPIO1_IO19	Input	PU (100K)
SD1_DAT3	F18	NVCC_SD1	GPIO	ALT5	GPIO1_IO21	Input	PU (100K)
SD2_CLK	C21	NVCC_SD2	GPIO	ALT5	GPIO1_IO10	Input	PU (100K)
SD2_CMD	F19	NVCC_SD2	GPIO	ALT5	GPIO1_IO11	Input	PU (100K)

Table 98. 21 x 21 mm, 0.8 mm Pitch Ball Map (continued)

AB	AA	Y	W	V	U	T	R	
LVDS1_TX2_N	LVDS1_TX1_P	LVDS1_TX0_N	LVDS0_TX3_P	LVDS0_TX2_P	LVDS0_TX0_P	GPIO_2	GPIO_17	1
LVDS1_TX2_P	LVDS1_TX1_N	LVDS1_TX0_P	LVDS0_TX3_N	LVDS0_TX2_N	LVDS0_TX0_N	GPIO_9	GPIO_16	2
GND	LVDS1_TX3_N	LVDS1_CLK_N	GND	LVDS0_CLK_P	LVDS0_TX1_P	GPIO_6	GPIO_7	3
DRAM_D6	LVDS1_TX3_P	LVDS1_CLK_P	KEY_ROW2	LVDS0_CLK_N	LVDS0_TX1_N	GPIO_1	GPIO_5	4
DRAM_D12	DRAM_D3	GND	KEY_COL0	KEY_ROW4	KEY_COL3	GPIO_0	GPIO_8	5
DRAM_D14	DRAM_D10	DRAM_RESET	KEY_COL2	KEY_ROW0	KEY_ROW1	KEY_COL4	GPIO_4	6
DRAM_D16	GND	DRAM_D20	GND	NVCC_LVDS2P5	KEY_COL1	KEY_ROW3	GPIO_3	7
DRAM_DQM2	DRAM_D17	DRAM_D21	GND	GND	GND	GND	GND	8
DRAM_D18	DRAM_D23	DRAM_D19	GND	NVCC_DRAM	VDDARM23_IN	VDDARM23_IN	VDDARM23_IN	9
DRAM_SDQS3_B	GND	DRAM_D25	GND	NVCC_DRAM	VDDSOC_CAP	VDDSOC_CAP	VDDSOC_CAP	10
DRAM_D27	DRAM_SDCKE1	DRAM_SDCKE0	GND	NVCC_DRAM	GND	GND	VDDARM23_CAP	11
DRAM_SDBA2	DRAM_A14	DRAM_A15	GND	NVCC_DRAM	GND	GND	GND	12
DRAM_A8	GND	DRAM_A7	GND	NVCC_DRAM	VDDSOC_CAP	VDDSOC_CAP	VDDARM_CAP	13
DRAM_A1	DRAM_A2	DRAM_A3	DRAM_A4	NVCC_DRAM	VDDSOC_CAP	VDDSOC_CAP	VDDARM_IN	14
DRAM_RAS	DRAM_A10	DRAM_SDBA1	GND	NVCC_DRAM	GND	GND	GND	15
DRAM_SDWE	GND	DRAM_CS0	GND	NVCC_DRAM	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	16
DRAM_SDODT1	DRAM_D32	DRAM_D36	GND	NVCC_DRAM	GND	GND	GND	17
DRAM_DQM4	DRAM_D33	DRAM_D37	GND	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	18
DRAM_D38	GND	DRAM_D40	GND	GND	GND	GND	NVCC_ENET	19
DRAM_D41	DRAM_D45	DRAM_D44	ENET_TXD1	ENET_MDC	ENET_TXD0	DISP0_DAT21	DISP0_DAT13	20
DRAM_D42	DRAM_D57	DRAM_DQM7	ENET_RXD0	ENET_TX_EN	ENET_CRS_DV	DISP0_DAT16	DISP0_DAT10	21
DRAM_D52	GND	DRAM_D59	ENET_RXD1	ENET_REF_CLK	DISP0_DAT20	DISP0_DAT15	DISP0_DAT8	22
DRAM_D60	DRAM_D61	DRAM_D62	ENET_RX_ER	ENET_MDIO	DISP0_DAT19	DISP0_DAT11	DISP0_DAT6	23
GND	DRAM_SDQS7_B	GND	DISP0_DAT23	DISP0_DAT22	DISP0_DAT17	DISP0_DAT12	DISP0_DAT7	24
DRAM_D56	DRAM_SDQS7	DRAM_D58	DRAM_D63	DISP0_DAT18	DISP0_DAT14	DISP0_DAT9	DISP0_DAT5	25

7 Revision History

Table 99 provides a revision history for the i.MX 6Dual/6Quad data sheet.

Table 99. i.MX 6Dual/6Quad Data Sheet Document Revision History

Rev. Number	Date	Substantive Change(s)
5	09/2017	Rev. 5 changes include the following: • Changed throughout: – Changed terminology from “floating” to “not connected”. – Removed VADC feature from 19mm x 19mm package. Contact NXP sales and marketing with enablement options. • Section 1, “Introduction” on page 1: Corrected typo in last sentence of first paragraph “aut1omotive”. • Section 1.2, “Features” on page 5: Changed Internal/external peripheral item from “LVDS serial ports—One port up to 165 MPixels/sec…” to: “…—One port up to 170 MPixels/sec…”. • Table 1, “Example Orderable Part Numbers”: Added part numbers for silicon revision 1.4 with suffix “E”. • Section 1.3, “Signal Naming Convention” on page 8” and Section 6.1, “Signal Naming Convention”: changed wording from *updated* or *changed signal naming,* to *standard signal naming*. • Table 2, “i.MX 6Dual/6Quad Modules List,” on page 11: – Added bullet to uSDHC row: “Conforms to the SD Host Controller Standard Specification v3.0” • Section 4, “Electrical Characteristics” on page 20: Changed several references from JESD and JEDEC standards to cross references to the Section 4.10, “Multi-Mode DDR Controller (MMDC). • Table 4, “Absolute Maximum Ratings,” on page 21: Multiple changes: – Core supply voltages: Separated rows by LDO enabled and LDO bypass. For LDO enabled, changed maximum value from 1.5 to 1.6V. – Renamed Internal supply voltages to Core supply output voltage (LDO enabled) and changed maximum value from 1.3 to 1.4V. Added symbol NVCC_PLL_OUT. – Reordered VDD_HIGH_IN row and changed maximum value from 3.6 to 3.7V. – DDR I/O supply voltage row changes: — Changed Symbols from “Supplies denoted as I/O supply” to: “NVCC_DRAM” — Added footnote. – GPIO I/O supply voltage: Added symbols. Changed maximum value from 3.6 to 3.7V. – Resequenced: HDMI, PCIe, and SATA PHY high (VPH) supply voltage to precede low (VP) – Added row: RGMII I/O supply voltage – Added row, V_{in}/V_{out} input/output voltage range (non-DDR pins) distinguishing between DDR pins. – Changed maximum value for V_{in}/V_{out} input/output voltage range DDR pins to OVDD+0.4. – Added footnotes to both maximum values of V_{in}/V_{out} input/output voltage range. – Added row: USB_OTG_CHD_B • Section 4.1.2, “Thermal Resistance” on page 22: Added NOTE: “Per JEDEC JESD51-2, the intent of thermal resistance measurements…”. • Section 4.1.5, “Maximum Measured Supply Currents” on page 26: Clarified language throughout this section regarding the use case to estimate the maximum supply current. • Section 4.2.1, “Power-Up Sequence” on page 33: – Removed content about calculating the proper current limiting resistor for a coin cell. – Removed inference to internal POR. • Section 4.5.2, “OSC32K” on page 37: Removed content about calculating the proper current limiting resistor for a coin cell. • Section 4.6.1, “XTALI and RTC_XTALI (Clock Inputs) DC Parameters” on page 39: – Added “NOTE: The Vil and Vih specifications only apply when an external clock source is used…”. *(Revision History table continues on next page.)*

Table 99. i.MX 6Dual/6Quad Data Sheet Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
5 (*Cont.*)	09/2017	• Table 21, "XTALI and RTC_XTALI DC Parameters," on page 39: – Added footnote to RTC_XTALI high level DC input voltage row: "This voltage specification must not be exceeded and …". Section 4.6.4, "RGMII I/O 2.5V I/O DC Electrical Parameters" on page 40: Added section and table. • Section 4.10, "Multi-Mode DDR Controller (MMDC)" on page 64: Replaced section with new content. Was: 4.9.4 "*DDR SDRAM Specific Parameters (DDR3/DDR3L/LPDDR2)*" with timing diagrams and parameter tables for DDR3/DDR3L/LPDDR2. • Table 51, "eMMC4.4/4.41 Interface Timing Specification," on page 81, – Corrected SD3, uSDHC Input Setup Time, minimum value from 2.6ns to 1.7ns. – Added footnote to Card Input Clock regarding duty cycle range. • Table 52, "SDR50/SDR104 Interface Timing Specification," on page 82: Changes to Min/Max values: – SD2 min from: 0.3 x tCLK; to: 0.46 x tCLK – SD2 max from: 0.7 x tCLK to: 0.54 x tCLK – SD3 min from: 0.3 x tCLK; to: 0.46 x tCLK. Also corrected ID from duplicate SD2 to SD3. – SD3 max from: 0.7 x tCLK; to: 0.54 x tCLK – SD5 max from: 1 ns; to: 0.74 ns • Table 62, "Camera Input Signal Cross Reference, Format, and Bits Per Cycle," on page 95: Changed RGB565, 16 bits column heading from 2 cycles to 1 cycle. • Table 63, "Sensor Interface Timing Characteristics," on page 98, Sensor Interface Timing characteristics: Added rows to include Vsync values. • Table 95, "21 x 21 mm Supplies Contact Assignment," on page 144: Added description to ZQPAD. • Table 96, "21 x 21 mm Functional Contact Assignments," on page 146: – Changed rows DRAM_SDCLK_0 and DRAM_SDCLK_1, Out of Reset Conditions from *"Input–Hi-Z"* to *"Output*–0". – Added description to GPANAIO row: "…output for NXP use only…" *(Revision History table continues on next page.)*

Table 99. i.MX 6Dual/6Quad Data Sheet Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
Rev. 3	02/2014	• Updates throughout for Silicon revision D, include: - Figure 1 Part number nomenclature diagram. - Example Orderable Part Number tables, Table 1 • Feature description for Miscellaneous IPs and interfaces; SSI and ESAI. • Table 6, UART 1–5 description change: programmable baud rate up to 5 MHz. • Table 6, uSDHC 1–4 description change: including SDXC cards up to 2 TB. • Table 6, operating range for Run mode: LDO bypassed, minimum value corrected to 1.150 V. • Table 6, table footnotes, added LDO enabled mode footnote for internal LDO output set points. • Table 61, added table footnote to the Comment heading in the Comment column. • Removed table “On-Chip LDOs and their On-Chip Loads.” • Section 4.1.4, External Clock Sources; added Note, “The internal RTC oscillator does not …”. • Section 4.1.5, reworded second paragraph about the power management IC to explain that a robust thermal design is required for the increased system power dissipation. • Table 8, Maximum Supply Currents: NVCC_RGMII Condition value changed to N=6. • Table 8, Maximum Supply currents: Added row; NVCC_LVDS2P5 • Section 4.2.1 Power-Up Sequence: reworded third bulleted item regarding POR control. • Section 4.2.1 Power-Up Sequence: removed Note. • Section 4.5.2 OSC32K, second paragraph reworded to describe OSC32K automatic switching. • Section 4.5.2 OSC32K, added Note following second paragraph to caution use of internal oscillator use. • Table 21 XTALI and RTC_XTALI DC parameters; changed RTC_XTALI Vih minimum value to 0.8. • Table 21 XTALI and RTC_XTALI DC parameters; changed RTC_XTALI Vih maximum value to 1.1. • Table 38 Reset Timing Parameters; removed footnote. • Section 4.9.3 External Interface Module; enhanced wording to first paragraph to describe operating frequency for data transfers, and to explain register settings are valid for entire range of frequencies. • Table 41. EIM Bus Timing Parameters; reworded footnotes for clarity. • Table 42. EIM Asynchronous Timing Parameters; removed comment from the Max heading cell. • Table 42. EIM Asynchronous Timing Parameters; reworded footnote 2 for clarity. • Table 57. RMII Signal Timing; parameter M19 Max value relaxed to 13.5 ns. • Table 73. MLB 256/512 Fs Timing Parameters; added last row for MLBSIG (MLBDAT). • Table 74. MLB 1024 Fs Timing Parameters; added last row for MLBSIG (MLBDAT). • Table 95. Corrected the ALT5 Default Function names. • Figure 100 and Figure 101 21 x 21 mm Lidded Package; updated drawing (Rev D).
Rev. 2.3	07/26 /2013	• Table 96, *21 x 21Functional Contact Assignments*: Restored NANDF_WP_B row and description. • System Timing Parameters Table 38, *Reset timing parameter*, CC1 description clarified, change from: “Duration of SRC_POR_B to be qualified as valid (input slope <= 5 ns)” to: “Duration of SRC_POR_B to be qualified as valid” and added a footnote to the parameter with the following text: “SRC_POR_B rise and fall times must be 5 ns or less.” This change was made for clarity and does not represent a specification change.
Rev. 2.2	07/2013	• Editor corrections to revision history links. No technical content changes.
Rev. 2.1	07/2013	• Figure 1, Changed temperature references from Consumer to Commercial. • Table 96, *21 x 21Functional Contact Assignments*: —Removed rows: DRAM_VREF, HDMI_DDCCEC, and HDMI_REF. —Due to a typographical error in revision 2.0, the ball names for rows EIM_DA2 through EIM_DA15 were ordered incorrectly. This has been corrected in revision 2.1. The ball map is correct in both revision 2.0 and 2.1. *(Revision History table continues on next page.)*

Table 99. i.MX 6Dual/6Quad Data Sheet Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
Rev. 2	04/2013	Substantive changes throughout this document are as follows: • Incorporated standardized signal names. This change is extensive throughout. Added reference to EB792, i.MX Signal Name Mapping. • Figures updated to align to standardized signal names. • Aligned references to FCBGA to read FC**P**BGA throughout document. • Updated references to eMMC standard to include 4.41. • Table 2, "i.MX 6Dual/6Quad Modules List," Changed reference to Global Power Controller to read General Power Controller. • Table 4, "Absolute Maximum Ratings," Added VDD_ARM23_IN to Core supply voltages. • Table 6 "Operating Ranges": Run Mode - LDO Enabled, VDD_ARM_IN/VDD_ARM23_IN, 792 MHz, input voltage minimum changed to 1.275V and VDD_ARM CAP minimum changed to 1.150V. NVCC_NAND, changed to NVCC_NANDF. • Table 6 "Operating Ranges": Added reference for information on product lifetime: *i.MX 6Dual/6Quad Product Usage Lifetime Estimates Application Note*, AN4724. • Table 9. "Maximum Supply Currents": Added current for i.MX6Dual • Table 10 "Stop Mode Current and Power Consumption": Added SNVS Only mode. • Table 22 "GPIO I/O DC Parameters": Removed parameters Iskod and Isspp. • Table 48, "ECSPI Master Mode Timing Parameters," Updated parameter CS6 ECSPIx_SSx Lag Time (CS hold time) Min from Half SCLK period to Half SCLK period-2. • Table 77 "SD/eMMC4.3 Interface Timing Specification," eMMC parameter SD8 value Min updated from 5.6 ns to 1.5 ns. • Table 89 RGMII Signal Switching Specifications RGMII parameter TskewR units corrected. • Table 134 "21 x 21 mm Functional Contact Assignments," Updated GPIO_1 Ball Name value to PU (100K). • Table 134 "21 x 21 mm Functional Contact Assignments," Clarification of ENET_REF_CLK naming. • Removed section, EIM Signal Cross Reference. Signal names are now aligned with reference manual. • Section 1.2, "Features added bulleted item regarding the SOC-level memory system. • Section 4.2.1, "Power-Up Sequence" updated wording. • Section 4.3.2, "Regulators for Analog Modules": Added NVCC_PLL_OUT to section heading. • Section 4.6.1, "XTALI and RTC_XTALI (Clock Inputs) DC Parameters": Added section. • Section 4.10, "General-Purpose Media Interface (GPMI) Timing" figures replaced, tables revised.