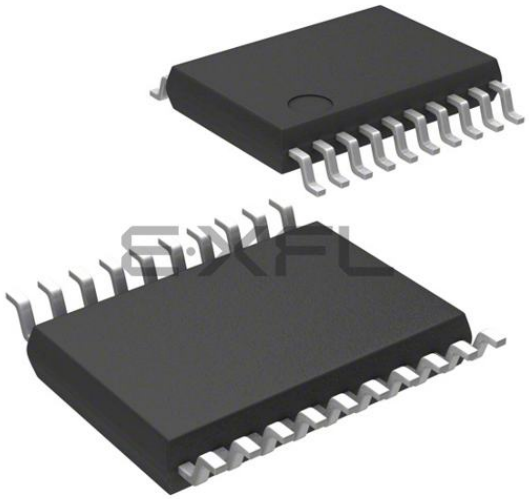


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8A
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, ProxSense, PWM, WDT
Number of I/O	12
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8tl52f4p6tr

List of tables

1 Introduction

This datasheet provides the STM8TL52G4, STM8TL52F4, STM8TL53C4, STM8TL53G4 and STM8TL53F4 pinouts, ordering information, mechanical and electrical device characteristics.

For complete information on the microcontroller memory, registers and peripherals, please refer to the STM8TL5xxx reference manual (RM0312) and to the STM8TL5xxx Flash programming manual (PM0212) for Flash memory related information. For information on the debug module and SWIM (single wire interface module), refer to the STM8 SWIM communication protocol and debug module user manual (UM0470). For information on the STM8 core, refer to the STM8 CPU programming manual (PM0044).

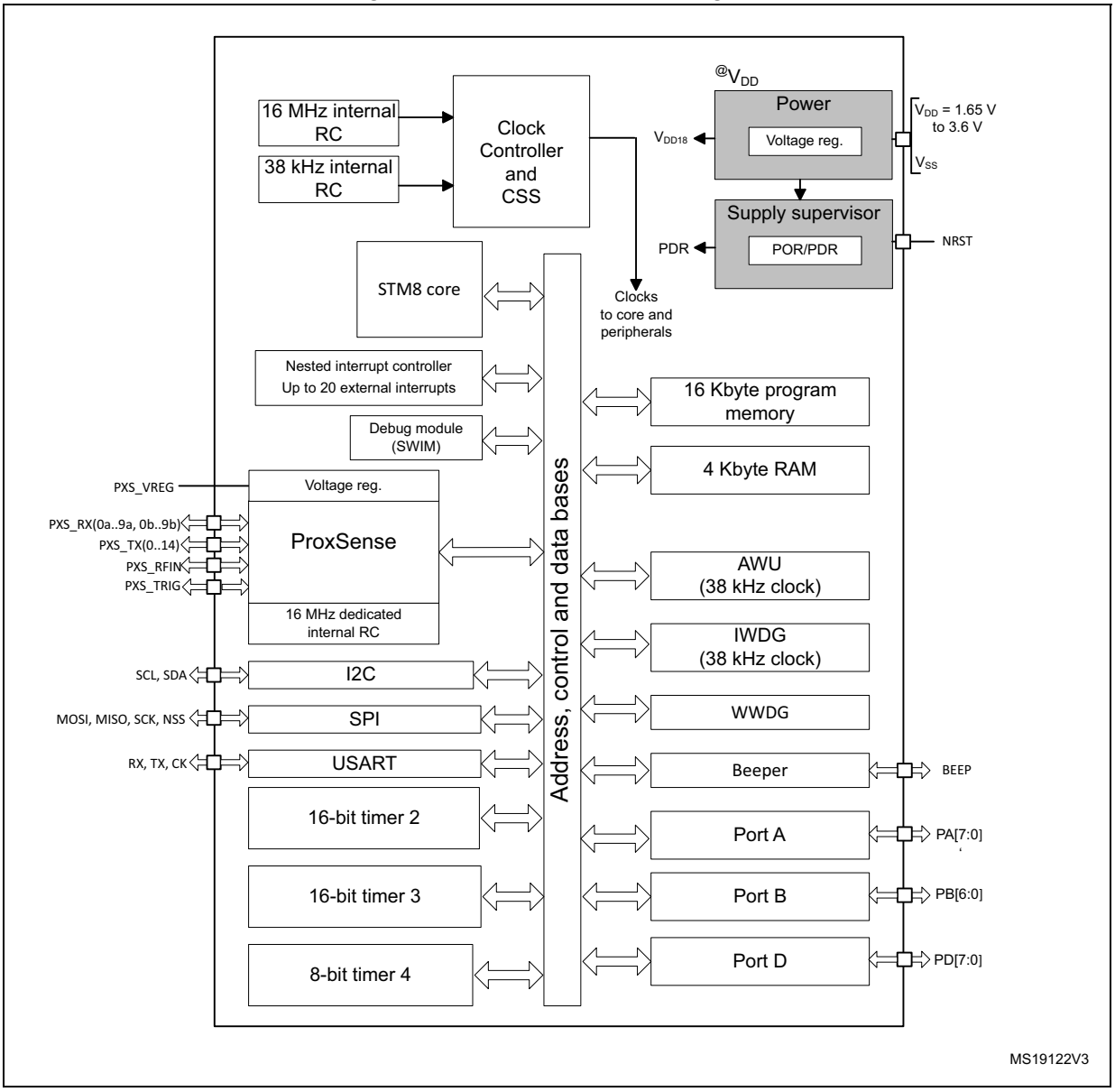
All devices of the STM8TL5xxx product line provide the following benefits:

- Advanced capacitive sensing
  - Patented ProxSense ™ acquisition peripheral, providing high-end acquisition, filtering and environment adaptation
  - Outstanding signal-to-noise ratio for touch and proximity sensing
  - Up to 300 projected capacitive channels
- Reduced system cost
  - Up to 16 Kbyte of low-density embedded Flash program memory including up to 2 Kbyte of data EEPROM
  - High system integration level with internal clock oscillators and watchdogs
  - Smaller battery and cheaper power supplies
- Low power consumption and advanced features
  - Up to 16 MIPS at 16 MHz CPU clock frequency
  - Less than 150 µA/MHz, 0.8 µA in Active-halt mode with AWU, and 0.3 µA in Halt mode
  - Clock gated system and optimized power management
- Short development cycles
  - Application scalability across a common family product architecture with compatible pinout, memory map and modular peripherals
  - Full documentation and a wide choice of development tools
- Product longevity
  - Advanced core and peripherals made in a state-of-the-art technology
  - Product family operating from 1.65 V to 3.6 V supply

Note: ProxSense ™ is a trademark of Azoteq (Pty) Ltd.

3 Product overview

Figure 1. STM8TL5xx4 block diagram



Legend:

AWU: Auto-wakeup unit
Int. RC: internal RC oscillator
I²C: Inter-integrated circuit multimaster interface
POR/PDR: Power on reset / power down reset
SPI: Serial peripheral interface
SWIM: Single wire interface module
USART: Universal synchronous / asynchronous receiver / transmitter
IWDG: Independent watchdog
WWDG: Window watchdog
ProxSense™: capacitive sensing peripheral

3.9 System configuration controller

The system configuration controller provides the capability to remap some alternate functions on different I/O ports. TIM3 channels can be remapped.

3.10 Independent watchdog

The independent watchdog (IWDG) peripheral can be used to resolve processor malfunctions due to hardware or software failures.

It is clocked by the 38 kHz LSI internal RC clock source, and thus stays active even in case of a CPU clock failure.

3.11 Window watchdog

The window watchdog (WWDG) is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.12 Auto-wakeup counter

The auto-wakeup (AWU) counter is used to wakeup the device from Active-halt mode.

3.13 General purpose and basic timers

STM8TL5xx4 devices contain two 16-bit general purpose timers (TIM2 and TIM3) and one 8-bit basic timer (TIM4).

16-bit general purpose timers

The 16-bit timers consist of 16-bit up/down auto-reload counters driven by a programmable prescaler. They perform a wide range of functions, including:

- Timebase generation
- Measuring the pulse lengths of input signals (input capture)
- Generating output waveforms (output compare, PWM and One pulse mode)
- Interrupt capability on various events (capture, compare, overflow, break, trigger)
- Synchronization with other timers or external signals (external clock, reset, trigger and enable)

8-bit basic timer

The 8-bit timer consists of an 8-bit up auto-reload counter driven by a programmable prescaler. It can be used for timebase generation with interrupt generation on timer overflow.

3.14 Beeper

STM8TL5xx4 devices include a beeper function used to generate a beep signal in the range of 1, 2 or 4 kHz when the LSI clock is operating at a frequency of 38 kHz.

3.15 USART

The USART interface (USART) allows full duplex, asynchronous communications with external devices requiring an industry standard NRZ asynchronous serial data format. It offers a very wide range of baud rates.

- 1 Mbit/s full duplex SCI
- SPI emulation
- High precision baud rate generator
- Single wire half duplex mode

3.16 SPI

The serial peripheral interface (SPI) provides half/ full duplex synchronous serial communication with external devices.

- Maximum speed: 8 Mbit/s ($f_{SYSCLK/2)}$ both for master and slave
- Full duplex synchronous transfers
- Simplex synchronous transfers on 2 lines with a possible bidirectional data line
- Master or slave operation - selectable by hardware or software
- Hardware CRC calculation
- Slave/master selection input pin

3.17 I^2C

The I^2C bus interface (I^2C) provides multi-master capability, and controls all I^2C bus-specific sequencing, protocol, arbitration and timing.

- Master, slave and multi-master capability
- Dual addressing mode capability
- Standard mode up to 100 kHz and fast speed modes up to 400 kHz
- 7-bit and 10-bit addressing modes
- Hardware CRC calculation

3.18 ProxSense

The ProxSense peripheral uses a charge-transfer method to detect capacitance changes.

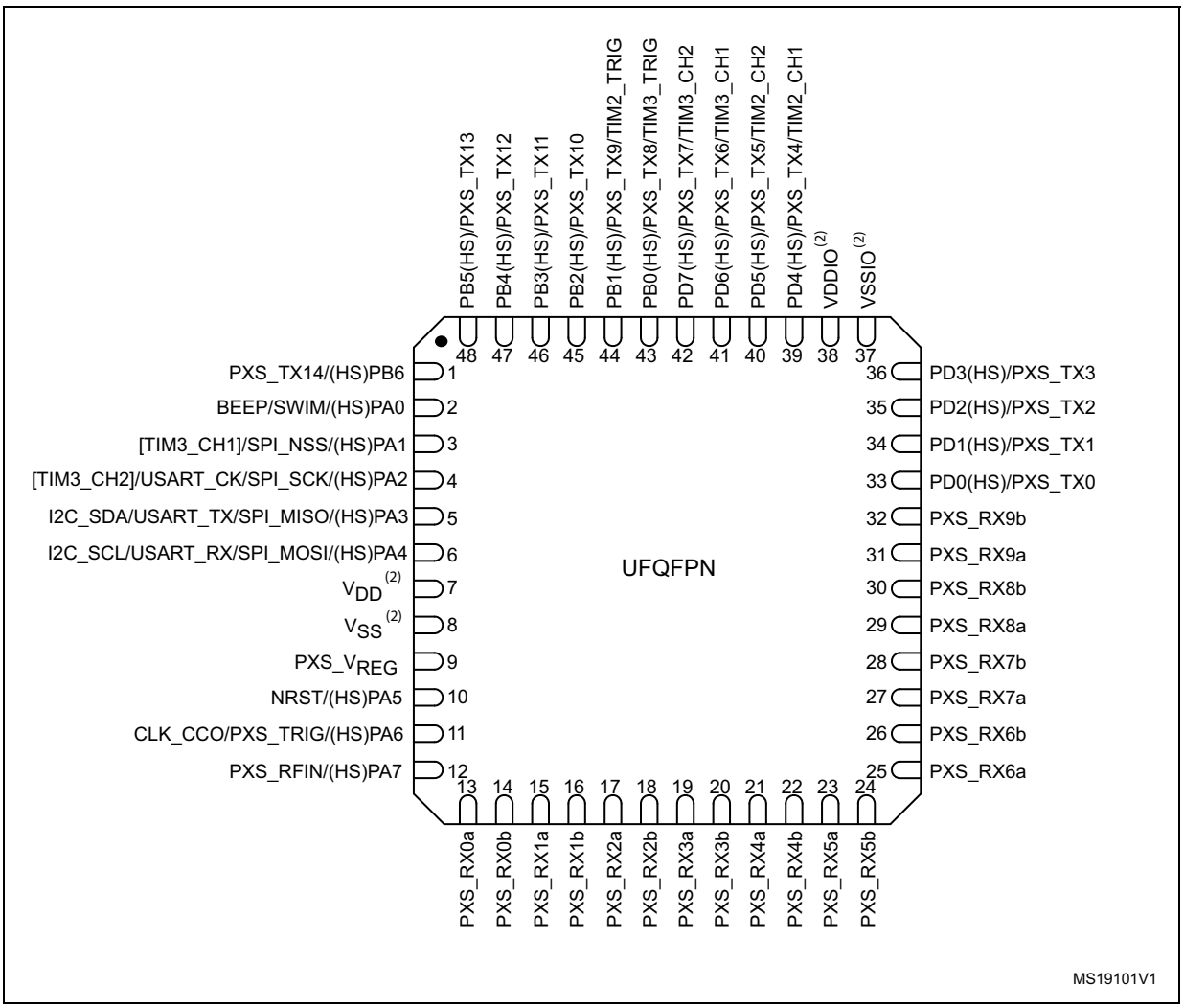
- Up to 300 capacitive sensing channels composed of 15 transmitters and 20 receivers with up to 10 Rx channels acquired in parallel
- Fast acquisition with a typical scan time of 250 µs for 10 Rx channels
- Configurable internal sampling capacitor (C_S)
- Electrode Parasitic Capacitance Compensation (EPCC) to ensure the best sensitivity in all user environments
- RF noise detection, allowing to reject corrupted samples
- External trigger to de-synchronize the acquisition from known noise
- Can be configured to return to low power mode between each conversion
- Acquisition possible in Run, Wait and Active-halt modes

3.19 TouchSensing dedicated library available upon request

- Complete C source code library with firmware examples (MISRA compliant)
- Multifunction capability to combine capacitive sensing functions with traditional MCU features
- Compatible with proximity, touchkey, linear and rotary touch sensor implementation
- Configuration of all ProxSense parameters
- Extra filtering and calibration functions
- TouchSensing user interface through firmware API for status reporting and application configuration
- Compliance with Cosmic, IAR and Raisonance C compilers

4 Pin description

Figure 2. STM8TL53 48-pin UFQFPN package pinout



1. HS corresponds to 20 mA high sink/source capability.
2. Power supply pins must be correctly decoupled with capacitors near the pins. Please refer to the power supply circuitry details in *Section 9.3.2: Power supply on page 46* and the STM8TL5xxx reference manual (RM0312), Section 6: Power supply.

Table 4. STM8TL5xx4 pin description (continued)

Pin no.			Pin name	Type	Input				Output			Main function (after reset)	Alternate function	
UFQFPN48	UFQFPN28	TSSOP20			Level	floating	wpu	Ext. interrupt	High sink/source	OD	PP		Default	Remap
8	5	8	VSS	S	-	-	-	-	-	-	-	Digital ground	-	-
9	6	9	PXS_VREG	S	-	-	-	-	-	-	-	-	ProxSense voltage regulator External decoupling capacitor	-
10	7	10	PA5/NRST(3)	I/O	TC	-	-	-	HS	X	X	Reset	Port A5 (output only)	-
11	8	-	PA6/ PXS_TRIG/ CLK_CCO	I/O	FT	X	X	X	HS	X	X	Port A6	ProxSense external trigger input	-
		-											CLK clock output	-
12	9	-	PA7/PXS_RFIN	I/O	TC	X	X	X	HS	X	X	Port A7	ProxSense antenna input	-
13	10	11	PXS_RX0a	-	-	-	-	-	-	-	-	PXS_RX0a	ProxSense receiver 0a	-
14	-	-	PXS_RX0b	-	-	-	-	-	-	-	-	PXS_RX0b	ProxSense receiver 0b	-
15	11	12	PXS_RX1a	-	-	-	-	-	-	-	-	PXS_RX1a	ProxSense receiver 1a	-
16	-	-	PXS_RX1b	-	-	-	-	-	-	-	-	PXS_RX1b	ProxSense receiver 1b	-
17	12	13	PXS_RX2a	-	-	-	-	-	-	-	-	PXS_RX2a	ProxSense receiver 2a	-
18	-	-	PXS_RX2b	-	-	-	-	-	-	-	-	PXS_RX	ProxSense receiver 2b	-
19	13	-	PXS_RX3a	-	-	-	-	-	-	-	-	PXS_RX3a	ProxSense receiver 3a	-
20	-	-	PXS_RX3b	-	-	-	-	-	-	-	-	PXS_RX3b	ProxSense receiver 3b	-
21	14	-	PXS_RX4a	-	-	-	-	-	-	-	-	PXS_RX4a	ProxSense receiver 4a	-
22	-	-	PXS_RX4b	-	-	-	-	-	-	-	-	PXS_RX4b	ProxSense receiver 4b	-

Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5210	I2C	I2C_CR1	I2C control register 1	0x00
0x00 5211		I2C_CR2	I2C control register 2	0x00
0x00 5212		I2C_FREQR	I2C frequency register	0x00
0x00 5213		I2C_OAR1L	I2C own address register 1 low	0x00
0x00 5214		I2C_OAR1H	I2C own address register 1 high	0x00
0x00 5215		I2C_OAR2	I2C own address register 2	0x00
0x00 5216		I2C_DR	I2C data register	0x00
0x00 5217		I2C_SR1	I2C status register 1	0x00
0x00 5218		I2C_SR2	I2C status register 2	0x00
0x00 5219		I2C_SR3	I2C status register 3	0x00
0x00 521A		I2C_ITR	I2C interrupt control register	0x00
0x00 521B		I2C_CCRL	I2C Clock control register low	0x00
0x00 521C		I2C_CCRH	I2C Clock control register high	0x00
0x00 521D		I2C_TRISER	I2C TRISE register	0x00
0x00 521E to 0x00 522F	Reserved area (18 byte)			
0x00 5230	USART	USART_SR	USART status register	0xC0
0x00 5231		USART_DR	USART data register	0xXX
0x00 5232		USART_BRR1	USART baud rate register 1	0x00
0x00 5233		USART_BRR2	USART baud rate register 2	0x00
0x00 5234		USART_CR1	USART control register 1	0x00
0x00 5235		USART_CR2	USART control register 2	0x00
0x00 5236		USART_CR3	USART control register 3	0x00
0x00 5237		USART_CR4	USART control register 4	0x00
0x00 5238 to 0x00 524F	Reserved area (18 byte)			

Table 8. CPU/SWIM/debug module/interrupt controller registers (continued)

Address	Block	Register label	Register name	Reset status
0x00 7F0B to 0x00 7F5F	Reserved area (85 byte)			
0x00 7F60	CFG	CFG_GCR	Global configuration register	0x00
0x00 7F61 0x00 7F6F	Reserved area (15 byte)			
0x00 7F70	ITC-SPR (1)	ITC_SPR1	Interrupt Software priority register 1	0xFF
0x00 7F71		ITC_SPR2	Interrupt Software priority register 2	0xFF
0x00 7F72		ITC_SPR3	Interrupt Software priority register 3	0xFF
0x00 7F73		ITC_SPR4	Interrupt Software priority register 4	0xFF
0x00 7F74		ITC_SPR5	Interrupt Software priority register 5	0xFF
0x00 7F75		ITC_SPR6	Interrupt Software priority register 6	0xFF
0x00 7F76		ITC_SPR7	Interrupt Software priority register 7	0xFF
0x00 7F77		ITC_SPR8	Interrupt Software priority register 8	0xFF
0x00 7F78 to 0x00 7F79	Reserved area (2 byte)			
0x00 7F80	SWIM	SWIM_CSR	SWIM control status register	0x00
0x00 7F81 to 0x00 7F8F	Reserved area (15 byte)			
0x00 7F90	DM	DM_BK1RE	Breakpoint 1 register extended byte	0xFF
0x00 7F91		DM_BK1RH	Breakpoint 1 register high byte	0xFF
0x00 7F92		DM_BK1RL	Breakpoint 1 register low byte	0xFF
0x00 7F93		DM_BK2RE	Breakpoint 2 register extended byte	0xFF
0x00 7F94		DM_BK2RH	Breakpoint 2 register high byte	0xFF
0x00 7F95		DM_BK2RL	Breakpoint 2 register low byte	0xFF
0x00 7F96		DM_CR1	Debug module control register 1	0x00
0x00 7F97		DM_CR2	Debug module control register 2	0x00
0x00 7F98		DM_CSR1	Debug module control/status register 1	0x10
0x00 7F99		DM_CSR2	Debug module control/status register 2	0x00
0x00 7F9A		DM_ENFCTR	Enable function register	0xFF

1. Refer to *Table 7: General hardware register map on page 28* (addresses 0x00 50A0 to 0x00 50A5) for a list of external interrupt registers.

Table 9. Interrupt mapping (continued)

IRQ No.	Source block	Description	Wakeup from Halt mode	Wakeup from Active-halt mode	Wakeup from Wait (WFI mode)	Wakeup from Wait (WFE mode)(1)	Vector address
22	TIM3	TIM3 capture/compare interrupt	-	-	Yes	Yes	0x00 8060
23-24	Reserved						0x00 8064-0x00 806B
25	TIM4	TIM4 update/overflow/ trigger interrupt	-	-	Yes	Yes	0x00 806C
26	SPI	SPI TX buffer empty/ RX buffer not empty/ error/wakeup interrupt	Yes	Yes	Yes	Yes	0x00 8070
27	USART	USART transmit data register empty/ transmission complete interrupt	-	-	Yes	Yes	0x00 8074
28	USART	USART received data ready/overrun error/ idle line detected/parity error/global error interrupt	-	-	Yes	Yes	0x00 8078
29	I2C	I2C interrupt(3)	Yes	Yes	Yes	Yes	0x00 807C

1. The Low power wait mode is entered when executing a WFE instruction in Low power run mode. In WFE mode, the interrupt is served if it has been previously enabled. After processing the interrupt, the processor goes back to WFE mode. When the interrupt is configured as a wakeup event, the CPU wakes up and resumes processing.
2. ProxSense activated before executing HALT instruction.
3. The device is woken up from Halt or Active-halt mode only when the address received matches the interface address.

Table 14. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD} power line (source)	80	mA
I_{VSS}	Total current out of V_{SS} ground line (sink)	80	
I_{IO}	Output current sunk by any other I/O and control pin	25	
	Output current source by any I/Os and control pin	–25	
$I_{INJ(PIN)}$(1)	Injected current on PA pins(2)	±5	
$I_{INJ(PIN)}$	Injected current on PB pins	0	
$I_{INJ(PIN)}$	Injected current on PD pins	0	
$\Sigma I_{INJ(PIN)}$(1)	Total injected current (sum of all I/O and control pins)(2)	±25	

1. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected.
2. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

Table 15. Thermal characteristics

Symbol	Ratings	Min	Unit
T_{STG}	Storage temperature range	–65 to +150	° C
T_J	Maximum junction temperature	150	

9.3 Operating conditions

Subject to general operating conditions for V_{DD} and T_A.

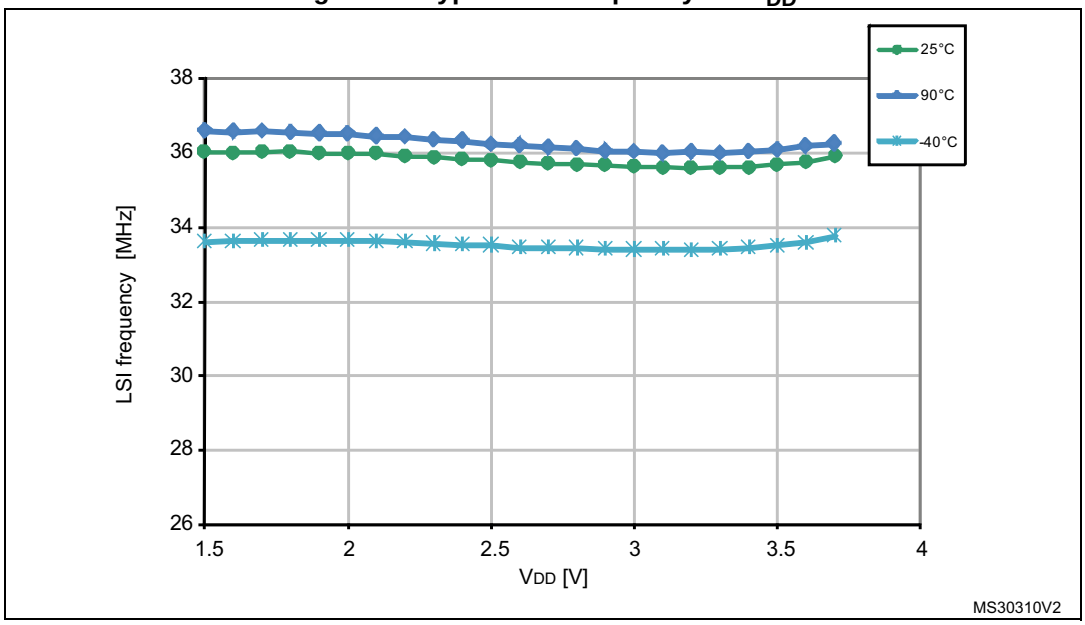
9.3.1 General operating conditions

Table 16. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MASTER}(1)	Master clock frequency	1.65 V ≤ V_{DD} < 3.6 V	2	16	MHz
V_{DD}	Standard operating voltage	-	1.65	3.6	V
P_D(2)	Power dissipation at T_A= 85 °C for suffix 2 devices	UQFPN48	-	625	mW
		UQFPN28	-	250	
		TSSOP20		180	
T_A	Temperature range	1.65 V ≤ V_{DD} < 3.6 V	–40	85	°C
T_J	Junction temperature range	–40 °C ≤ T_A ≤ 85 °C	–40	105	

1. f_{MASTER} = f_{CPU}.
2. To calculate $P_{Dmax}(T_A)$ use the formula given in thermal characteristics $P_{Dmax}=(T_{Jmax} - T_A)/\Theta_{JA}$ with T_{Jmax} in this table and Θ_{JA} in table “Thermal characteristics”.

Figure 16. Typical LSI frequency vs. V_{DD}



9.3.7 Memory characteristics

T_A = –40 to 85°C unless otherwise specified.

RAM characteristics

Table 27. RAM and hardware registers

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{RM}	Data retention mode (1)	Halt mode (or Reset)	1.4	-	-	V

1. Minimum supply voltage without losing data stored in RAM (in Halt mode or under Reset) or in hardware registers (only in Halt mode). Guaranteed by characterization, not tested in production.

Flash memory characteristics

Table 28. Flash program memory

Symbol	Parameter	Conditions	Min.	Typ.	Max.(1)	Unit
V_{DD}	Operating voltage (all modes, read/write/erase)	f_{MASTER} = 16 MHz	1.65	-	3.6	V
t_{prog}	Programming time for 1 or 64 byte (block) erase/write cycles (on programmed byte)		-	6	-	ms
	Programming time for 1 to 64 byte (block) write cycles (on erased byte)		-	3	-	ms
I_{prog}	Programming/ erasing consumption	T_A=+25 °C, V_{DD} = 3.0 V	-	0.7	-	mA
		T_A=+25 °C, V_{DD} = 1.8 V	-		-	

1. Data based on characterization results, not tested in production.

Figure 18. Typical V_{IL} and V_{IH} vs V_{DD}

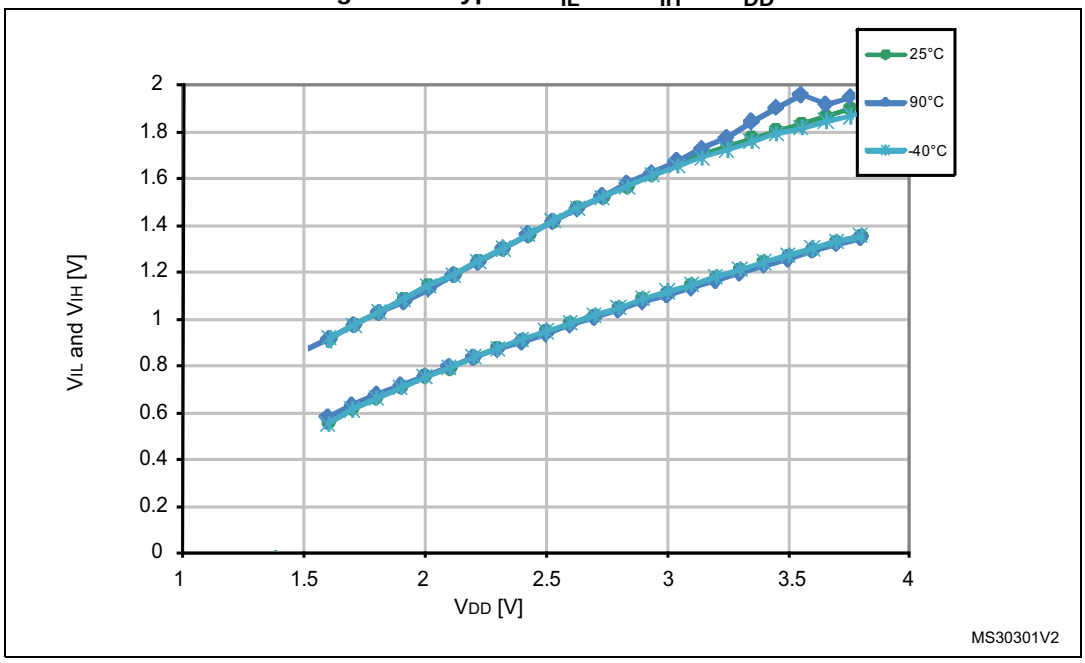


Figure 20. Typ. V_{OL} at V_{DD} = 3.0 V (standard ports)

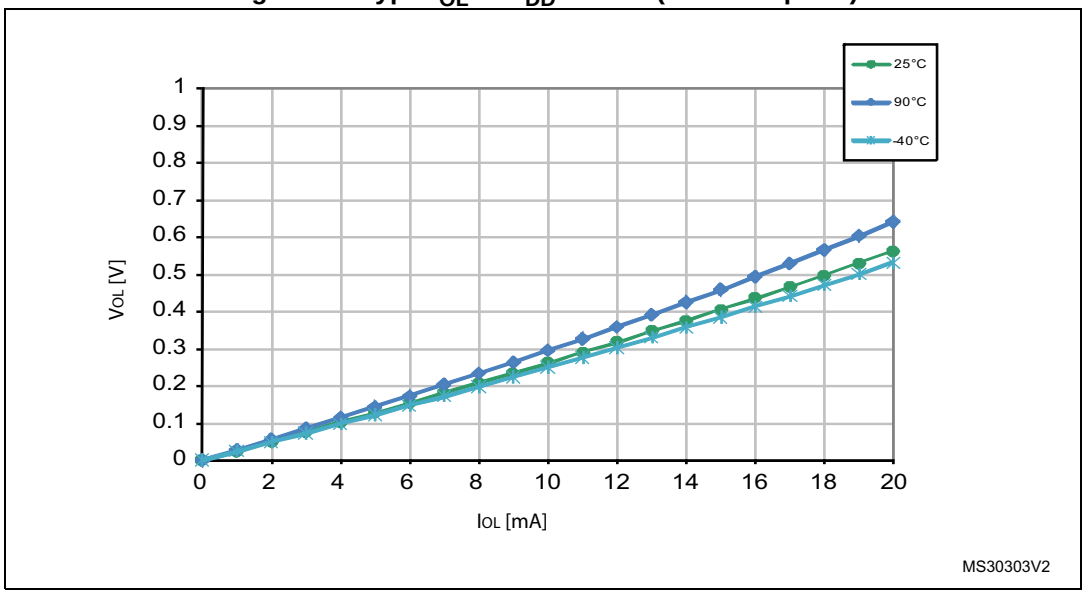


Figure 21. Typ. V_{DD} - V_{OH} at V_{DD} = 1.8 V (standard ports)

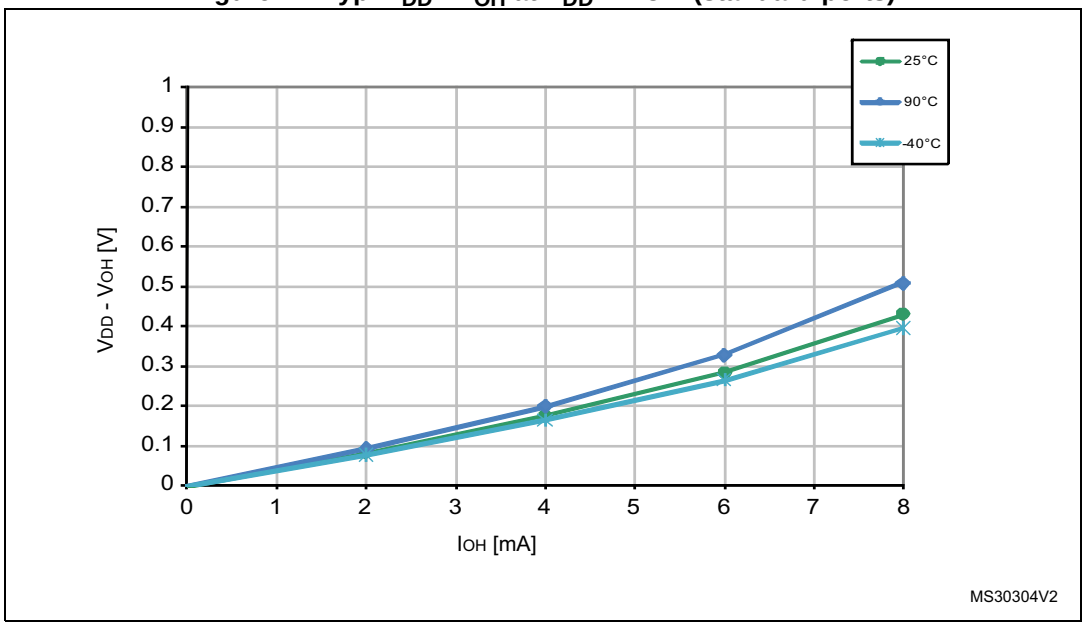
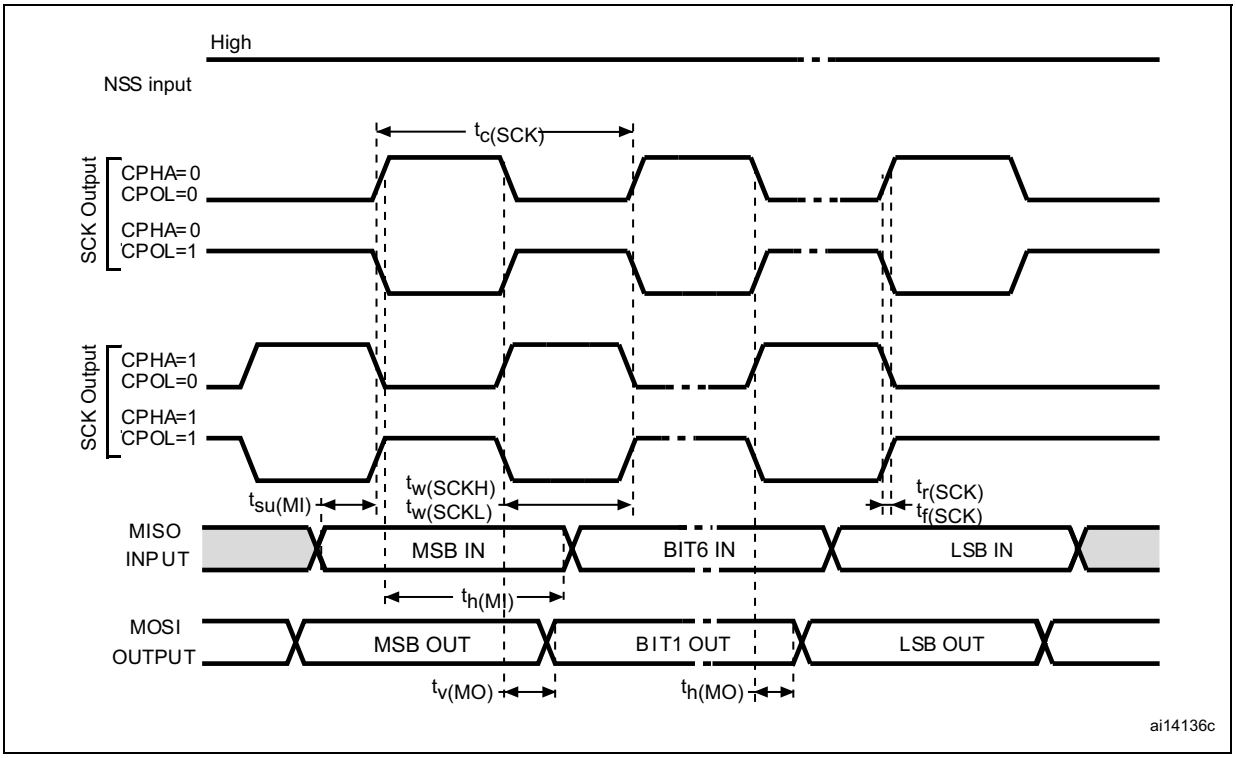


Figure 29. SPI timing diagram - master mode(1)



1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Table 36. EMS data

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	UFQFPN48, V_{DD} = 3.3 V	3B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	UFQFPN48, V_{DD} = 3.3 V, f_{HSI}	3B

Electromagnetic interference (EMI)

Based on a simple application running on the product (toggling 2 LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm SAE J 1752/3 which specifies the board and the loading of each pin.

Table 37. EMI data (1)

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. 16 MHz	Unit
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = +25 °C	0.1 MHz to 30 MHz	-5	dBµV
			30 MHz to 130 MHz	-5	
			130 MHz to 1 GHz	0	
			SAE EMI Level	1	-

1. Not tested in production.

Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity. For more details, refer to application note AN1181.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). Two models can be simulated: human body model and charge device model. This test conforms to the JESD22-A114A/A115A standard.

Table 38. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Maximum value (1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C	2000(2)	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)		1000	

1. Data based on characterization results, not tested in production.
2. Device sustained up to 3000 V during ESD trials.

Static latch-up

- **LU**: 3 complementary static tests are required on 6 parts to assess the latch-up performance. A supply overvoltage (applied to each power supply pin) and a current injection (applied to each input, output and configurable I/O pin) are performed on each sample. This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to application note AN1181.

Table 39. Electrical sensitivities

Symbol	Parameter	Class
LU	Static latch-up class	II

9.4 Thermal characteristics

The maximum chip junction temperature (T_{Jmax}) must never exceed the values given in *Table 16: General operating conditions on page 45*.

The maximum chip-junction temperature, T_{Jmax}, in degrees Celsius, may be calculated using the following equation:

$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$

Where:

- T_{Amax} is the maximum ambient temperature in °C
- Θ_{JA} is the package junction-to-ambient thermal resistance in °C/W
- P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$)
- P_{INTmax} is the product of I_{DD} and V_{DD}, expressed in watts. This is the maximum chip internal power.
- $P_{I/Omax}$ represents the maximum power dissipation on output pins
  where:
  $P_{I/Omax} = \Sigma (V_{OL}*I_{OL}) + \Sigma((V_{DD}-V_{OH})*I_{OH})$,
  taking into account the actual V_{OL}/I_{OL} and V_{OH}/I_{OH} of the I/Os at low and high level in the application.

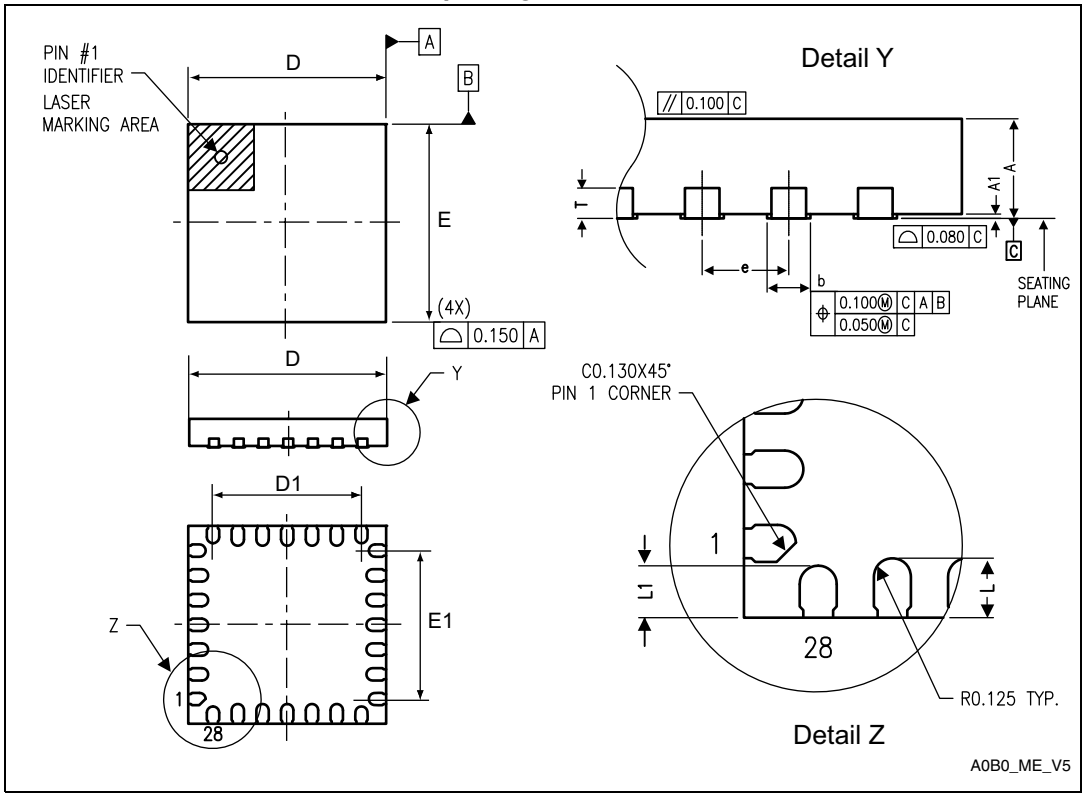
Table 40. Thermal characteristics(1)

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient UFQFPN 48 - 7 x 7 mm	32	°C/W
	Thermal resistance junction-ambient UFQFPN 28 - 4 x 4 mm	80	
	Thermal resistance junction-ambient TSSOP20	110	

1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

10.3 UFQFPN28 package information

Figure 34. UFQFPN28 - 28-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline



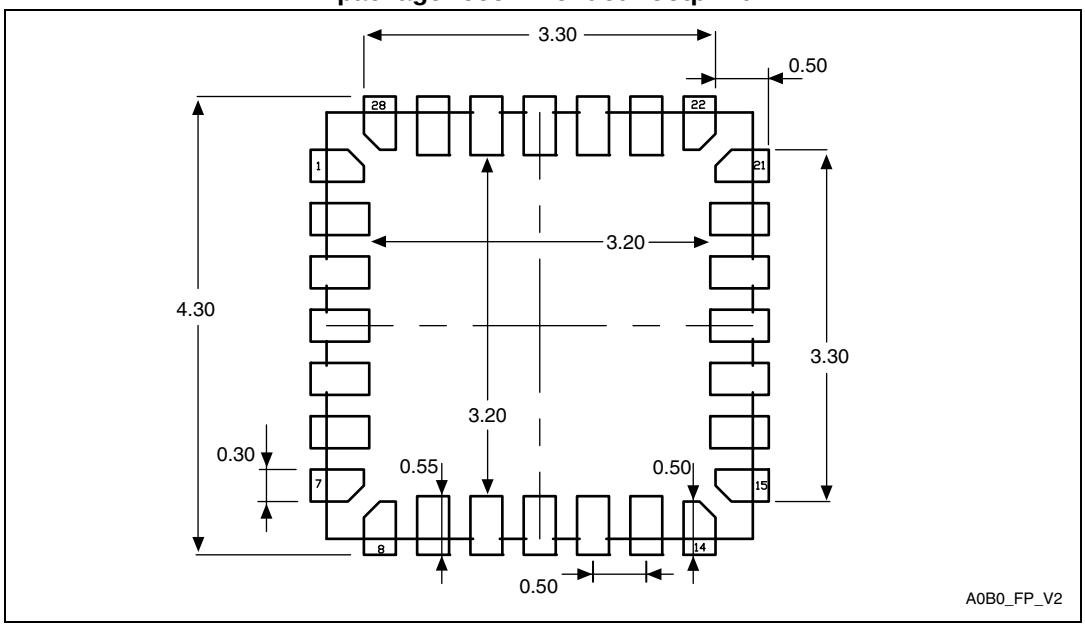
1. Drawing is not to scale.

Table 42. UFQFPN28 - 28-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data(1)

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	-	0.000	0.050	-	0.0000	0.0020
D	3.900	4.000	4.100	0.1535	0.1575	0.1614
D1	2.900	3.000	3.100	0.1142	0.1181	0.1220
E	3.900	4.000	4.100	0.1535	0.1575	0.1614
E1	2.900	3.000	3.100	0.1142	0.1181	0.1220
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
L1	0.250	0.350	0.450	0.0098	0.0138	0.0177
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 35. UFQFPN28 - 28-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package recommended footprint

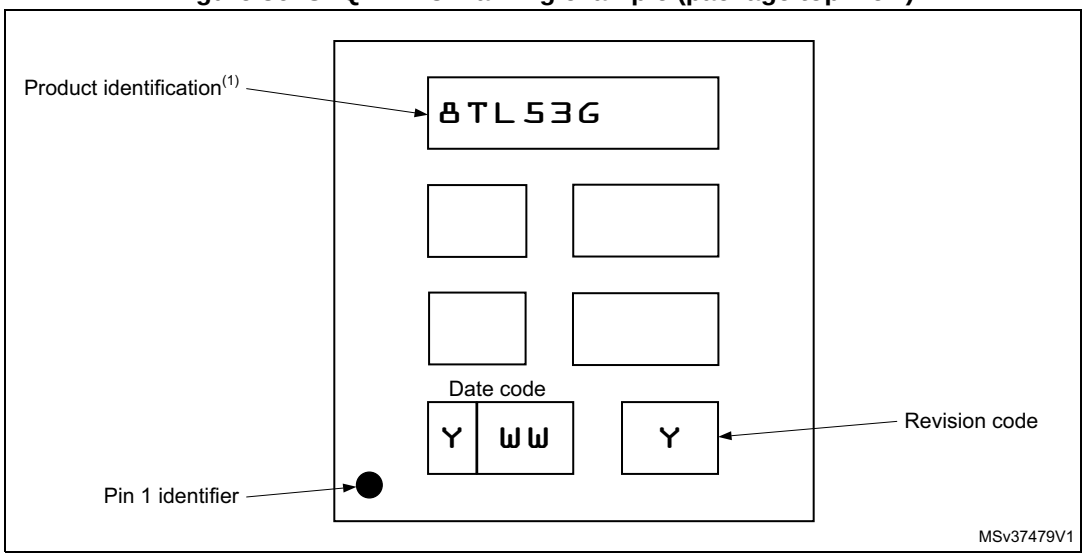


1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 36. UFQFPN28 marking example (package top view)



1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering