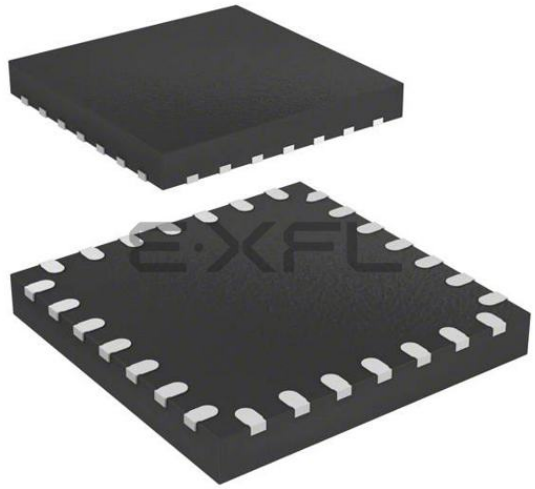

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, ProxSense, PWM, WDT
Number of I/O	17
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-UFQFN
Supplier Device Package	28-UFQFPN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8tl52g4u6

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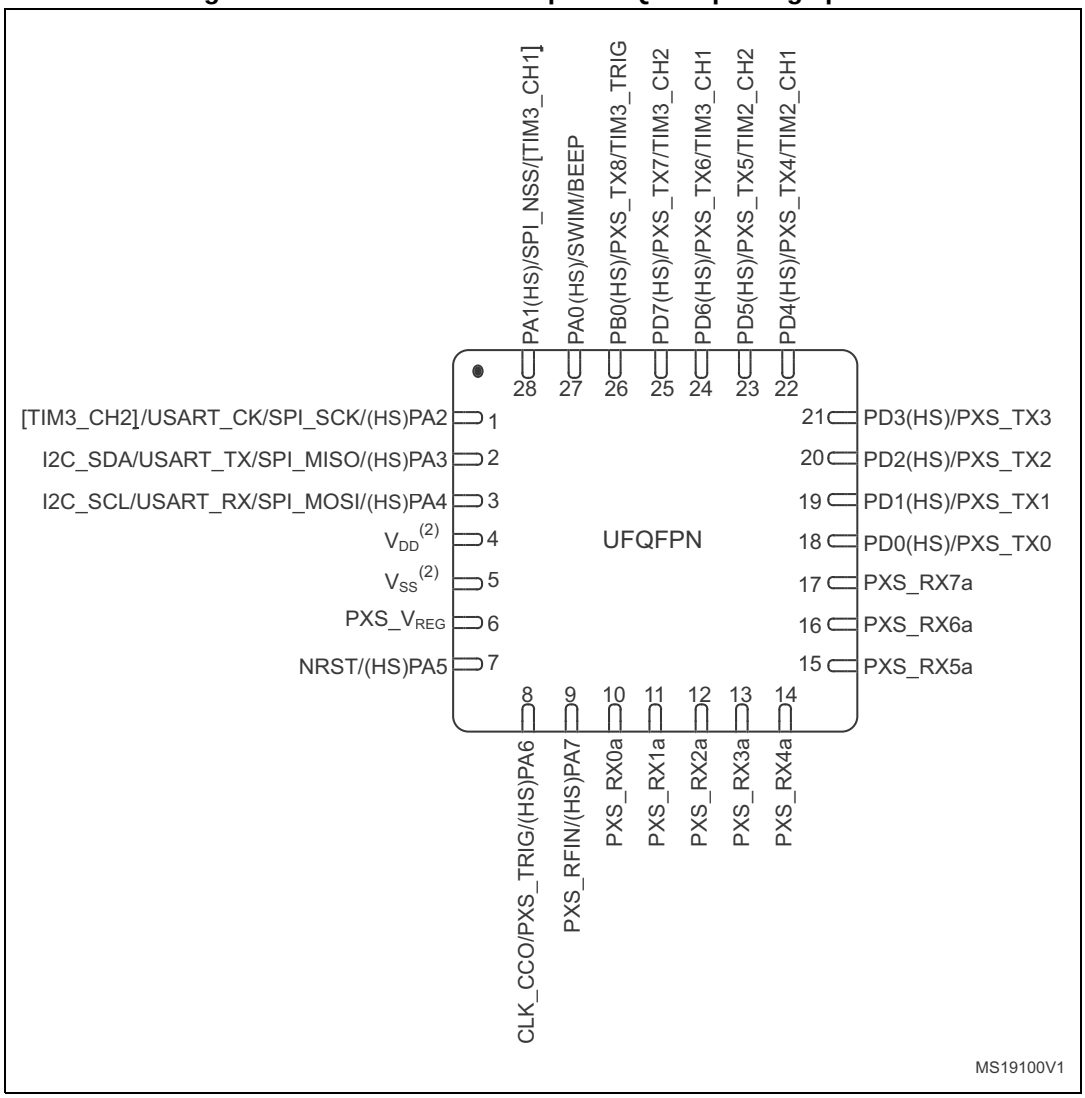
Figure 3. STM8TL53G4U6 28-pin UFQFPN package pinout



1. HS corresponds to 20 mA high sink/source capability.
2. Power supply pins must be correctly decoupled with capacitors near the pins. Please refer to the power supply circuitry details in *Section 9.3.2: Power supply on page 46* and the STM8TL5xxx reference manual (RM0312), Section 6: Power supply.

Table 5. Flash and RAM boundary addresses

Memory area	Size	Start address	End address
RAM	4 Kbyte	**0x00 0000**	0x00 0FFF
Flash program memory	16 Kbyte	0x00 8000	0x00 BFFF

Table 6. I/O Port hardware register map

Address	Block	Register label	Register name	Reset status
0x00 5000	Port A	PA_ODR	Port A data output latch register	0x00
0x00 5001		PA_IDR	Port A input pin value register	0xXX
0x00 5002		PA_DDR	Port A data direction register	0x00
0x00 5003		PA_CR1	Port A control register 1	0x00
0x00 5004		PA_CR2	Port A control register 2	0x00
0x00 5005	Port B	PB_ODR	Port B data output latch register	0x00
0x00 5006		PB_IDR	Port B input pin value register	0xXX
0x00 5007		PB_DDR	Port B data direction register	0x00
0x00 5008		PB_CR1	Port B control register 1	0x00
0x00 5009		PB_CR2	Port B control register 2	0x00
0x00 500A to 0x00 500E	Reserved area (5 byte)			
0x00 500F	Port D	PD_ODR	Port D data output latch register	0x00
0x00 5010		PD_IDR	Port D input pin value register	0xXX
0x00 5011		PD_DDR	Port D data direction register	0x00
0x00 5012		PD_CR1	Port D control register 1	0x00
0x00 5013		PD_CR2	Port D control register 2	0x00

Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5210	I2C	I2C_CR1	I2C control register 1	0x00
0x00 5211		I2C_CR2	I2C control register 2	0x00
0x00 5212		I2C_FREQR	I2C frequency register	0x00
0x00 5213		I2C_OAR1L	I2C own address register 1 low	0x00
0x00 5214		I2C_OAR1H	I2C own address register 1 high	0x00
0x00 5215		I2C_OAR2	I2C own address register 2	0x00
0x00 5216		I2C_DR	I2C data register	0x00
0x00 5217		I2C_SR1	I2C status register 1	0x00
0x00 5218		I2C_SR2	I2C status register 2	0x00
0x00 5219		I2C_SR3	I2C status register 3	0x00
0x00 521A		I2C_ITR	I2C interrupt control register	0x00
0x00 521B		I2C_CCRL	I2C Clock control register low	0x00
0x00 521C		I2C_CCRH	I2C Clock control register high	0x00
0x00 521D		I2C_TRISER	I2C TRISE register	0x00
0x00 521E to 0x00 522F	Reserved area (18 byte)			
0x00 5230	USART	USART_SR	USART status register	0xC0
0x00 5231		USART_DR	USART data register	0xXX
0x00 5232		USART_BRR1	USART baud rate register 1	0x00
0x00 5233		USART_BRR2	USART baud rate register 2	0x00
0x00 5234		USART_CR1	USART control register 1	0x00
0x00 5235		USART_CR2	USART control register 2	0x00
0x00 5236		USART_CR3	USART control register 3	0x00
0x00 5237		USART_CR4	USART control register 4	0x00
0x00 5238 to 0x00 524F	Reserved area (18 byte)			

Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5280	TIM3	TIM3_CR1	TIM3 control register 1	0x00
0x00 5281		TIM3_CR2	TIM3 control register 2	0x00
0x00 5282		TIM3_SMCR	TIM3 slave mode control register	0x00
0x00 5283		TIM3_ETR	TIM3 external trigger register	0x00
0x00 5284		TIM3_IER	TIM3 interrupt enable register	0x00
0x00 5285		TIM3_SR1	TIM3 status register 1	0x00
0x00 5286		TIM3_SR2	TIM3 status register 2	0x00
0x00 5287		TIM3_EGR	TIM3 event generation register	0x00
0x00 5288		TIM3_CCMR1	TIM3 capture/compare mode register 1	0x00
0x00 5289		TIM3_CCMR2	TIM3 capture/compare mode register 2	0x00
0x00 528A		TIM3_CCER1	TIM3 capture/compare enable register 1	0x00
0x00 528B		TIM3_CNTRH	TIM3 counter register high	0x00
0x00 528C		TIM3_CNTRL	TIM3 counter register low	0x00
0x00 528D		TIM3_PSCR	TIM3 prescaler register	0x00
0x00 528E		TIM3_ARRH	TIM3 auto-reload register high	0xFF
0x00 528F		TIM3_ARRL	TIM3 auto-reload register low	0xFF
0x00 5290		TIM3_CCR1H	TIM3 capture/compare register 1 high	0x00
0x00 5291		TIM3_CCR1L	TIM3 capture/compare register 1 low	0x00
0x00 5292		TIM3_CCR2H	TIM3 capture/compare register 2 high	0x00
0x00 5293		TIM3_CCR2L	TIM3 capture/compare register 2 low	0x00
0x00 5294		TIM3_BKR	TIM3 break register	0x00
0x00 5295		TIM3_OISR	TIM3 output idle state register	0x00
0x00 5296 to 0x00 52DF	Reserved area (74 byte)			
0x00 52E0	TIM4	TIM4_CR1	TIM4 control register 1	0x00
0x00 52E1		TIM4_CR2	TIM4 control register 2	0x00
0x00 52E2		TIM4_SMCR	TIM4 Slave mode control register	0x00
0x00 52E3		TIM4_IER	TIM4 interrupt enable register	0x00
0x00 52E4		TIM4_SR1	TIM4 Status register 1	0x00
0x00 52E5		TIM4_EGR	TIM4 event generation register	0x00
0x00 52E6		TIM4_CNTR	TIM4 counter register	0x00
0x00 52E7		TIM4_PSCR	TIM4 prescaler register	0x00
0x00 52E8		TIM4_ARR	TIM4 auto-reload register low	0xFF

Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 52E9 to 0x00 52FF	Reserved area (23 byte)			
0x00 5300	PXS	PXS_CR1	ProxSense control register 1	0x00
0x00 5301		PXS_CR2	ProxSense control register 2	0x00
0x00 5302		PXS_CR3	ProxSense control register 3	0x04
0x00 5303		Reserved area (1 byte)		
0x00 5304		PXS_ISR	ProxSense interrupt and status register	0x00
0x00 5305		Reserved area (1 byte)		
0x00 5306		PXS_CKCR1	ProxSense clock control register 1	0x30
0x00 5307		PXS_CKCR2	ProxSense clock control register 2	0x11
0x00 5308		PXS_RXENRH	ProxSense receiver enable register high	0x00
0x00 5309		PXS_RXENRL	ProxSense receiver enable register low	0x00
0x00 5310 to 0x00 5311	Reserved area (2 byte)			
0x00 530A	PXS	PXS_RXCR1H	ProxSense receiver control register 1 high	0x00
0x00 530B		PXS_RXCR1L	ProxSense receiver control register 1 low	0x00
0x00 530C		PXS_RXCR2H	ProxSense receiver control register 2 high	0x00
0x00 530D		PXS_RXCR2L	ProxSense receiver control register 2 low	0x00
0x00 530E		PXS_RXCR3H	ProxSense receiver control register 3 high	0x00
0x00 530F		PXS_RXCR3L	ProxSense receiver control register 3 low	0x00
0x00 5312		PXS_RXINSRH	ProxSense receiver inactive state register high	0x00
0x00 5313		PXS_RXINSRL	ProxSense receiver inactive state register low	0x00
0x00 5314 to 0x00 5315	Reserved area (2 byte)			
0x00 5316	PXS	PXS_TXENRH	ProxSense transmit enable register high	0x00
0x00 5317		PXS_TXENRL	ProxSense transmit enable register low	0x00
0x00 5318 to 0x00 5319	Reserved area (2 byte)			

6 Interrupt vector mapping

Table 9. Interrupt mapping

IRQ No.	Source block	Description	Wakeup from Halt mode	Wakeup from Active-halt mode	Wakeup from Wait (WFI mode)	Wakeup from Wait (WFE mode)(1)	Vector address
	RESET	Reset	Yes	Yes	Yes	Yes	0x00 8000
	TRAP	Software interrupt	-	-	-	-	0x00 8004
0	Reserved						0x00 8008
1	FLASH	FLASH end of programing/ write attempted to protected page interrupt	-	-	Yes	Yes	0x00 800C
2	PXS	End of conversion/First conversion completed	-	Yes(2)	Yes	Yes	0x00 8010
3	Reserved						0x00 8011 -0x00 8017
4	AWU	Auto wakeup from Halt	-	Yes	Yes	Yes	0x00 8018
5	Reserved						0x00 801C
6	EXTIB	External interrupt port B	Yes	Yes	Yes	Yes	0x00 8020
7	EXTID	External interrupt port D	Yes	Yes	Yes	Yes	0x00 8024
8	EXTI0	External interrupt 0	Yes	Yes	Yes	Yes	0x00 8028
9	EXTI1	External interrupt 1	Yes	Yes	Yes	Yes	0x00 802C
10	EXTI2	External interrupt 2	Yes	Yes	Yes	Yes	0x00 8030
11	EXTI3	External interrupt 3	Yes	Yes	Yes	Yes	0x00 8034
12	EXTI4	External interrupt 4	Yes	Yes	Yes	Yes	0x00 8038
13	EXTI5	External interrupt 5	Yes	Yes	Yes	Yes	0x00 803C
14	EXTI6	External interrupt 6	Yes	Yes	Yes	Yes	0x00 8040
15	EXTI7	External interrupt 7	Yes	Yes	Yes	Yes	0x00 8044
16	Reserved						0x00 8048
17	Reserved						0x00 804C -0x00 804F
18	Reserved						0x00 8050
19	TIM2	TIM2 update/overflow/ trigger/break interrupt	-	-	Yes	Yes	0x00 8054
20	TIM2	TIM2 capture/compare interrupt	-	-	Yes	Yes	0x00 8058
21	TIM3	TIM3 update/overflow/ trigger/break interrupt	-	-	Yes	Yes	0x00 805C

Table 9. Interrupt mapping (continued)

IRQ No.	Source block	Description	Wakeup from Halt mode	Wakeup from Active-halt mode	Wakeup from Wait (WFI mode)	Wakeup from Wait (WFE mode)(1)	Vector address
22	TIM3	TIM3 capture/compare interrupt	-	-	Yes	Yes	0x00 8060
23-24	Reserved						0x00 8064-0x00 806B
25	TIM4	TIM4 update/overflow/ trigger interrupt	-	-	Yes	Yes	0x00 806C
26	SPI	SPI TX buffer empty/ RX buffer not empty/ error/wakeup interrupt	Yes	Yes	Yes	Yes	0x00 8070
27	USART	USART transmit data register empty/ transmission complete interrupt	-	-	Yes	Yes	0x00 8074
28	USART	USART received data ready/overrun error/ idle line detected/parity error/global error interrupt	-	-	Yes	Yes	0x00 8078
29	I2C	I2C interrupt(3)	Yes	Yes	Yes	Yes	0x00 807C

1. The Low power wait mode is entered when executing a WFE instruction in Low power run mode. In WFE mode, the interrupt is served if it has been previously enabled. After processing the interrupt, the processor goes back to WFE mode. When the interrupt is configured as a wakeup event, the CPU wakes up and resumes processing.
2. ProxSense activated before executing HALT instruction.
3. The device is woken up from Halt or Active-halt mode only when the address received matches the interface address.

8 Unique ID

STM8TL5xx4 devices feature a 96-bit unique device identifier which provides a reference number that is unique for any device and in any context. The 96 bits of the identifier can never be altered by the user.

The unique device identifier can be read in single byte and may then be concatenated using a custom algorithm.

The unique device identifier is ideally suited:

- For use as serial numbers
- For use as security keys to increase the code security in the program memory while using and combining this unique ID with software cryptographic primitives and protocols before programming the internal memory
- To activate secure boot processes

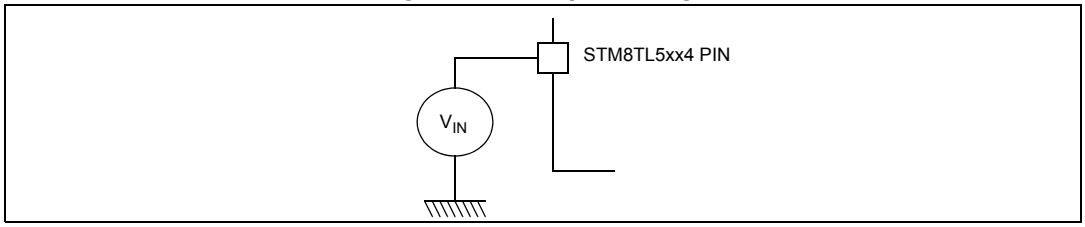
Table 12. Unique ID registers (96 bits)

Address	Content description	Unique ID bits							
		7	6	5	4	3	2	1	0
0x4925	X coordinate on the wafer	U_ID[7:0]							
0x4926		U_ID[15:8]							
0x4927	Y coordinate on the wafer	U_ID[23:16]							
0x4928		U_ID[31:24]							
0x4929	Wafer number	U_ID[39:32]							
0x492A	Lot number	U_ID[47:40]							
0x492B		U_ID[55:48]							
0x492C		U_ID[63:56]							
0x492D		U_ID[71:64]							
0x492E		U_ID[79:72]							
0x492F		U_ID[87:80]							
0x4930		U_ID[95:88]							

9.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 9*.

Figure 9. Pin input voltage



9.2 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 13. Voltage characteristics

Symbol	Ratings		Min	Max	Unit
V_{DD}- V_{SS}	External supply voltage (including V_{DD} and V_{DDIO})(1)		−0.3	4.0	V
V_{IN}(2)	Receiver channel pins (PXS_Rx0a...Rx9b)		V_{SS}−0.3	PXS_V_{REG} (~1.45)	
	Input voltage on PB0...7 and PD0...7(3)	Pins used as General purpose I/O	V_{SS}−0.3	4.0	
		Pins used as transmitter channel pins (PXS_Tx0 to PXS_Tx15)	V_{SS}−0.3	PXS_V_{REG} (~1.45)	
	Input voltage on any PA pins		V_{SS}−0.3	4.0	
V_{ESD}	Electrostatic discharge voltage	see *Absolute maximum ratings (electrical sensitivity) on page 69*			

1. All power (V_{DD}, V_{DDIO}) and ground (V_{SS}, V_{SSIO}) pins must always be connected to the external power supply.
2. V_{IN} maximum must always be respected. Refer to *Table 14.* for maximum allowed injected current values.
3. Current injection on these pins is not allowed.

9.3.6 Clock and timing characteristics

Internal clock source

The parameters given in *Table 24* are derived from tests performed under ambient temperature and V_{DD} supply voltage. They are subject to general operating conditions for V_{DD} and T_A.

High speed internal RC oscillator

Table 24. HSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{HSI}	Frequency	V_{DD} = 3.0 V	-	16	-	MHz
ACC_{HSI}	Accuracy of HSI oscillator (factory calibrated)	V_{DD} = 3.0 V, T_A = 25 °C	–1	-	1	%
		1.65 V ≤ VDD ≤ 3.6 V, T_A = -40 to 85°C	–3	-	3	%
$I_{DD(HSI)}$	HSI oscillator power consumption		-	70	100	µA

1. V_{DD} = 3V, T_A = –40 to 125 °C, unless otherwise specified.

Figure 14. Typical HSI frequency vs. V_{DD}

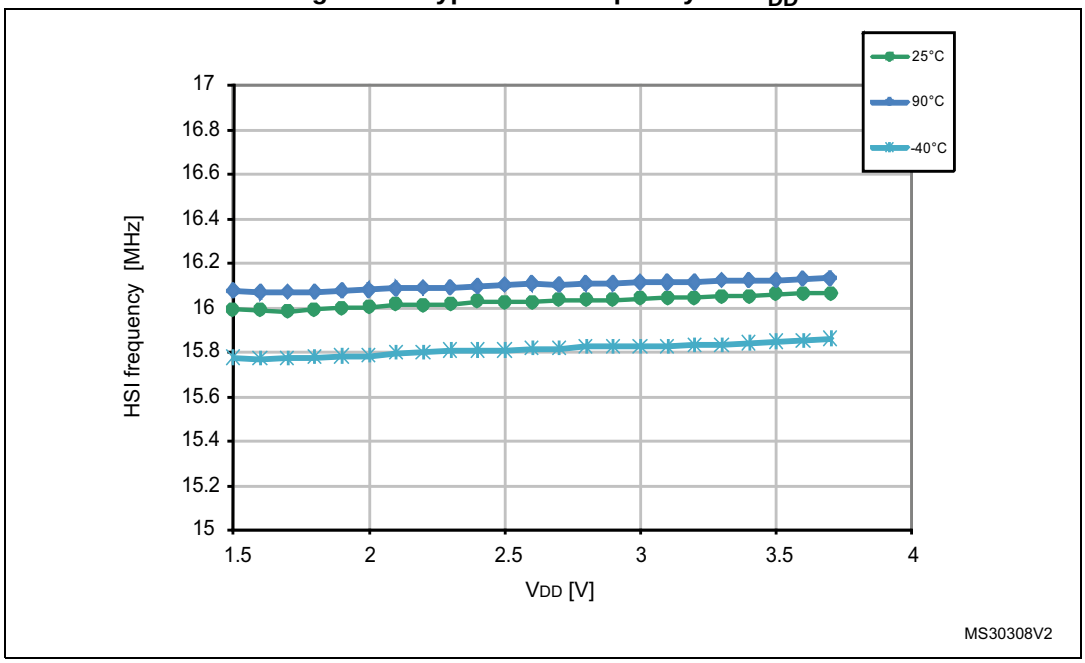
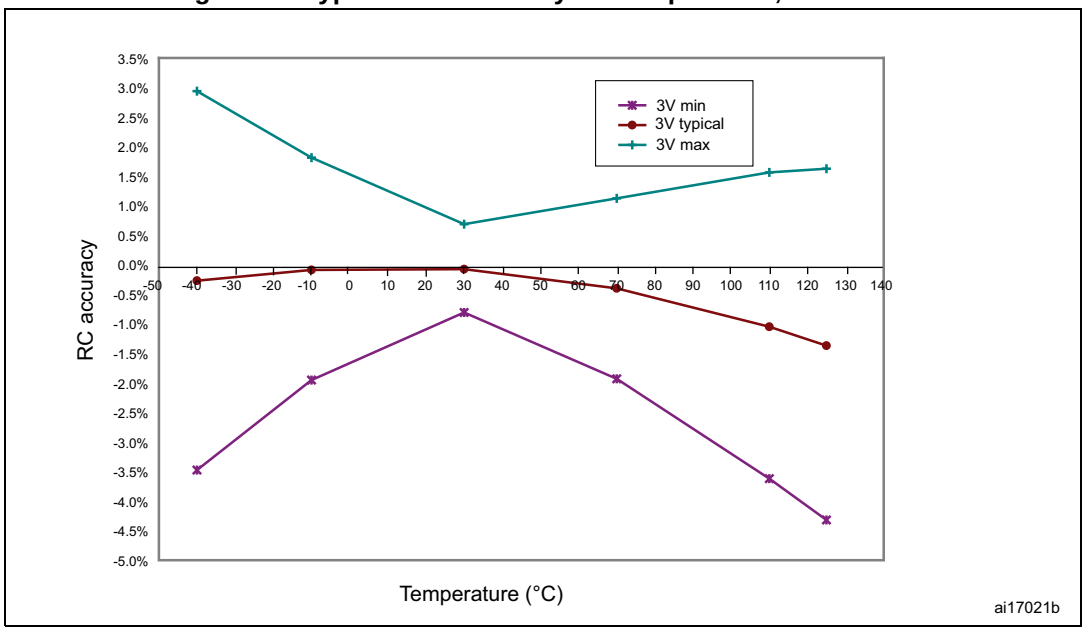


Figure 15. Typical HSI accuracy vs. temperature, VDD = 3 V



High speed ProxSense RC oscillator

Table 25. HSI_PXS oscillator characteristics(1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{HSI_PXS}	Frequency	V_{DD} = 3.0 V	-	16	-	MHz

1. V_{DD} = 3V, T_A = –40 to 85 °C, unless otherwise specified.

Low speed internal RC oscillator (LSI)

Table 26. LSI oscillator characteristics (1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{LSI}	Frequency		26	38	56	kHz
$f_{drift(LSI)}$	LSI oscillator frequency drift(2)	0 °C ≤ T_A ≤ 85°C	–12	-	11	%

1. V_{DD} = 1.65 V to 3.6 V, T_A = –40 to 85°C unless otherwise specified.
2. For each individual part, this value is the frequency drift from the initial measured frequency.

9.3.8 I/O port pin characteristics

General characteristics

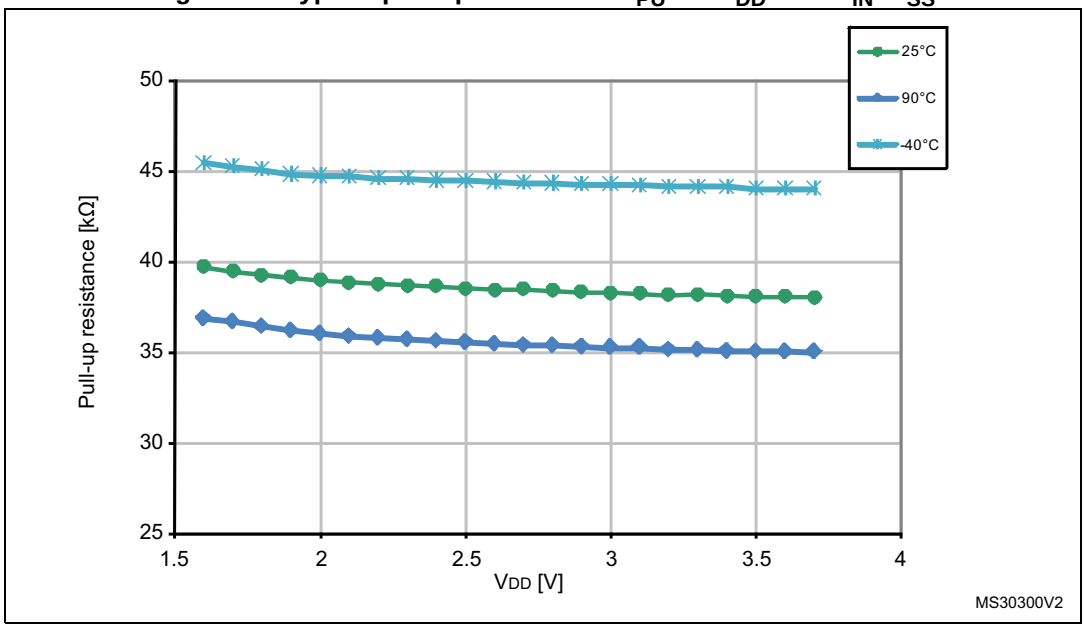
Subject to general operating conditions for V_{DD} and T_A unless otherwise specified. All unused pins must be kept at a fixed voltage: using the output mode of the I/O for example or an external pull-up or pull-down resistor.

Table 31. I/O static characteristics (1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage(2)	Standard I/Os	V_{SS}–0.3	-	0.3 x V_{DD}	V
V_{IH}	Input high level voltage(2)	Standard I/Os	0.70 x V_{DD}	-	V_{DD}+0.3	
V_{hys}	Schmitt trigger voltage hysteresis(3)	Standard I/Os	-	200	-	mV
I_{lkg}	Input leakage current(4)	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	50	nA
		$V_{SS} \le V_{IN} \le V_{reg}$ Rx, Tx I/Os	-	-	50	
R_{PU}	Weak pull-up equivalent resistor(5)	$V_{IN} = V_{SS}$	30	45	60	kΩ
C_{IO}(6)	I/O pin capacitance	-	-	5	-	pF

1. V_{DD} = 3.0 V, T_A = –40 to 85 °C unless otherwise specified.
2. Data based on characterization results, not tested in production.
3. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested.
4. The maximum value may be exceeded if negative current is injected on adjacent pins.
5. R_{PU} pull-up equivalent resistor based on a resistive transistor (corresponding I_{PU} current characteristics.
6. Data guaranteed by Design, not tested in production.

Figure 17. Typical pull-up resistance R_{PU} vs. V_{DD} with $V_{IN}=V_{SS}$



Output driving current

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 32. Output driving current (high sink ports)

I/O type	Symbol	Parameter	Conditions	Min.	Max.	Unit
Standard	V_{OL} (1)	Output low level voltage for an I/O pin	I_{IO} = +2 mA, V_{DD} = 1.8 V	-	0.45	V
			I_{IO} = +2 mA, V_{DD} = 3.0 V	-	0.45	
			I_{IO} = +10 mA, V_{DD} = 3.0 V	-	0.7	
	V_{OH} (2)	Output high level voltage for an I/O pin	I_{IO} = –1 mA, V_{DD} = 1.8 V	V_{DD}-0.45	-	
			I_{IO} = –1 mA, V_{DD} = 3.0 V	V_{DD}-0.45	-	
			I_{IO} = –10 mA, V_{DD} = 3.0 V	V_{DD}-0.7	-	
ProxSense I/O	V_{OH}	Output high level voltage for PXS_TX ProxSense I/O	I_{PXS_TX} = 0.2 mA	V_{REG}	-	
	V_{OH}	Output high level voltage for PXS_RX ProxSense I/O	I_{PXS_RX} = 0.1 mA	V_{REG}	-	

1. The I_{IO} current sunk must always respect the absolute maximum rating and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. The I_{IO} current sourced must always respect the absolute maximum rating and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.

Figure 19. Typ. V_{OL} at V_{DD} = 1.8 V (standard ports)

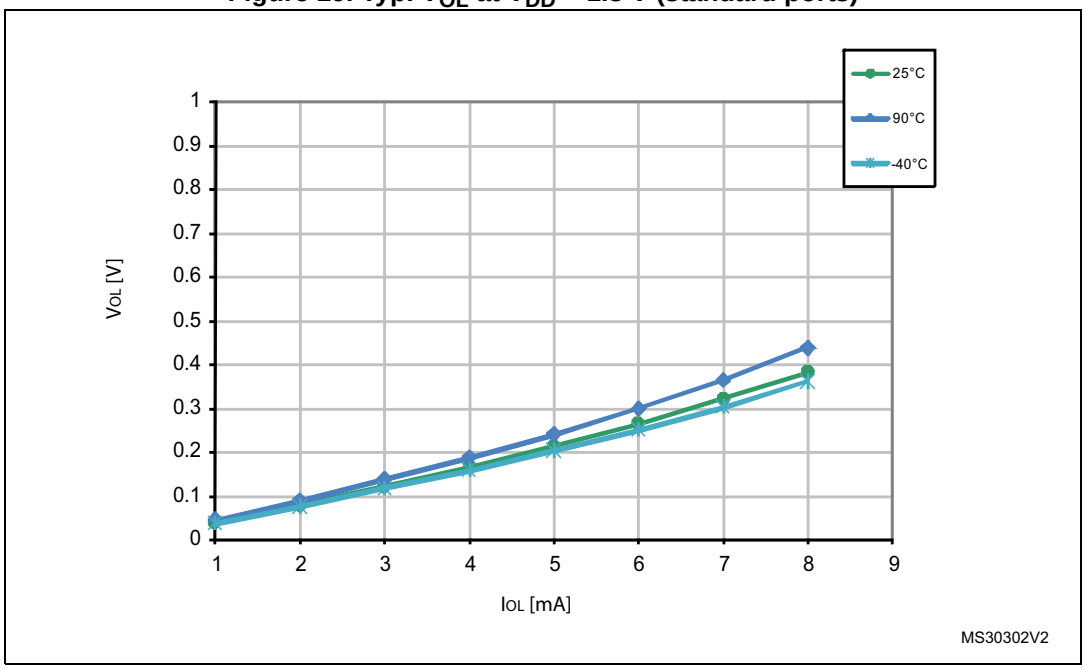
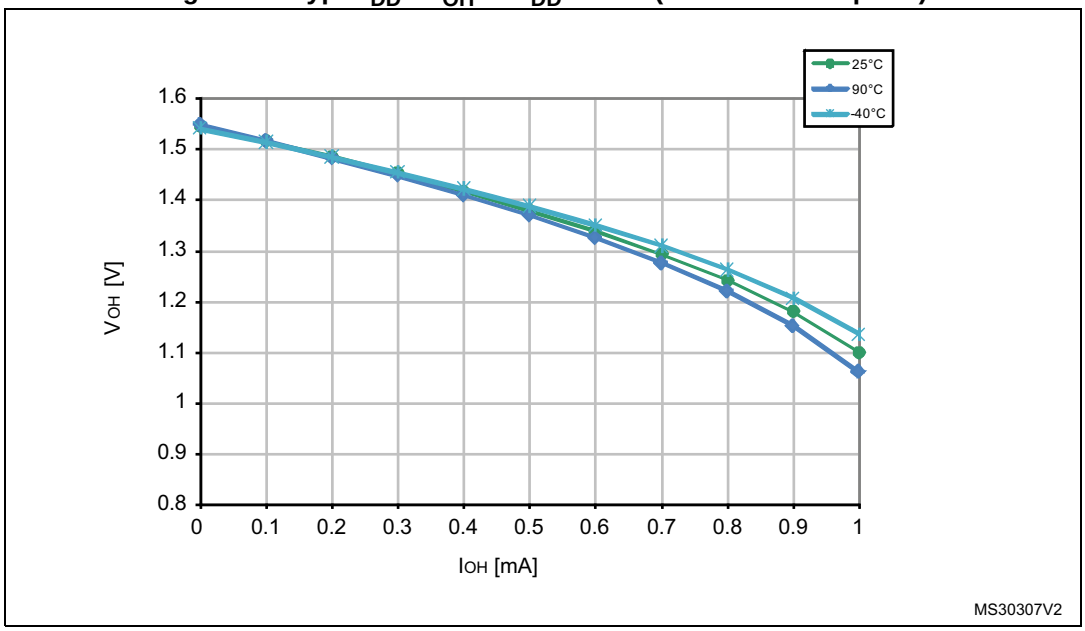


Figure 24. Typ. V_{DD} - V_{OH} at V_{DD} = 1.8V (ProxSense RX ports)



9.3.9 Communication interfaces

Serial peripheral interface (SPI)

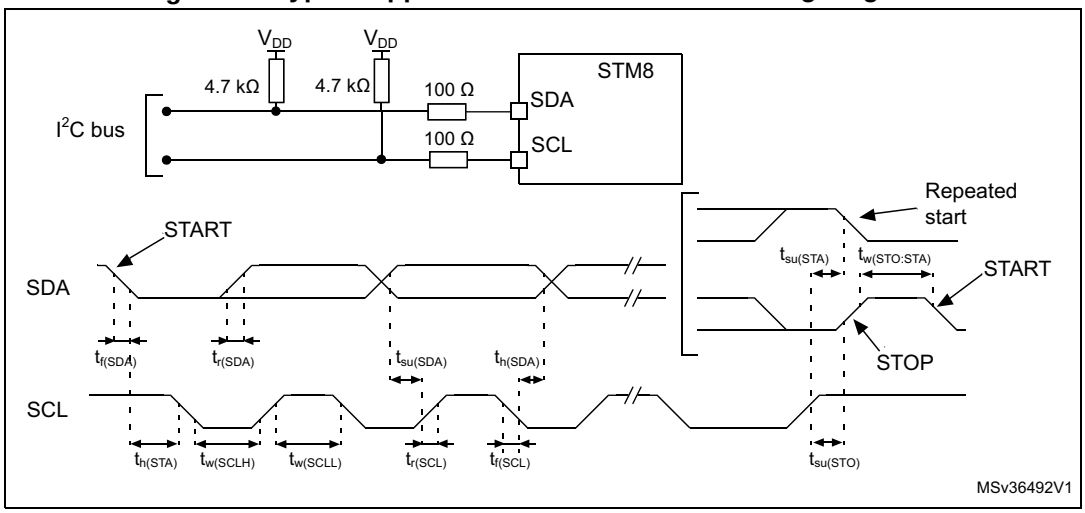
The parameters given in *Table 34* are derived from tests performed under ambient temperature, f_{MASTER} frequency and V_{DD} supply voltage conditions summarized in *Section 9.3.1 on page 45*, unless otherwise specified. Refer to I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 34. SPI characteristics

Symbol	Parameter	Conditions(1)	Min.	Max.	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	0	8	MHz
		Slave mode	0	8	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF	-	30	ns
$t_{su(NSS)}$(2)	NSS setup time	Slave mode	4 x t_{MASTER}	-	
$t_{h(NSS)}$(2)	NSS hold time	Slave mode	80	-	
$t_{w(SCKH)}$(2) $t_{w(SCKL)}$(2)	SCK high and low time	Master mode, f_{MASTER} = 8 MHz, f_{SCK}= 4 MHz	105	145	
$t_{su(MI)}$(2) $t_{su(SI)}$(2)	Data input setup time	Master mode	30	-	
		Slave mode	3	-	
$t_{h(MI)}$(2) $t_{h(SI)}$(2)	Data input hold time	Master mode	15	-	
		Slave mode	0	-	
$t_{a(SO)}$(2)(3)	Data output access time	Slave mode	-	3x t_{MASTER}	
$t_{dis(SO)}$(2)(4)	Data output disable time	Slave mode	30	-	
$t_{v(SO)}$(2)	Data output valid time	Slave mode (after enable edge)	-	60	
$t_{v(MO)}$(2)	Data output valid time	Master mode (after enable edge)	-	20	
$t_{h(SO)}$(2)	Data output hold time	Slave mode (after enable edge)	15	-	
$t_{h(MO)}$(2)		Master mode (after enable edge)	1	-	

1. Parameters are given by selecting 10–MHz I/O output frequency.
2. Values based on design simulation and/or characterization results, and not tested in production.
3. Min time is for the minimum time to drive the output and max time is for the maximum time to validate the data.
4. Min time is for the minimum time to invalidate the output and max time is for the maximum time to put the data in Hi–Z.

Figure 30. Typical application with I²C bus and timing diagram [1)]



1. Measurement points are done at CMOS levels: 0.3 x V_{DD} and 0.7 x V_{DD}.

9.3.10 EMC characteristics

Susceptibility tests are performed on a sample 36 basis during product characterization.

Functional EMS (electromagnetic susceptibility)

Based on a simple running application on the product (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electrostatic discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Prequalification trials:

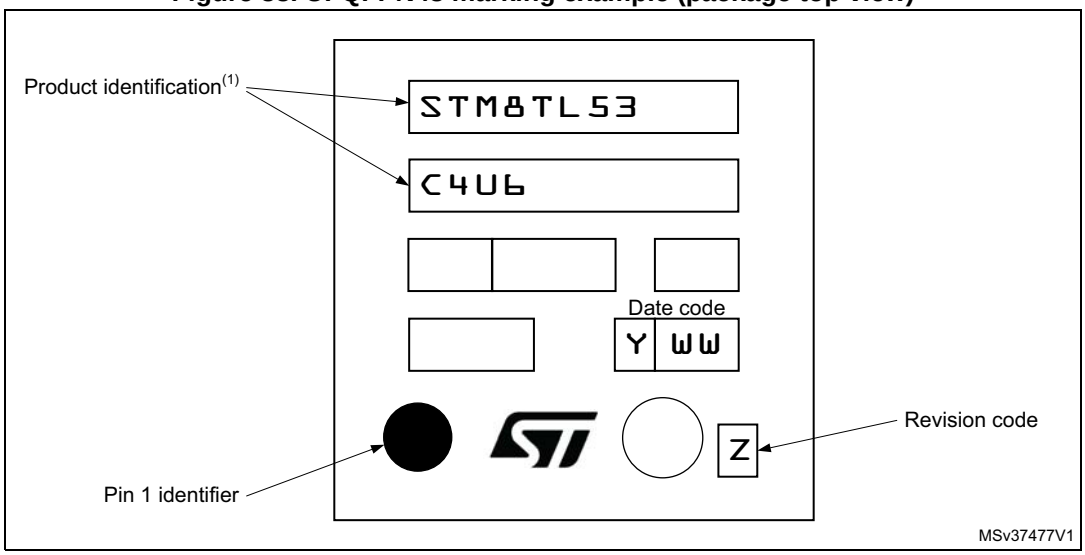
Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 33. UFQFPN48 marking example (package top view)

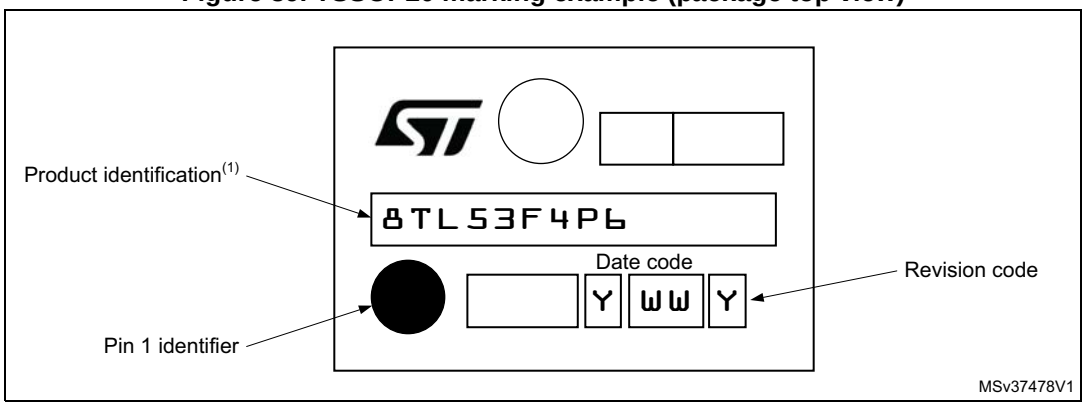


1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 39. TSSOP20 marking example (package top view)



1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

12 STM8 development tools

Development tools for the STM8 microcontrollers include the very low-cost debugger and programmer tool ST-Link supported by a complete software tool package including C compiler, assembler and integrated development environment with high-level language debugger. In addition, the STM8 is to be supported by a complete range of tools including starter kits, evaluation boards and a low-cost in-circuit debugger/programmer.

12.1 Software tools

STM8 development tools are supported by a complete, free software package from STMicroelectronics that includes ST Visual Develop (STVD) IDE and the ST Visual Programmer (STVP) software interface. STVD provides seamless integration of the Cosmic and Raisonance C compilers for STM8. A free version that outputs up to 32 Kbytes of code is available.

12.1.1 STM8 toolset

STM8 toolset with STVD integrated development environment and STVP programming software is available for free download at www.st.com. This package includes:

ST Visual Develop (STVD) – Full-featured integrated development environment from ST, featuring

- Seamless integration of C and ASM toolsets
- Full-featured debugger
- Project management
- Syntax highlighting editor
- Integrated programming interface

ST Visual Programmer (STVP) – Easy-to-use, unlimited graphical interface allowing read, write and verify of your STM8 microcontroller Flash program memory, data EEPROM and option bytes. STVP also offers project mode for saving programming configurations and automating programming sequences.