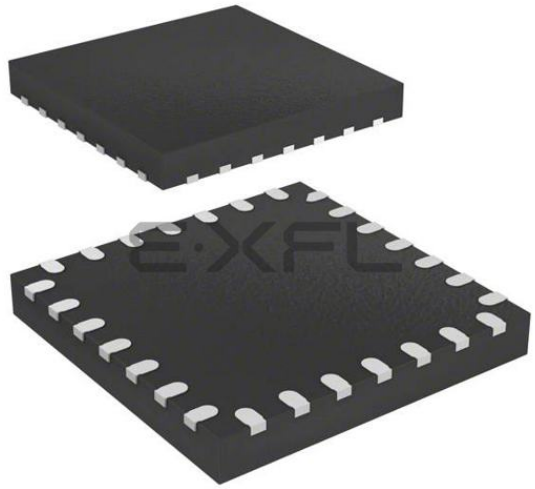

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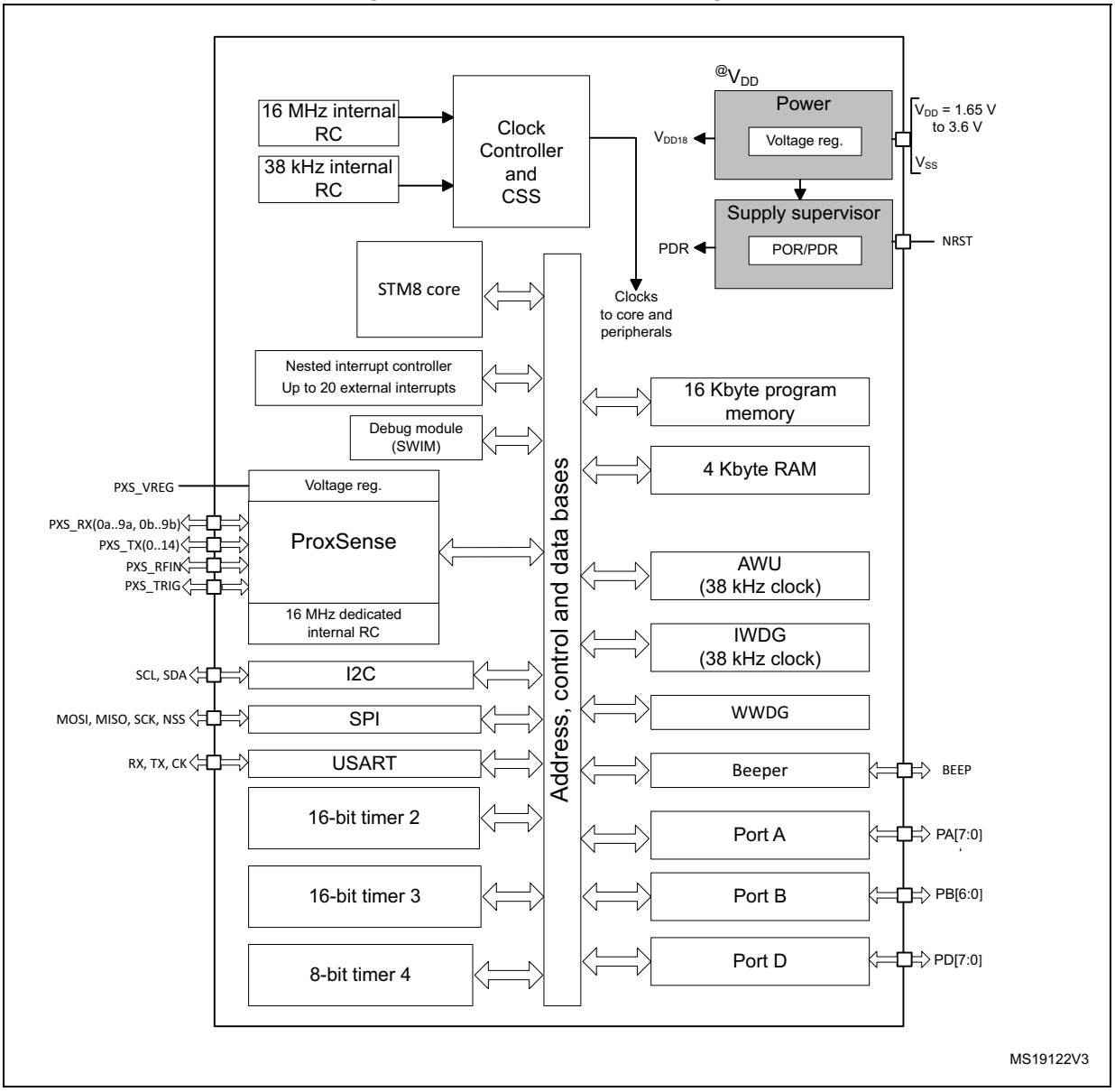
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, ProxSense, PWM, WDT
Number of I/O	17
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-UFQFN
Supplier Device Package	28-UFQFPN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8tl53g4u6

3 Product overview

Figure 1. STM8TL5xx4 block diagram

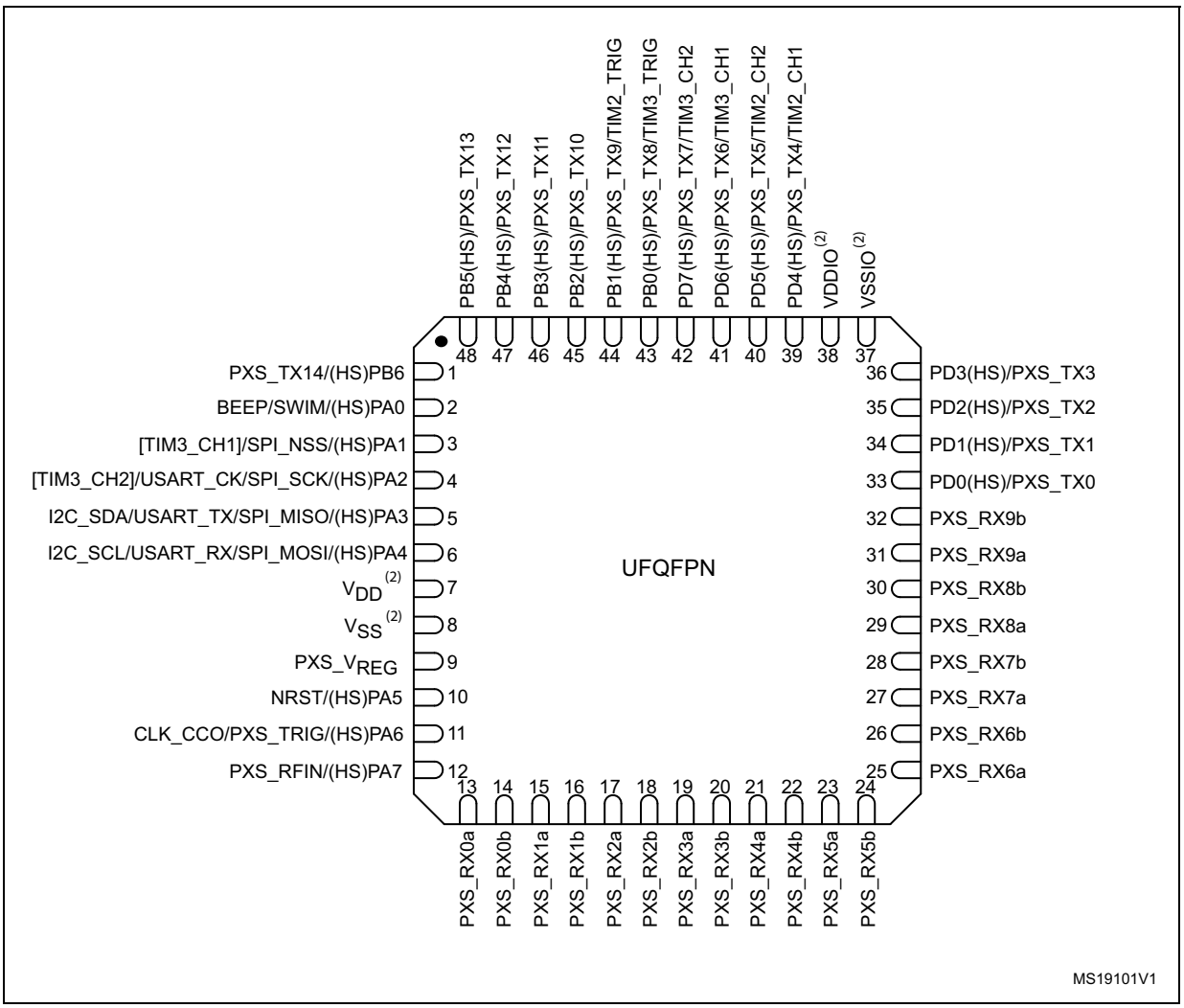


Legend:

AWU: Auto-wakeup unit
Int. RC: internal RC oscillator
I²C: Inter-integrated circuit multimaster interface
POR/PDR: Power on reset / power down reset
SPI: Serial peripheral interface
SWIM: Single wire interface module
USART: Universal synchronous / asynchronous receiver / transmitter
IWDG: Independent watchdog
WWDG: Window watchdog
ProxSense™: capacitive sensing peripheral

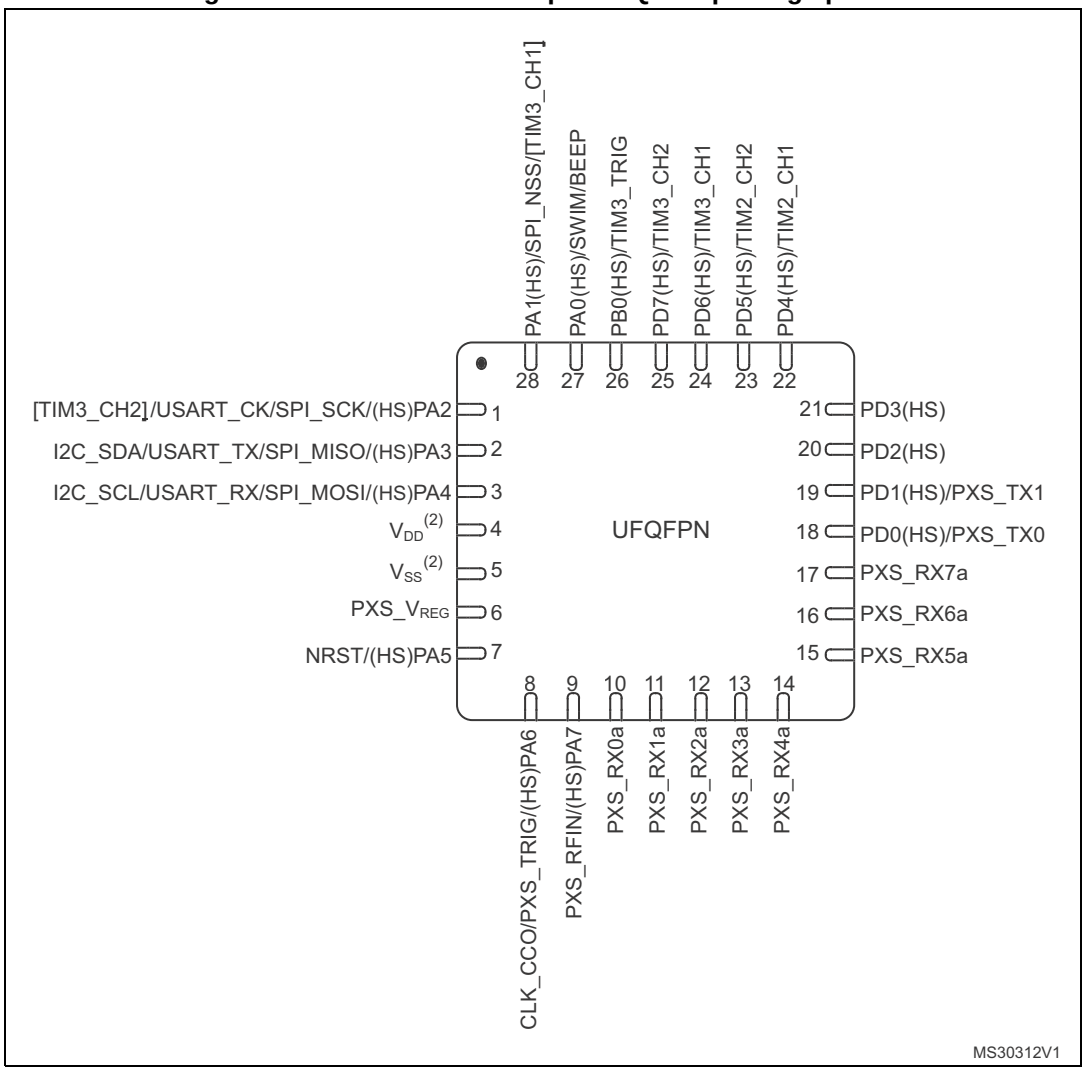
4 Pin description

Figure 2. STM8TL53 48-pin UFQFPN package pinout



1. HS corresponds to 20 mA high sink/source capability.
2. Power supply pins must be correctly decoupled with capacitors near the pins. Please refer to the power supply circuitry details in *Section 9.3.2: Power supply on page 46* and the STM8TL5xxx reference manual (RM0312), Section 6: Power supply.

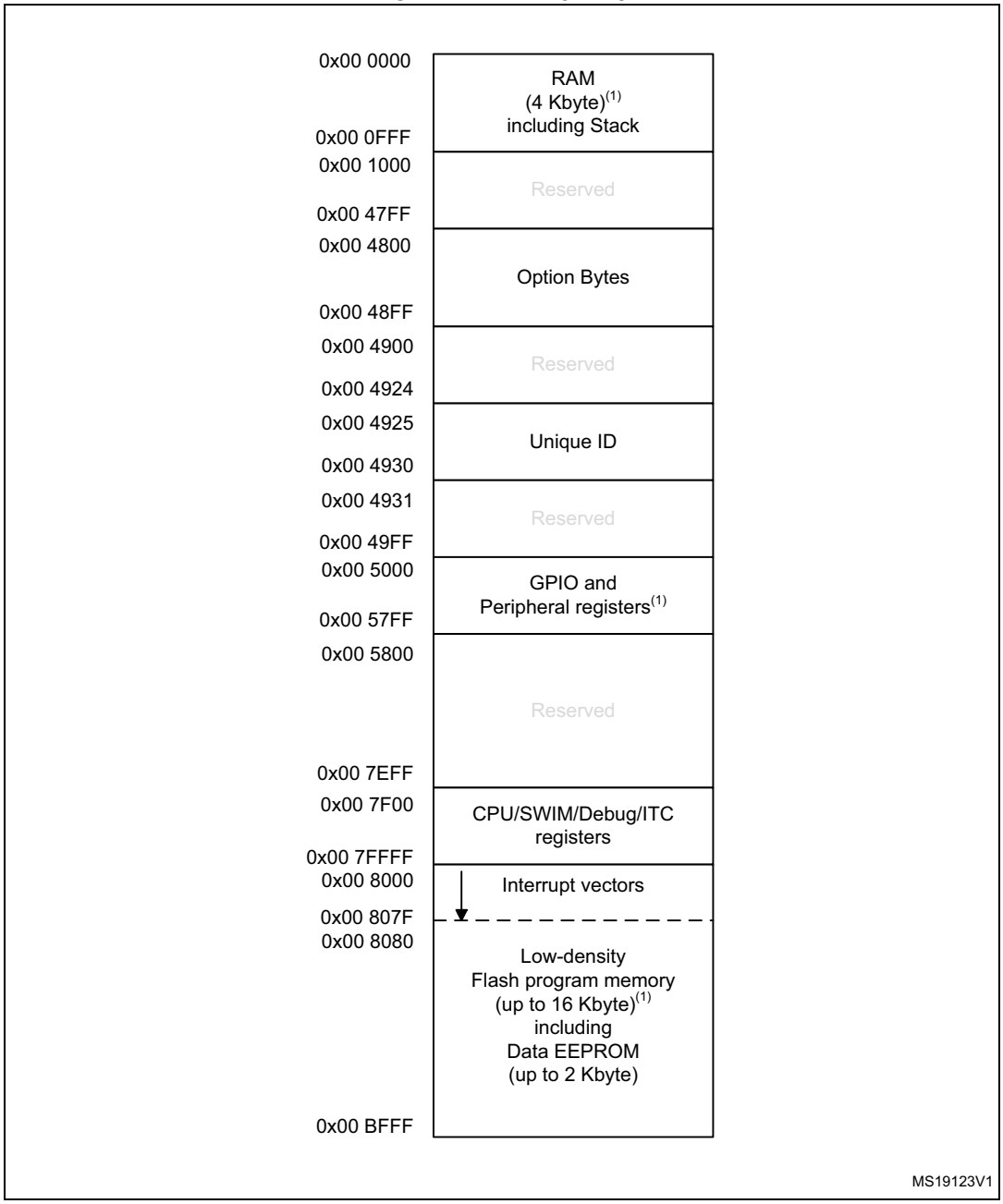
Figure 4. STM8TL52G4U6 28-pin UFQFPN package pinout



1. HS corresponds to 20 mA high sink/source capability.
2. Power supply pins must be correctly decoupled with capacitors near the pins. Please refer to the power supply circuitry details in *Section 9.3.2: Power supply on page 46* and the STM8TL5xxx reference manual (RM0312) Section 6: Power supply.

5 Memory and register map

Figure 7. Memory map



1. Refer to *Table 7* for an overview of hardware register mapping, to *Table 6* for details on I/O port hardware registers, and to *Table 8* for information on CPU/SWIM/debug module controller registers.

Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5210	I2C	I2C_CR1	I2C control register 1	0x00
0x00 5211		I2C_CR2	I2C control register 2	0x00
0x00 5212		I2C_FREQR	I2C frequency register	0x00
0x00 5213		I2C_OAR1L	I2C own address register 1 low	0x00
0x00 5214		I2C_OAR1H	I2C own address register 1 high	0x00
0x00 5215		I2C_OAR2	I2C own address register 2	0x00
0x00 5216		I2C_DR	I2C data register	0x00
0x00 5217		I2C_SR1	I2C status register 1	0x00
0x00 5218		I2C_SR2	I2C status register 2	0x00
0x00 5219		I2C_SR3	I2C status register 3	0x00
0x00 521A		I2C_ITR	I2C interrupt control register	0x00
0x00 521B		I2C_CCRL	I2C Clock control register low	0x00
0x00 521C		I2C_CCRH	I2C Clock control register high	0x00
0x00 521D		I2C_TRISER	I2C TRISE register	0x00
0x00 521E to 0x00 522F	Reserved area (18 byte)			
0x00 5230	USART	USART_SR	USART status register	0xC0
0x00 5231		USART_DR	USART data register	0xXX
0x00 5232		USART_BRR1	USART baud rate register 1	0x00
0x00 5233		USART_BRR2	USART baud rate register 2	0x00
0x00 5234		USART_CR1	USART control register 1	0x00
0x00 5235		USART_CR2	USART control register 2	0x00
0x00 5236		USART_CR3	USART control register 3	0x00
0x00 5237		USART_CR4	USART control register 4	0x00
0x00 5238 to 0x00 524F	Reserved area (18 byte)			

Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5350	PXS	PXS_RX0EPCCSELR	ProxSense receiver electrode parasitic compensation capacitor selection register	0x00
0x00 5351		PXS_RX1EPCCSELR	ProxSense receiver electrode parasitic compensation capacitor selection register	0x00
0x00 5352		PXS_RX2EPCCSELR	ProxSense receiver electrode parasitic compensation capacitor selection register	0x00
0x00 5353		PXS_RX3EPCCSELR	ProxSense receiver electrode parasitic compensation capacitor selection register	0x00
0x00 5354		PXS_RX4EPCCSELR	ProxSense receiver electrode parasitic compensation capacitor selection register	0x00
0x00 5355		PXS_RX5EPCCSELR	ProxSense receiver electrode parasitic compensation capacitor selection register	0x00
0x00 5356		PXS_RX6EPCCSELR	ProxSense receiver electrode parasitic compensation capacitor selection register	0x00
0x00 5357		PXS_RX7EPCCSELR	ProxSense receiver electrode parasitic compensation capacitor selection register	0x00
0x00 5358		PXS_RX8EPCCSELR	ProxSense receiver electrode parasitic compensation capacitor selection register	0x00
0x00 5359		PXS_RX9EPCCSELR	ProxSense receiver electrode parasitic compensation capacitor selection register	0x00
0x00 535A to 0x00 7EFF	Reserved area (11174 byte)			

1. After power-on reset.

Table 8. CPU/SWIM/debug module/interrupt controller registers

Address	Block	Register label	Register name	Reset status
0x00 7F00	CPU	A	Accumulator	0x00
0x00 7F01		PCE	Program counter extended	0x00
0x00 7F02		PCH	Program counter high	0x80
0x00 7F03		PCL	Program counter low	0x00
0x00 7F04		XH	X index register high	0x00
0x00 7F05		XL	X index register low	0x00
0x00 7F06		YH	Y index register high	0x00
0x00 7F07		YL	Y index register low	0x00
0x00 7F08		SPH	Stack pointer high	0x05
0x00 7F09		SPL	Stack pointer low	0xFF
0x00 7F0A		CC	Condition code register	0x28

6 Interrupt vector mapping

Table 9. Interrupt mapping

IRQ No.	Source block	Description	Wakeup from Halt mode	Wakeup from Active-halt mode	Wakeup from Wait (WFI mode)	Wakeup from Wait (WFE mode)(1)	Vector address
	RESET	Reset	Yes	Yes	Yes	Yes	0x00 8000
	TRAP	Software interrupt	-	-	-	-	0x00 8004
0	Reserved						0x00 8008
1	FLASH	FLASH end of programing/ write attempted to protected page interrupt	-	-	Yes	Yes	0x00 800C
2	PXS	End of conversion/First conversion completed	-	Yes(2)	Yes	Yes	0x00 8010
3	Reserved						0x00 8011 -0x00 8017
4	AWU	Auto wakeup from Halt	-	Yes	Yes	Yes	0x00 8018
5	Reserved						0x00 801C
6	EXTIB	External interrupt port B	Yes	Yes	Yes	Yes	0x00 8020
7	EXTID	External interrupt port D	Yes	Yes	Yes	Yes	0x00 8024
8	EXTI0	External interrupt 0	Yes	Yes	Yes	Yes	0x00 8028
9	EXTI1	External interrupt 1	Yes	Yes	Yes	Yes	0x00 802C
10	EXTI2	External interrupt 2	Yes	Yes	Yes	Yes	0x00 8030
11	EXTI3	External interrupt 3	Yes	Yes	Yes	Yes	0x00 8034
12	EXTI4	External interrupt 4	Yes	Yes	Yes	Yes	0x00 8038
13	EXTI5	External interrupt 5	Yes	Yes	Yes	Yes	0x00 803C
14	EXTI6	External interrupt 6	Yes	Yes	Yes	Yes	0x00 8040
15	EXTI7	External interrupt 7	Yes	Yes	Yes	Yes	0x00 8044
16	Reserved						0x00 8048
17	Reserved						0x00 804C -0x00 804F
18	Reserved						0x00 8050
19	TIM2	TIM2 update/overflow/ trigger/break interrupt	-	-	Yes	Yes	0x00 8054
20	TIM2	TIM2 capture/compare interrupt	-	-	Yes	Yes	0x00 8058
21	TIM3	TIM3 update/overflow/ trigger/break interrupt	-	-	Yes	Yes	0x00 805C

Table 9. Interrupt mapping (continued)

IRQ No.	Source block	Description	Wakeup from Halt mode	Wakeup from Active-halt mode	Wakeup from Wait (WFI mode)	Wakeup from Wait (WFE mode)(1)	Vector address
22	TIM3	TIM3 capture/compare interrupt	-	-	Yes	Yes	0x00 8060
23-24	Reserved						0x00 8064-0x00 806B
25	TIM4	TIM4 update/overflow/ trigger interrupt	-	-	Yes	Yes	0x00 806C
26	SPI	SPI TX buffer empty/ RX buffer not empty/ error/wakeup interrupt	Yes	Yes	Yes	Yes	0x00 8070
27	USART	USART transmit data register empty/ transmission complete interrupt	-	-	Yes	Yes	0x00 8074
28	USART	USART received data ready/overrun error/ idle line detected/parity error/global error interrupt	-	-	Yes	Yes	0x00 8078
29	I2C	I2C interrupt(3)	Yes	Yes	Yes	Yes	0x00 807C

1. The Low power wait mode is entered when executing a WFE instruction in Low power run mode. In WFE mode, the interrupt is served if it has been previously enabled. After processing the interrupt, the processor goes back to WFE mode. When the interrupt is configured as a wakeup event, the CPU wakes up and resumes processing.
2. ProxSense activated before executing HALT instruction.
3. The device is woken up from Halt or Active-halt mode only when the address received matches the interface address.

8 Unique ID

STM8TL5xx4 devices feature a 96-bit unique device identifier which provides a reference number that is unique for any device and in any context. The 96 bits of the identifier can never be altered by the user.

The unique device identifier can be read in single byte and may then be concatenated using a custom algorithm.

The unique device identifier is ideally suited:

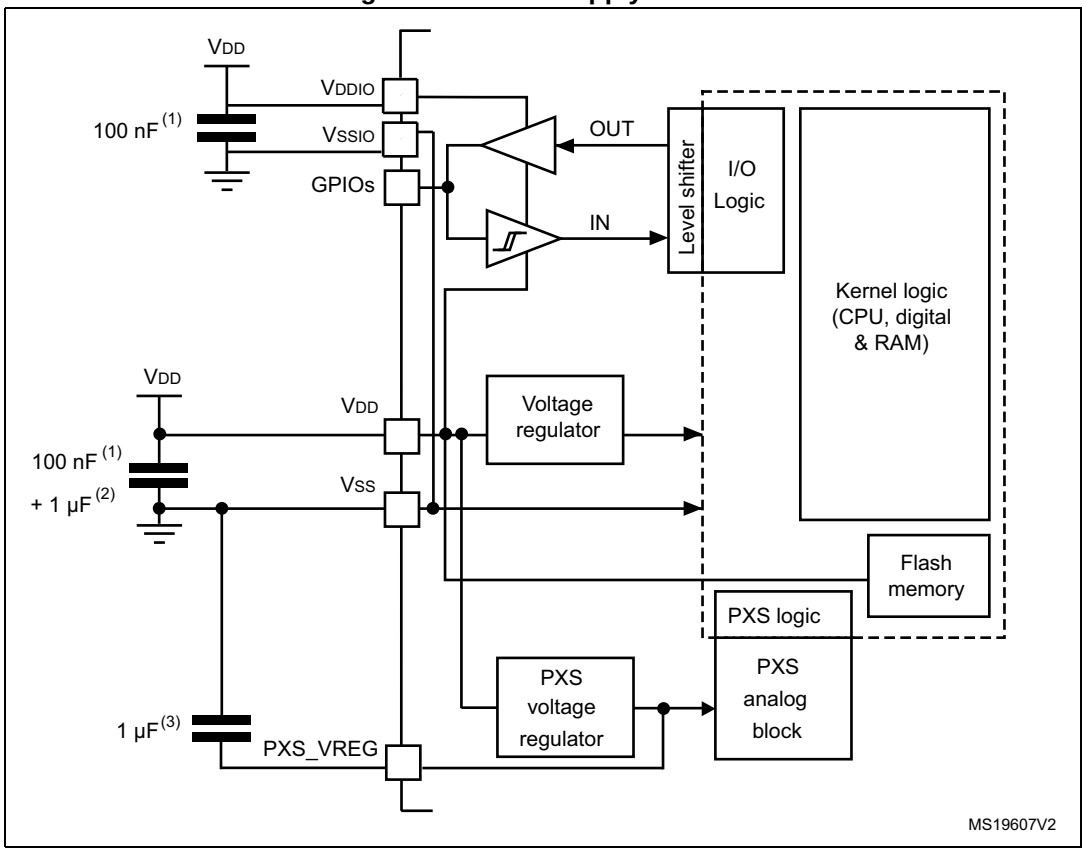
- For use as serial numbers
- For use as security keys to increase the code security in the program memory while using and combining this unique ID with software cryptographic primitives and protocols before programming the internal memory
- To activate secure boot processes

Table 12. Unique ID registers (96 bits)

Address	Content description	Unique ID bits							
		7	6	5	4	3	2	1	0
0x4925	X coordinate on the wafer	U_ID[7:0]							
0x4926		U_ID[15:8]							
0x4927	Y coordinate on the wafer	U_ID[23:16]							
0x4928		U_ID[31:24]							
0x4929	Wafer number	U_ID[39:32]							
0x492A	Lot number	U_ID[47:40]							
0x492B		U_ID[55:48]							
0x492C		U_ID[63:56]							
0x492D		U_ID[71:64]							
0x492E		U_ID[79:72]							
0x492F		U_ID[87:80]							
0x4930		U_ID[95:88]							

9.3.2 Power supply

Figure 10. Power supply scheme



1. Each power supply pair must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins to ensure the correct functionality of the device.
2. The 1µF capacitor must be connected to the V_{DD} pin.
3. The 1µF ceramic capacitor connected to PXS_VREG must be low ESR (ESR ≤ 1Ω).

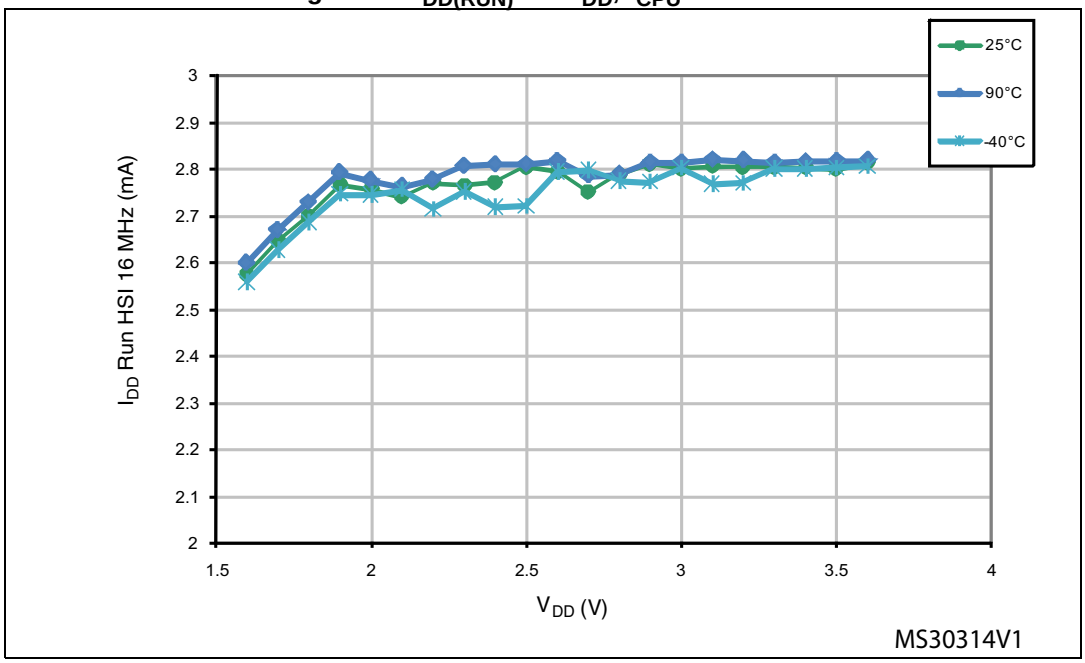
9.3.3 Power-up / power-down operating conditions

Table 17. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{VDD}	V_{DD} rise time rate		20	-	1300	µs/V
t_{TEMP}	Reset release delay	V_{DD} rising	-	1	-	ms
V_{POR}	Power on reset threshold		1.44(2)	-	1.65(1)	V
V_{PDR}	Power down reset threshold		1.30(2)	-	1.60(2)	V

1. Tested in production.
2. Data based on characterization results, not tested in production.

Figure 11. $I_{DD(RUN)}$ vs. V_{DD}, f_{CPU} = 16 MHz



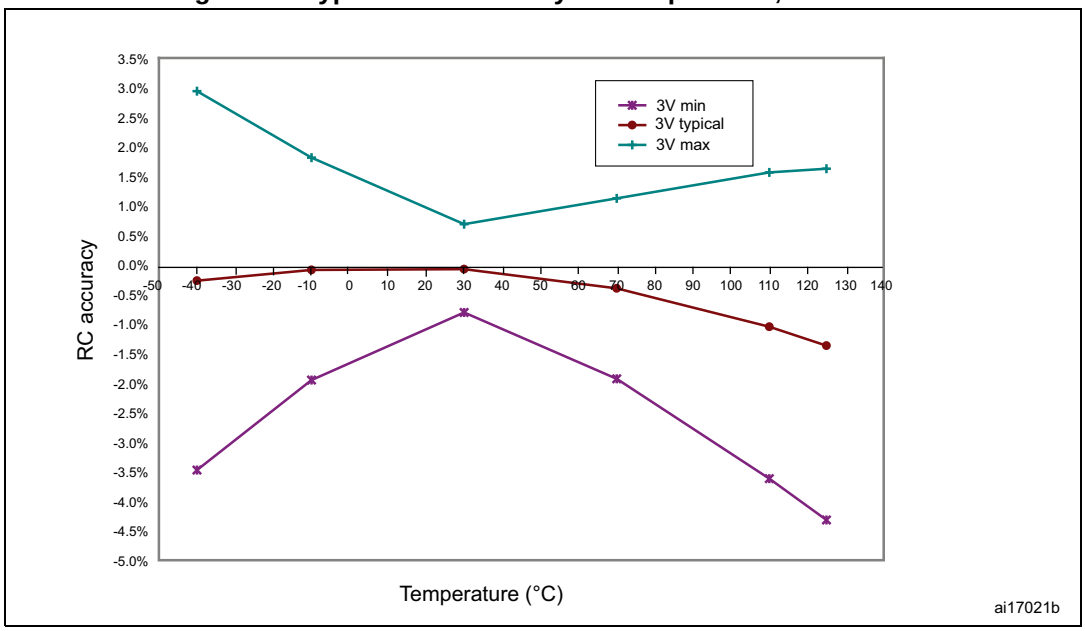
1. Typical current consumption measured with code executed from Flash.

Table 20. Total current consumption in Wait mode(1)

Symbol	Parameter	Conditions		Typ.	Max.(2)	Unit
$I_{DD(Wait)}$	Supply current in Wait mode	CPU not clocked, all peripherals off, HSI internal RC osc	f_{MASTER} = 2 MHz	260	400	µA
			f_{MASTER} = 4 MHz	300	450	
			f_{MASTER} = 8 MHz	380	600	
			f_{MASTER} = 16 MHz	500	800	

1. Based on characterization results, unless otherwise specified.
2. Maximum values are given for T_A = –40 to 85 °C.

Figure 15. Typical HSI accuracy vs. temperature, VDD = 3 V



High speed ProxSense RC oscillator

Table 25. HSI_PXS oscillator characteristics(1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{HSI_PXS}	Frequency	V_{DD} = 3.0 V	-	16	-	MHz

1. V_{DD} = 3V, T_A = –40 to 85 °C, unless otherwise specified.

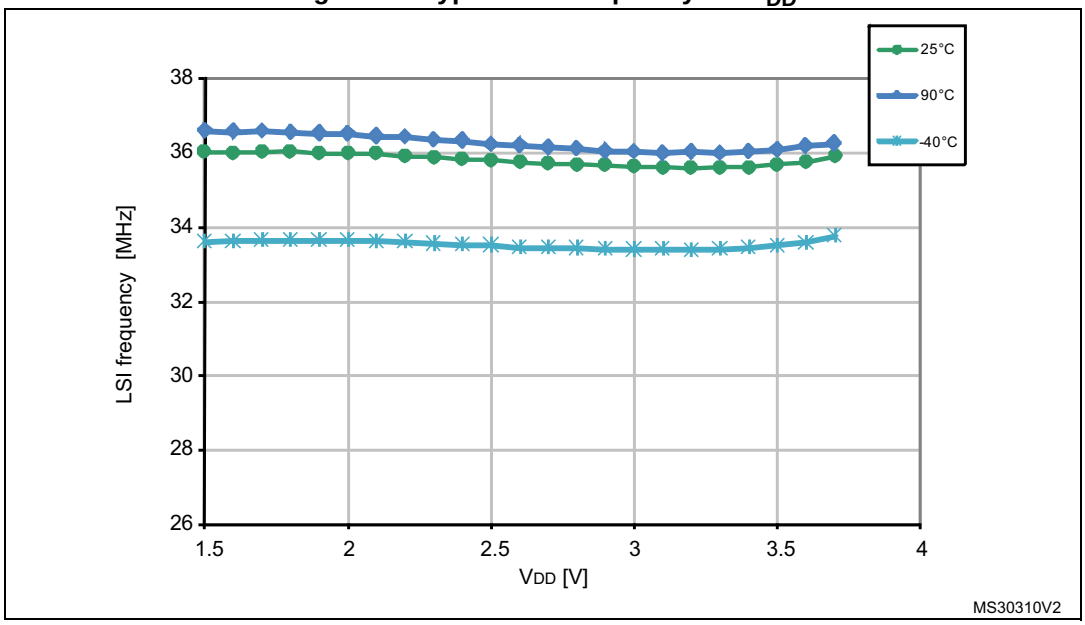
Low speed internal RC oscillator (LSI)

Table 26. LSI oscillator characteristics (1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{LSI}	Frequency		26	38	56	kHz
$f_{drift(LSI)}$	LSI oscillator frequency drift(2)	0 °C ≤ T_A ≤ 85°C	–12	-	11	%

1. V_{DD} = 1.65 V to 3.6 V, T_A = –40 to 85°C unless otherwise specified.
2. For each individual part, this value is the frequency drift from the initial measured frequency.

Figure 16. Typical LSI frequency vs. V_{DD}



9.3.7 Memory characteristics

T_A = –40 to 85°C unless otherwise specified.

RAM characteristics

Table 27. RAM and hardware registers

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{RM}	Data retention mode (1)	Halt mode (or Reset)	1.4	-	-	V

1. Minimum supply voltage without losing data stored in RAM (in Halt mode or under Reset) or in hardware registers (only in Halt mode). Guaranteed by characterization, not tested in production.

Flash memory characteristics

Table 28. Flash program memory

Symbol	Parameter	Conditions	Min.	Typ.	Max.(1)	Unit
V_{DD}	Operating voltage (all modes, read/write/erase)	f_{MASTER} = 16 MHz	1.65	-	3.6	V
t_{prog}	Programming time for 1 or 64 byte (block) erase/write cycles (on programmed byte)		-	6	-	ms
	Programming time for 1 to 64 byte (block) write cycles (on erased byte)		-	3	-	ms
I_{prog}	Programming/ erasing consumption	T_A=+25 °C, V_{DD} = 3.0 V	-	0.7	-	mA
		T_A=+25 °C, V_{DD} = 1.8 V	-		-	

1. Data based on characterization results, not tested in production.

NRST pin

The NRST pin input driver is CMOS. A permanent pull-up is present which is the same as R_{PU} (see *Table 31 on page 56*).

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

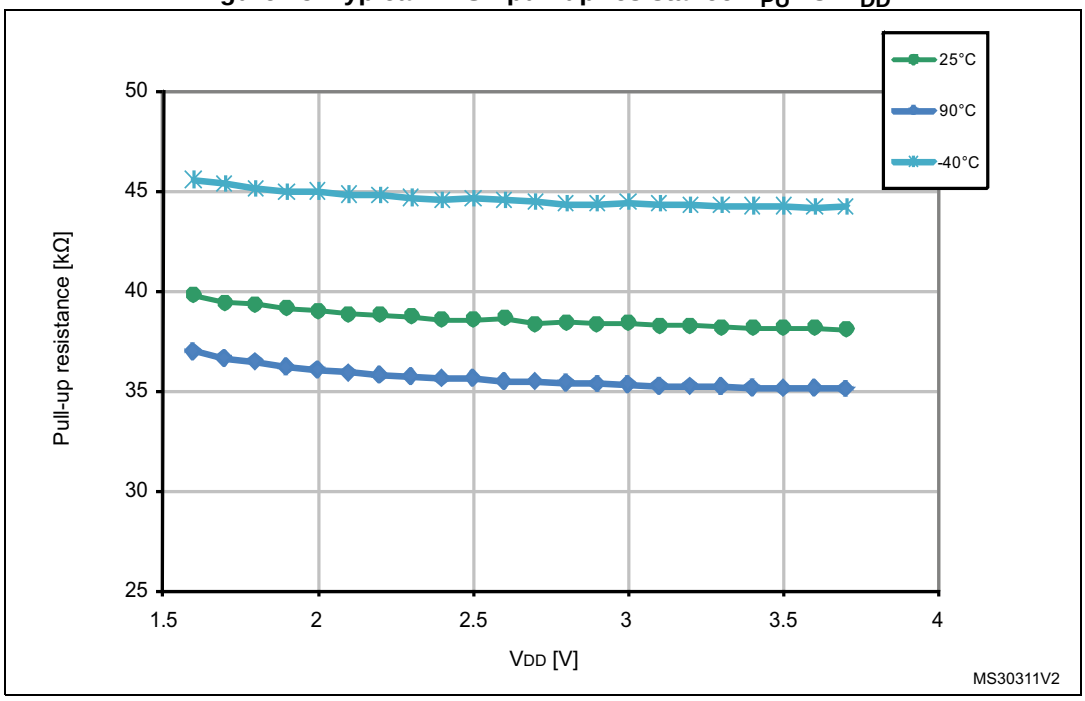
Table 33. NRST pin characteristics

Symbol	Parameter	Conditions	Min.	Typ.(1)	Max.	Unit
$V_{IL(NRST)}$	NRST input low level voltage(1)	-	V_{SS}	-	0.8	V
$V_{IH(NRST)}$	NRST input high level voltage(1)	-	1.4	-	V_{DD}	
$V_{OL(NRST)}$	NRST output low level voltage	I_{OL} = 2 mA	-	-	V_{DD}-0.8	
$R_{PU(NRST)}$	NRST pull-up equivalent resistor(2)	-	30	45	60	kΩ
$V_{F(NRST)}$	NRST input filtered pulse(3)	-	-	-	50	ns
$t_{OP(NRST)}$	NRST output pulse width	-	20	-	-	
$V_{NF(NRST)}$	NRST input not filtered pulse(3)	-	300	-	-	

1. Data based on characterization results, not tested in production.
2. The R_{PU} pull-up equivalent resistor is based on a resistive transistor.
3. Data guaranteed by design, not tested in production.

The reset network shown in *Figure 26* protects the device against parasitic resets. The user must ensure that the level on the NRST pin can go below the V_{IL} max. level specified in *Table 33*. Otherwise the reset is not taken into account internally.

Figure 25. Typical NRST pull-up resistance R_{PU} vs. V_{DD}



9.3.9 Communication interfaces

Serial peripheral interface (SPI)

The parameters given in *Table 34* are derived from tests performed under ambient temperature, f_{MASTER} frequency and V_{DD} supply voltage conditions summarized in *Section 9.3.1 on page 45*, unless otherwise specified. Refer to I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 34. SPI characteristics

Symbol	Parameter	Conditions(1)	Min.	Max.	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	0	8	MHz
		Slave mode	0	8	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF	-	30	ns
$t_{su(NSS)}$(2)	NSS setup time	Slave mode	4 x t_{MASTER}	-	
$t_{h(NSS)}$(2)	NSS hold time	Slave mode	80	-	
$t_{w(SCKH)}$(2) $t_{w(SCKL)}$(2)	SCK high and low time	Master mode, f_{MASTER} = 8 MHz, f_{SCK}= 4 MHz	105	145	
$t_{su(MI)}$(2) $t_{su(SI)}$(2)	Data input setup time	Master mode	30	-	
		Slave mode	3	-	
$t_{h(MI)}$(2) $t_{h(SI)}$(2)	Data input hold time	Master mode	15	-	
		Slave mode	0	-	
$t_{a(SO)}$(2)(3)	Data output access time	Slave mode	-	3x t_{MASTER}	
$t_{dis(SO)}$(2)(4)	Data output disable time	Slave mode	30	-	
$t_{v(SO)}$(2)	Data output valid time	Slave mode (after enable edge)	-	60	
$t_{v(MO)}$(2)	Data output valid time	Master mode (after enable edge)	-	20	
$t_{h(SO)}$(2)	Data output hold time	Slave mode (after enable edge)	15	-	
$t_{h(MO)}$(2)		Master mode (after enable edge)	1	-	

1. Parameters are given by selecting 10–MHz I/O output frequency.
2. Values based on design simulation and/or characterization results, and not tested in production.
3. Min time is for the minimum time to drive the output and max time is for the maximum time to validate the data.
4. Min time is for the minimum time to invalidate the output and max time is for the maximum time to put the data in Hi–Z.

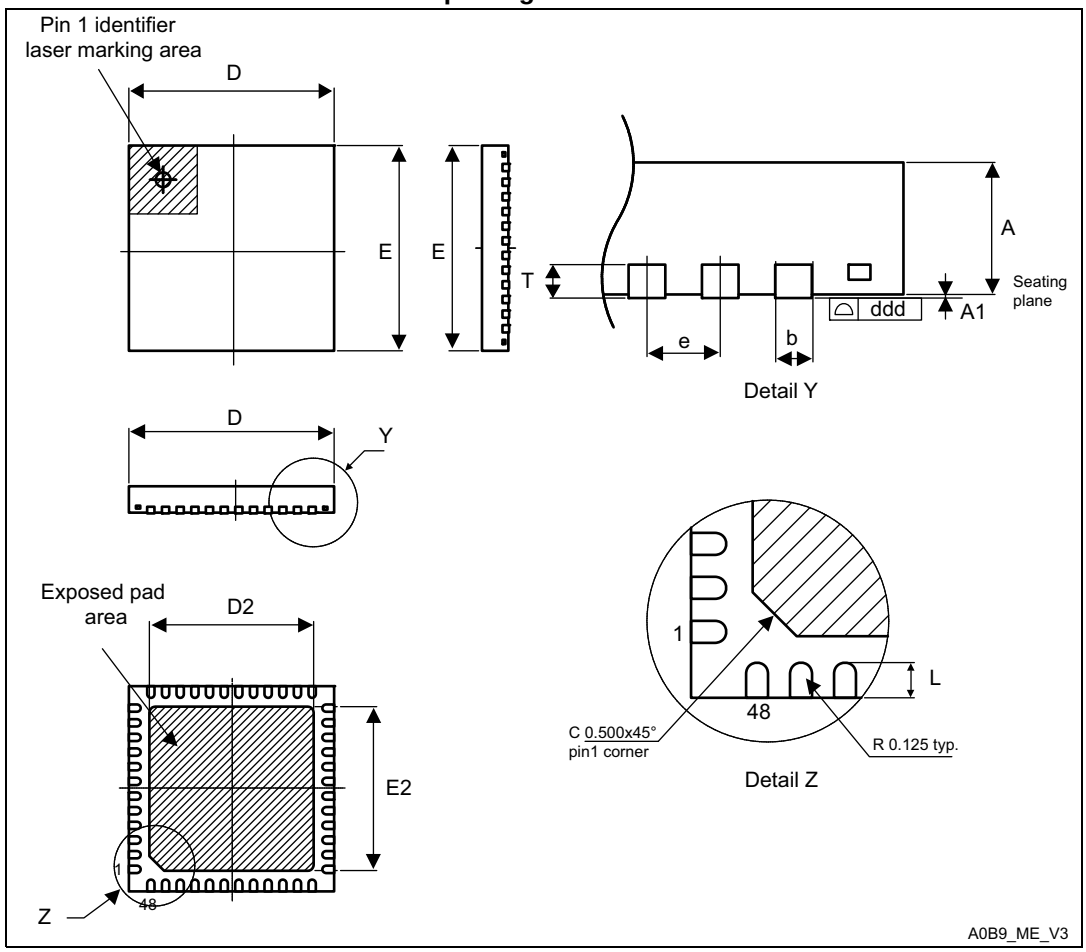
10 Package information

10.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at:*www.st.com*. ECOPACK® is an ST trademark.

10.2 UFQFPN48 package information

Figure 31. UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline

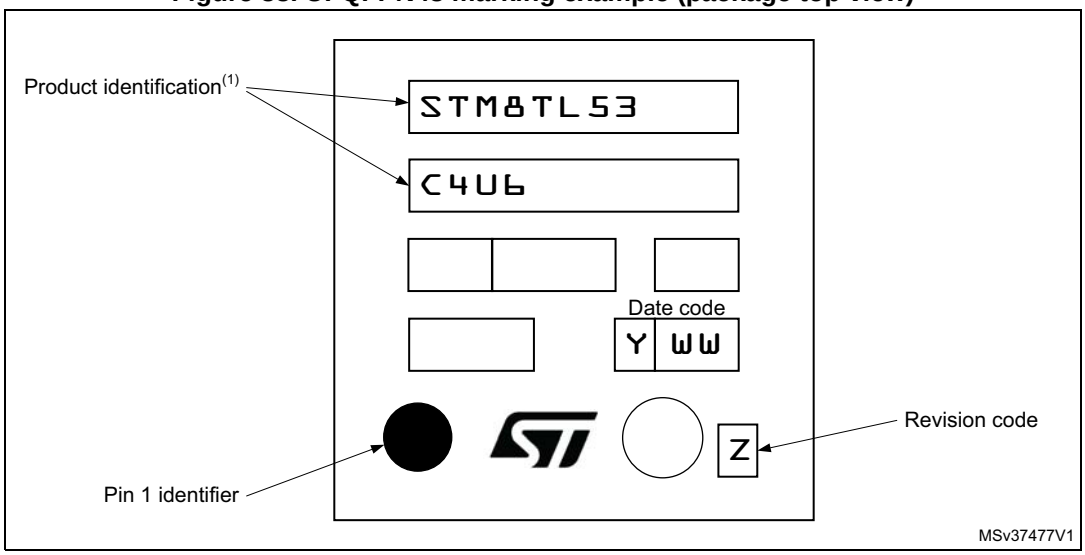


1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this back-side pad to PCB ground.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 33. UFQFPN48 marking example (package top view)



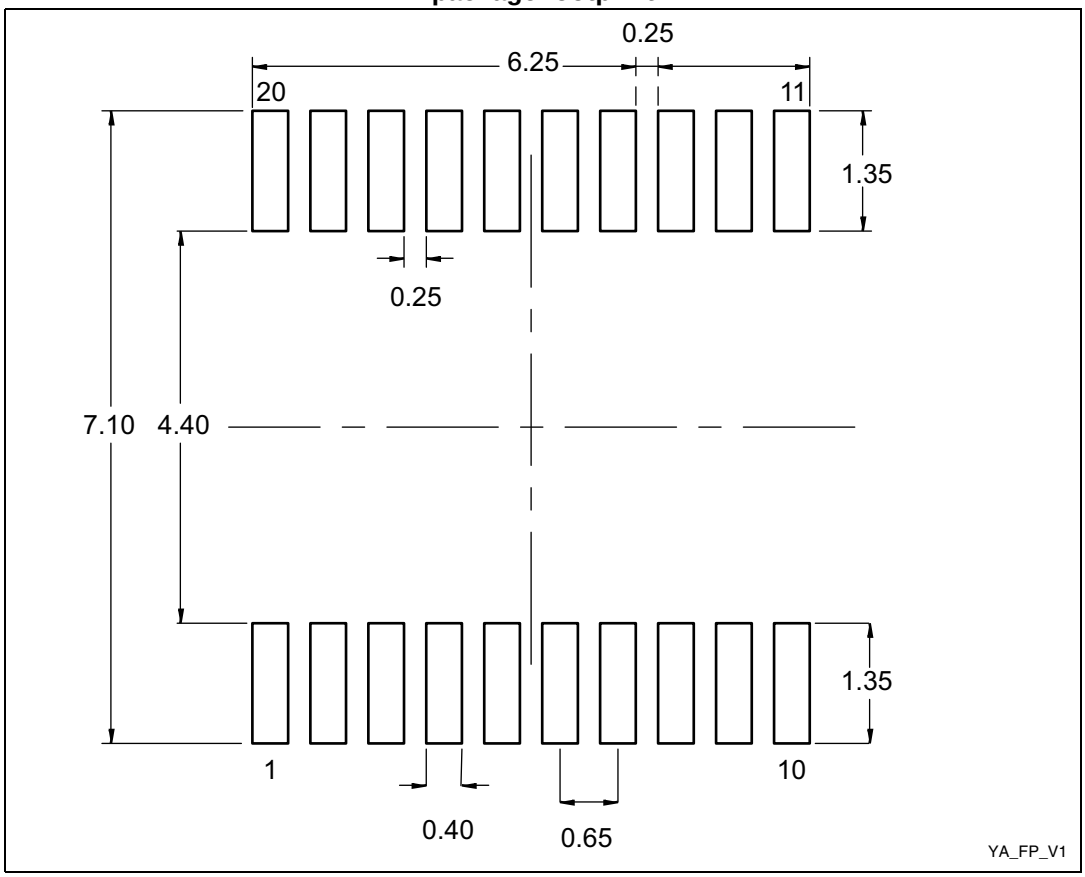
1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 43. TSSOP20 – 20-lead thin shrink small outline, 6.5 x 4.4 mm, 0.65 mm pitch, package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	-	8°	0°	-	8°
aaa	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to four decimal digits.
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
3. Dimension “E1” does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25mm per side.

Figure 38. TSSOP20 – 20-lead thin shrink small outline, 6.5 x 4.4 mm, 0.65 mm pitch, package footprint



1. Dimensions are expressed in millimeters.

12.1.2 STM-STUDIO

STM-STUDIO helps debug and diagnose STM8 and STM32 applications while they are running by reading and displaying their variables in real-time. STM-STUDIO perfectly complements traditional debugging tools to fine tune applications. It is well suited for debugging applications which cannot be stopped, such as TouchSensing applications. Its easy-to-use, graphical interface features:

- Non-intrusive read on-the-fly variables from RAM while the application is running
- Parse DWARF debugging information in the ELF application executable file
- Possibility to log data into a file, and replay later (exhaustive record display, not real-time)
- 2 types of viewers:
  - Variable viewer: Real-time waveforms, oscilloscope-like graphs
  - TouchPoint viewer: Association of 2 variables, one on the X axis, one on the Y axis

12.1.3 C and assembly toolchains

Control of C and assembly toolchains is seamlessly integrated into the STVD integrated development environment, making it possible to configure and control the building of your application directly from an easy-to-use graphical interface.

Available toolchains include:

- ***Cosmic C compiler for STM8*** – One free version that outputs up to 32 Kbytes of code is available. For more information, see www.cosmic-software.com.
- ***IAR embedded workbench*** – The C compiler for STM8 which is included in the toolset is free for up to 8Kbytes of code. For more information, see www.iar.com.
- ***Raisonance C compiler for STM8*** – One free version that outputs up to 32 Kbytes of code. For more information, see www.raisonance.com.
- ***STM8 assembler linker*** – Free assembly toolchain included in the STVD toolset, which allows you to assemble and link your application source code.

12.2 Programming tools

During the development cycle, ST-Link provides in-circuit programming of the STM8 Flash microcontroller on your application board via the SWIM protocol.

For production environments, programmers will include a complete range of gang and automated programming solutions from third-party tool developers already supplying programmers for the STM8 family.