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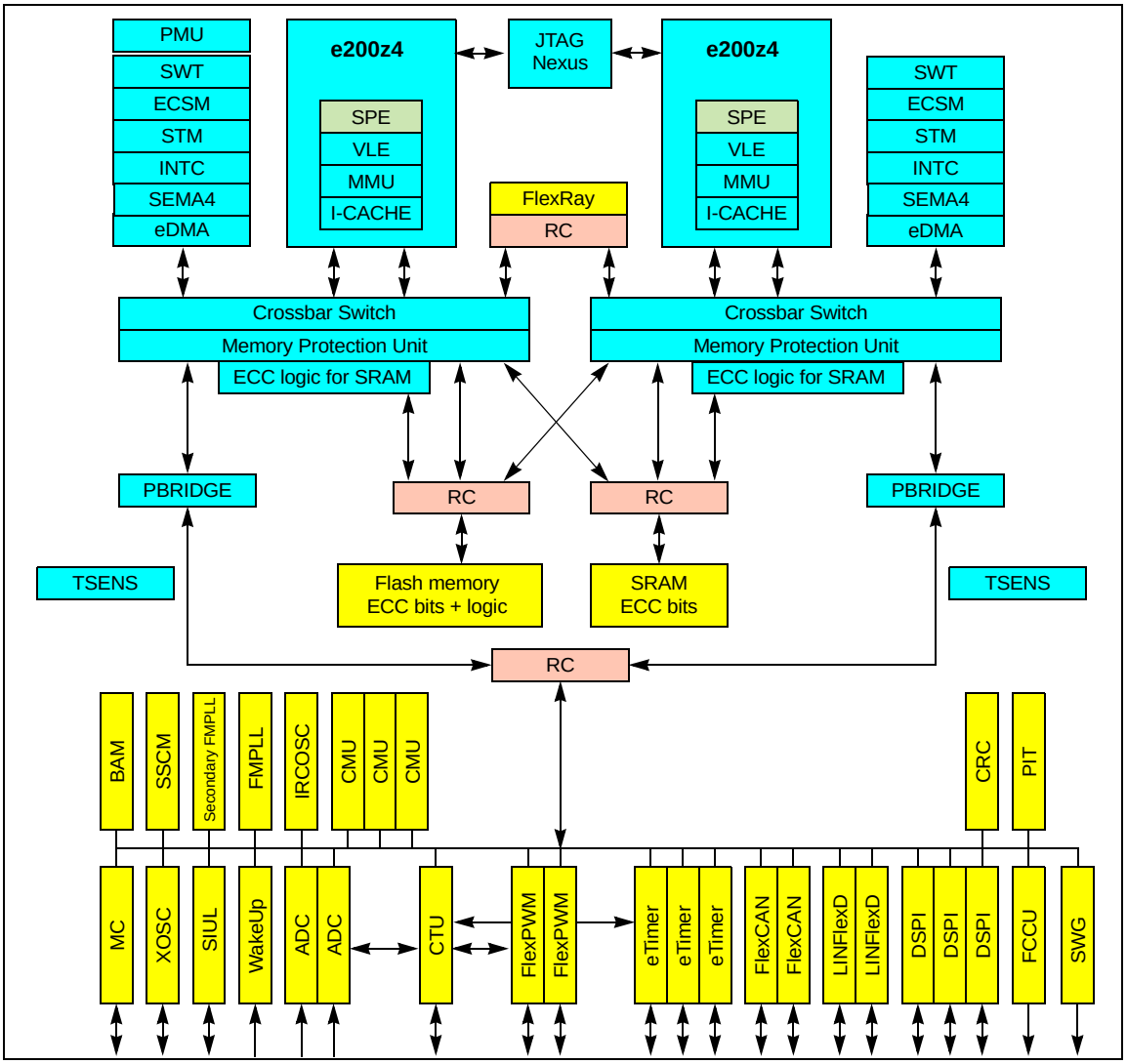
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	e200z4
Core Size	32-Bit Dual-Core
Speed	80MHz
Connectivity	CANbus, FlexRay, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	-
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5643lf0mlq8



ADC – Analog-to-Digital Converter
BAM – Boot Assist Module
CMU – Clock Monitoring Unit
CRC – Cyclic Redundancy Check unit
CTU – Cross Triggering Unit
DSPI – Serial Peripherals Interface
ECC – Error Correction Code
ECSM – Error Correction Status Module
eDMA – Enhanced Direct Memory Access controller
FCCU – Fault Collection and Control Unit
FlexCAN – Controller Area Network controller
FMPLL – Frequency Modulated Phase Locked Loop
INTC – Interrupt Controller
IRCOSC – Internal RC Oscillator
JTAG – Joint Test Action Group interface
LINFlexD – LIN controller with DMA support
MC – Mode Entry, Clock, Reset, & Power
PBRIDGE – Peripheral bridge
PIT – Periodic Interrupt Timer
PMU – Power Management Unit
RC – Redundancy Checker
RTC – Real Time Clock
SEMA4 – Semaphore Unit
SIUL – System Integration Unit Lite
SSCM – System Status and Configuration Module
STM – System Timer Module
SWG – Sine Wave Generator
SWT – Software Watchdog Timer
TSENS – Temperature Sensor
XOSC – Crystal Oscillator

Figure 1. MPC5643L block diagram

1.5.2 Crossbar switch (XBAR)

The XBAR multi-port crossbar switch supports simultaneous connections between four master ports and three slave ports. The crossbar supports a 32-bit address bus width and a 64-bit data bus width.

The crossbar allows four concurrent transactions to occur from any master port to any slave port, although one of those transfers must be an instruction fetch from internal flash memory. If a slave port is simultaneously requested by more than one master port, arbitration logic selects the higher priority master and grants it ownership of the slave port. All other masters requesting that slave port are stalled until the higher priority master completes its transactions.

The crossbar provides the following features:

- 4 masters and 3 slaves supported per each replicated crossbar
  - Masters allocation for each crossbar: e200z4d core with two independent bus interface units (BIU) for I and D access (2 masters), one eDMA, one FlexRay
  - Slaves allocation for each crossbar: a redundant flash-memory controller with 2 slave ports to guarantee maximum flexibility to handle Instruction and Data array, one redundant SRAM controller with 1 slave port each and 1 redundant peripheral bus bridge
- 32-bit address bus and 64-bit data bus
- Programmable arbitration priority
  - Requesting masters can be treated with equal priority and are granted access to a slave port in round-robin method, based upon the ID of the last master to be granted access or a priority order can be assigned by software at application run time
- Temporary dynamic priority elevation of masters

The XBAR is replicated for each processing channel.

1.5.3 Memory Protection Unit (MPU)

The Memory Protection Unit splits the physical memory into 16 different regions. Each master (eDMA, FlexRay, CPU) can be assigned different access rights to each region.

- 16-region MPU with concurrent checks against each master access
- 32-byte granularity for protected address region

The memory protection unit is replicated for each processing channel.

1.5.4 Enhanced Direct Memory Access (eDMA)

The enhanced direct memory access (eDMA) controller is a second-generation module capable of performing complex data movements via 16 programmable channels, with minimal intervention from the host processor. The hardware microarchitecture includes a DMA engine which performs source and destination address calculations, and the actual data movement operations, along with an SRAM-based memory containing the transfer control descriptors (TCD) for the channels. This implementation is used to minimize the overall block size.

The eDMA module provides the following features:

- 16 channels supporting 8-, 16-, and 32-bit value single or block transfers
- Support variable sized queues and circular buffered queue
- Source and destination address registers independently configured to post-increment or stay constant
- Support major and minor loop offset
- Support minor and major loop done signals
- DMA task initiated either by hardware requestor or by software
- Each DMA task can optionally generate an interrupt at completion and retirement of the task
- Signal to indicate closure of last minor loop

- Transfer control descriptors mapped inside the SRAM

The eDMA controller is replicated for each processing channel.

1.5.5 On-chip flash memory with ECC

This device includes programmable, non-volatile flash memory. The non-volatile memory (NVM) can be used for instruction storage or data storage, or both. The flash memory module interfaces with the system bus through a dedicated flash memory array controller. It supports a 64-bit data bus width at the system bus port, and a 128-bit read data interface to flash memory. The module contains four 128-bit prefetch buffers. Prefetch buffer hits allow no-wait responses. Buffer misses incur a 3 wait state response at 120 MHz.

The flash memory module provides the following features

- 1 MB of flash memory in unique multi-partitioned hard macro
- Sectorization: 16 KB + 2 × 48 KB + 16 KB + 2 × 64 KB + 2 × 128 KB + 2 × 256 KB
- EEPROM emulation (in software) within same module but on different partition
- 16 KB test sector and 16 KB shadow block for test, censorship device and user option bits
- Wait states:
  - 3 wait states for frequencies =< 120 MHz
  - 2 wait states for frequencies =< 80 MHz
  - 1 wait state for frequencies =< 60 MHz
- Flash memory line 128-bit wide with 8-bit ECC on 64-bit word (total 144 bits)
- Accessed via a 64-bit wide bus for write and a 128-bit wide array for read operations
- 1-bit error correction, 2-bit error detection

1.5.6 On-chip SRAM with ECC

The MPC5643L SRAM provides a general-purpose single port memory.

ECC handling is done on a 32-bit boundary for data and it is extended to the address to have the highest possible diagnostic coverage including the array internal address decoder.

The SRAM module provides the following features:

- System SRAM: 128 KB
- ECC on 32-bit word (syndrome of 7 bits)
  - ECC covers SRAM bus address
- 1-bit error correction, 2-bit error detection
- Wait states:
  - 1 wait state for frequencies =< 120 MHz
  - 0 wait states for frequencies =< 80 MHz

1.5.7 Platform flash memory controller

The following list summarizes the key features of the flash memory controller:

- Single AHB port interface supports a 64-bit data bus. All AHB aligned and unaligned reads within the 32-bit container are supported. Only aligned word writes are supported.
- Array interfaces support a 128-bit read data bus and a 64-bit write data bus for each bank.
- Code flash (bank0) interface provides configurable read buffering and page prefetch support.
  - Four page-read buffers (each 128 bits wide) and a prefetch controller support speculative reading and optimized flash access.

2 Package pinouts and signal descriptions

2.1 Package pinouts

Figure 2 shows the MPC5643L in the 144 LQFP package.

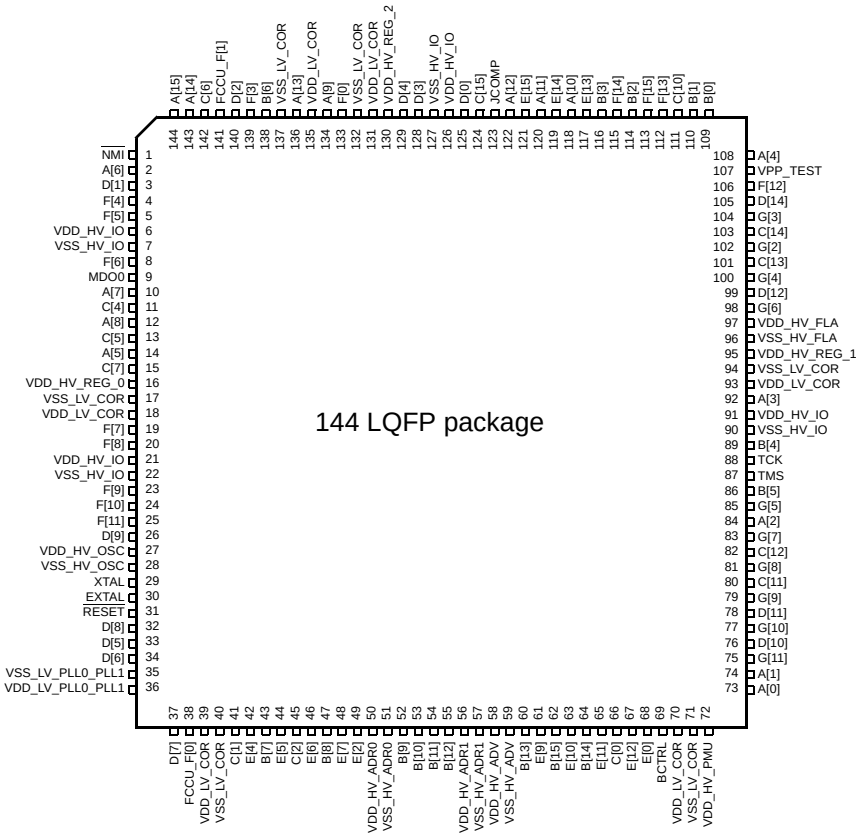


Figure 2. MPC5643L 144 LQFP pinout (top view)

Figure 3 shows the MPC5643L in the 257 MAPBGA package.

Table 3. 144 LQFP pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
64	B[14]	SIUL	—	GPIO[30]
		eTimer_0	—	ETC[4]
		SIUL	—	EIRQ[19]
		ADC_1	—	AN[1]
65	E[11]	SIUL	—	GPIO[75]
		ADC_1	—	AN[4]
66	C[0]	SIUL	—	GPIO[32]
		ADC_1	—	AN[3]
67	E[12]	SIUL	—	GPIO[76]
		ADC_1	—	AN[6]
68	E[0]	SIUL	—	GPIO[64]
		ADC_1	—	AN[5]
69	BCTRL	—		
70	$V_{DD\_LV\_COR}$	—		
71	$V_{SS\_LV\_COR}$	—		
72	$V_{DD\_HV\_PMU}$	—		
73	A[0]	SIUL	GPIO[0]	GPIO[0]
		eTimer_0	ETC[0]	ETC[0]
		DSPI_2	SCK	SCK
		SIUL	—	EIRQ[0]
74	A[1]	SIUL	GPIO[1]	GPIO[1]
		eTimer_0	ETC[1]	ETC[1]
		DSPI_2	SOUT	—
		SIUL	—	EIRQ[1]
75	G[11]	SIUL	GPIO[107]	GPIO[107]
		FlexRay	DBG3	—
		FlexPWM_0	—	FAULT[3]
76	D[10]	SIUL	GPIO[58]	GPIO[58]
		FlexPWM_0	A[0]	A[0]
		eTimer_0	—	ETC[0]
77	G[10]	SIUL	GPIO[106]	GPIO[106]
		FlexRay	DBG2	—
		DSPI_2	CS3	—
		FlexPWM_0	—	FAULT[2]

Table 3. 144 LQFP pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
113	F[15]	SIUL	GPIO[95]	GPIO[95]
		LINFlexD_1	—	RXD
114	B[2]	SIUL	GPIO[18]	GPIO[18]
		LINFlexD_0	TXD	—
		SSCM	DEBUG[2]	—
		SIUL	—	EIRQ[17]
115	F[14]	SIUL	GPIO[94]	GPIO[94]
		LINFlexD_1	TXD	—
116	B[3]	SIUL	GPIO[19]	GPIO[19]
		SSCM	DEBUG[3]	—
		LINFlexD_0	—	RXD
117	E[13]	SIUL	GPIO[77]	GPIO[77]
		eTimer_0	ETC[5]	ETC[5]
		DSPI_2	CS3	—
		SIUL	—	EIRQ[25]
118	A[10]	SIUL	GPIO[10]	GPIO[10]
		DSPI_2	CS0	CS0
		FlexPWM_0	B[0]	B[0]
		FlexPWM_0	X[2]	X[2]
		SIUL	—	EIRQ[9]
119	E[14]	SIUL	GPIO[78]	GPIO[78]
		eTimer_1	ETC[5]	ETC[5]
		SIUL	—	EIRQ[26]
120	A[11]	SIUL	GPIO[11]	GPIO[11]
		DSPI_2	SCK	SCK
		FlexPWM_0	A[0]	A[0]
		FlexPWM_0	A[2]	A[2]
		SIUL	—	EIRQ[10]
121	E[15]	SIUL	GPIO[79]	GPIO[79]
		DSPI_0	CS1	—
		SIUL	—	EIRQ[27]

Table 3. 144 LQFP pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
134	A[9]	SIUL	GPIO[9]	GPIO[9]
		DSPI_2	CS1	—
		FlexPWM_0	B[3]	B[3]
		FlexPWM_0	—	FAULT[0]
135	$V_{DD\_LV\_COR}$	—		
136	A[13]	SIUL	GPIO[13]	GPIO[13]
		FlexPWM_0	B[2]	B[2]
		DSPI_2	—	SIN
		FlexPWM_0	—	FAULT[0]
		SIUL	—	EIRQ[12]
137	$V_{SS\_LV\_COR}$	—		
138	B[6]	SIUL	GPIO[22]	GPIO[22]
		MC_CGM	clk_out	—
		DSPI_2	CS2	—
		SIUL	—	EIRQ[18]
139	F[3]	SIUL	GPIO[83]	GPIO[83]
		DSPI_0	CS6	—
140	D[2]	SIUL	GPIO[50]	GPIO[50]
		eTimer_1	ETC[3]	ETC[3]
		FlexPWM_0	X[3]	X[3]
		FlexRay	—	CB_RX
141	FCCU_F[1]	FCCU	F[1]	F[1]
142	C[6]	SIUL	GPIO[38]	GPIO[38]
		DSPI_0	SOUT	—
		FlexPWM_0	B[1]	B[1]
		SSCM	DEBUG[6]	—
		SIUL	—	EIRQ[24]
143	A[14]	SIUL	GPIO[14]	GPIO[14]
		FlexCAN_1	TXD	—
		eTimer_1	ETC[4]	ETC[4]
		SIUL	—	EIRQ[13]

Table 4. 257 MAPBGA pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
C2	Not connected	—		
C3	$V_{SS\_HV\_IO\_RING}$	—		
C4	FCCU_F[1]	FCCU	F[1]	F[1]
C5	D[2]	SIUL	GPIO[50]	GPIO[50]
		eTimer_1	ETC[3]	ETC[3]
		FlexPWM_0	X[3]	X[3]
		FlexRay	—	CB_RX
C6	A[13]	SIUL	GPIO[13]	GPIO[13]
		FlexPWM_0	B[2]	B[2]
		DSPI_2	—	SIN
		FlexPWM_0	—	FAULT[0]
		SIUL	—	EIRQ[12]
C7	$V_{DD\_HV\_REG\_2}$	—		
C8	$V_{DD\_HV\_REG\_2}$	—		
C9	I[0]	SIUL	GPIO[128]	GPIO[128]
		eTimer_2	ETC[0]	ETC[0]
		DSPI_0	CS4	—
		FlexPWM_1	—	FAULT[0]
C10	JCOMP	—	—	JCOMP
C11	H[11]	SIUL	GPIO[123]	GPIO[123]
		FlexPWM_1	A[2]	A[2]
C12	I[1]	SIUL	GPIO[129]	GPIO[129]
		eTimer_2	ETC[1]	ETC[1]
		DSPI_0	CS5	—
		FlexPWM_1	—	FAULT[1]
C13	F[14]	SIUL	GPIO[94]	GPIO[94]
		LINFlexD_1	TXD	—
C14	B[1]	SIUL	GPIO[17]	GPIO[17]
		eTimer_1	ETC[3]	ETC[3]
		SSCM	DEBUG[1]	—
		FlexCAN_0	—	RXD
		FlexCAN_1	—	RXD
		SIUL	—	EIRQ[16]
C15	$V_{SS\_HV\_IO\_RING}$	—		

Table 4. 257 MAPBGA pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
H3	C[4]	SIUL	GPIO[36]	GPIO[36]
		DSPI_0	CS0	CS0
		FlexPWM_0	X[1]	X[1]
		SSCM	DEBUG[4]	—
		SIUL	—	EIRQ[22]
H4	A[5]	SIUL	GPIO[5]	GPIO[5]
		DSPI_1	CS0	CS0
		eTimer_1	ETC[5]	ETC[5]
		DSPI_0	CS7	—
		SIUL	—	EIRQ[5]
H6	V_{DD_LV}	—		
H7	V_{SS_LV}	—		
H8	V_{SS_LV}	—		
H9	V_{SS_LV}	—		
H10	V_{SS_LV}	—		
H11	V_{SS_LV}	—		
H12	V_{DD_LV}	—		
H14	V_{SS_LV}	—		
H15	$V_{DD\_HV\_REG\_1}$	—		
H16	$V_{DD\_HV\_FLA}$	—		
H17	H[6]	SIUL	GPIO[118]	GPIO[118]
		FlexPWM_1	B[0]	B[0]
		DSPI_0	CS5	—
J1	F[7]	SIUL	GPIO[87]	GPIO[87]
		NPC	MCKO	—
J2	G[15]	SIUL	GPIO[111]	GPIO[111]
		NPC	MDO[8]	—
J3	$V_{DD\_HV\_REG\_0}$	—		
J4	$V_{DD\_HV\_REG\_0}$	—		
J6	V_{DD_LV}	—		
J7	V_{SS_LV}	—		
J8	V_{SS_LV}	—		
J9	V_{SS_LV}	—		
J10	V_{SS_LV}	—		
J11	V_{SS_LV}	—		

Table 5. Supply pins (continued)

Supply			Pin #	
Symbol	**Description**		**144 pkg**	**257 pkg**
$V_{SS\_LV\_COR}$	VSS_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.		17	VSS_HV[2]
$V_{DD\_LV\_COR}$	VDD_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR}$ pin.		18	VDD_LV[1]
V_{SS} 1V2	VSS_LV_PLL0_PLL1 / 1.2 V Decoupling pins for on-chip FMPLL modules. Decoupling capacitor must be connected between this pin and $V_{DD\_LV\_PLL}$.		35	N4
V_{DD} 1V2	VDD_LV_PLL0_PLL1 Decoupling pins for on-chip FMPLL modules. Decoupling capacitor must be connected between this pin and $V_{SS\_LV\_PLL}$.		36	P4
$V_{DD\_LV\_COR}$	VDD_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR}$ pin.		39	VDD_LV[1]
$V_{SS\_LV\_COR}$	VSS_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.		40	VSS_LV[2]
$V_{DD\_LV\_COR}$	VDD_LV_COR Decoupling pins for core logic and Regulator feedback. Decoupling capacitor must be connected between this pins and $V_{SS\_LV\_REGCOR}$.		70	VDD_LV[1]
$V_{SS\_LV\_COR}$	VSS_LV_REGCOR0 Decoupling pins for core logic and Regulator feedback. Decoupling capacitor must be connected between this pins and $V_{DD\_LV\_REGCOR}$.		71	VSS_LV[2]
$V_{DD\_LV\_COR}$	VDD_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR}$ pin.		93	VDD_LV[1]
$V_{SS\_LV\_COR}$	VSS_LV_COR / 1.2 V Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.		94	VSS_LV[2]
V_{DD} 1V2	VDD_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.		131	VDD_LV[1]
V_{SS} 1V2	VSS_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.		132	VSS_LV[2]
V_{DD} 1V2	VDD_LV_COR / Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.		135	VDD_LV[1]
V_{SS} 1V2	VSS_LV_COR / Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.		137	VSS_LV[2]

[1] VDD_LV balls are tied together on the 257 MAPBGA substrate.

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed[1]		Pin #		
								SRC = 1	SRC = 0		144 pkg	257 pkg
Port D												
D[0]	PCR[48]	SIUL	GPIO[48]	ALT0	GPIO[48]	—	—	SYM	S		125	B8
		FlexRay	CA_TX	ALT1	—	—						
		eTimer_1	ETC[1]	ALT2	ETC[1]	PSMI[10]; PADSEL=1						
		FlexPWM_0	B[1]	ALT3	B[1]	PSMI[25]; PADSEL=1						
D[1]	PCR[49]	SIUL	GPIO[49]	ALT0	GPIO[49]	—	—	M	S		3	E3
		eTimer_1	ETC[2]	ALT2	ETC[2]	PSMI[11]; PADSEL=2						
		CTU_0	EXT_TGR	ALT3	—	—						
		FlexRay	—	—	CA_RX	—						
D[2]	PCR[50]	SIUL	GPIO[50]	ALT0	GPIO[50]	—	—	M	S		140	C5
		eTimer_1	ETC[3]	ALT2	ETC[3]	PSMI[12]; PADSEL=1						
		FlexPWM_0	X[3]	ALT3	X[3]	PSMI[30]; PADSEL=0						
		FlexRay	—	—	CB_RX	—						
D[3]	PCR[51]	SIUL	GPIO[51]	ALT0	GPIO[51]	—	—	SYM	S		128	A7
		FlexRay	CB_TX	ALT1	—	—						
		eTimer_1	ETC[4]	ALT2	ETC[4]	PSMI[13]; PADSEL=1						
		FlexPWM_0	A[3]	ALT3	A[3]	PSMI[23]; PADSEL=2						

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed[1]		Pin #		
								SRC = 1	SRC = 0		144 pkg	257 pkg
F[11]	PCR[91]	SIUL	GPIO[91]	ALT0	GPIO[91]	—	—	M	S		25	L2
		NPC	—	ALT2	$\overline{\text{EVTI}}$	—						
F[12]	PCR[92]	SIUL	GPIO[92]	ALT0	GPIO[92]	—	—	M	S		106	C17
		eTimer_1	ETC[3]	ALT1	ETC[3]	PSMI[12]; PADSEL=2						
		SIUL	—	—	EIRQ[30]	—						
F[13]	PCR[93]	SIUL	GPIO[93]	ALT0	GPIO[93]	—	—	M	S		112	B14
		eTimer_1	ETC[4]	ALT1	ETC[4]	PSMI[13]; PADSEL=3						
		SIUL	—	—	EIRQ[31]	—						
F[14]	PCR[94]	SIUL	GPIO[94]	ALT0	GPIO[94]	—	—	M	S		115	C13
		LINFlexD_1	TXD	ALT1	—	—						
F[15]	PCR[95]	SIUL	GPIO[95]	ALT0	GPIO[95]	—	—	M	S		113	D13
		LINFlexD_1	—	—	RXD	PSMI[32]; PADSEL=2						
FCCU												
FCCU_F[0]	—	FCCU	F[0]	ALT0	F[0]	—	—	S	S		38	R2
FCCU_F[1]	—	FCCU	F[1]	ALT0	F[1]	—	—	S	S		141	C4
Port G												
G[2]	PCR[98]	SIUL	GPIO[98]	ALT0	GPIO[98]	—	—	M	S		102	E16
		FlexPWM_0	X[2]	ALT1	X[2]	PSMI[29]; PADSEL=1						
		DSPI_1	CS1	ALT2	—	—						

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed[1]		Pin #		
								SRC = 1	SRC = 0		144 pkg	257 pkg
I[1]	PCR[129]	SIUL	GPIO[129]	ALT0	GPIO[129]	—	—	M	S		—	C12
		eTimer_2	ETC[1]	ALT1	ETC[1]	PSMI[40]; PADSEL=1						
		DSPI_0	CS5	ALT2	—	—						
		FlexPWM_1	—	—	FAULT[1]	—						
I[2]	PCR[130]	SIUL	GPIO[130]	ALT0	GPIO[130]	—	—	M	S		—	F16
		eTimer_2	ETC[2]	ALT1	ETC[2]	PSMI[41]; PADSEL=1						
		DSPI_0	CS6	ALT2	—	—						
		FlexPWM_1	—	—	FAULT[2]	—						
I[3]	PCR[131]	SIUL	GPIO[131]	ALT0	GPIO[131]	—	—	M	S		—	E17
		eTimer_2	ETC[3]	ALT1	ETC[3]	PSMI[42]; PADSEL=1						
		DSPI_0	CS7	ALT2	—	—						
		CTU_0	EXT_TGR	ALT3	—	—						
		FlexPWM_1	—	—	FAULT[3]	—						
$\overline{\text{RDY}}$	PCR[132]	SIUL	GPIO[132]	ALT0	GPIO[132]	—	—	F	S		—	K3
		NPC	$\overline{\text{RDY}}$	ALT2	—	—						

1 Programmable via the SRC (Slew Rate Control) bit in the respective Pad Configuration Register; S = Slow, M = Medium, F = Fast, SYM = Symmetric (for FlexRay)

2 The default function of this pin out of reset is ALT1 (TDO).

3 Analog

NOTE

Open Drain can be configured by the PCRn for all pins used as output (except FCCU_F[0] and FCCU_F[1]).

[2] Adjust resistor at bipolar transistor collector for 3.3V to avoid VCE<VCE_{SAT}

The recommended external ballast transistor is the bipolar transistor BCP68 with the gain range of 85 up to 375 (for IC=500mA, VCE=1V) provided by several suppliers. This includes the gain variations BCP68-10, BCP68-16 and BCP68-25.The most important parameters for the interoperability with the integrated voltage regulator are the DC current gain (hFE) and the temperature coefficient of the gain (XTB). While the specified gain range of most BCP68 vendors is the same, there are slight variations in the temperature coefficient parameter. MPC5643L Voltage regulator operation was simulated against the typical variation on temperature coefficient and against the specified gain range to have a robust design.

Table 18. Voltage regulator electrical specifications

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
	C_{ext}	External decoupling/ stability capacitor	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	12	—	40	µF
	SR	Combined ESR of external capacitor	—	1	—	100	mΩ
	SR	Number of pins for external decoupling/ stability capacitor	—	5	—	—	—
C_{V1V2}	SR	Total capacitance on 1.2 V pins	Ceramic capacitors, taking into account tolerance, aging, voltage and temperature variation	300	—	900	nF
t_{SU}		Start-up time after main supply stabilization	C_{load} = 10 µF × 4	—	—	2.5	ms
—		Main High Voltage Power - Low Voltage Detection, upper threshold	—	—	—	2.93	V
—	D	Main supply low voltage detector, lower threshold	—	2.6	—	—	V
—	D	Digital supply high voltage detector upper threshold	Before a destructive reset initialization phase completion	1.355	—	1.495	V
			After a destructive reset initialization phase completion	1.39	—	1.47	
—	D	Digital supply high voltage detector lower threshold	Before a destructive reset initialization phase completion	1.315	—	1.455	V
			After a destructive reset initialization phase completion	1.35	—	1.38	

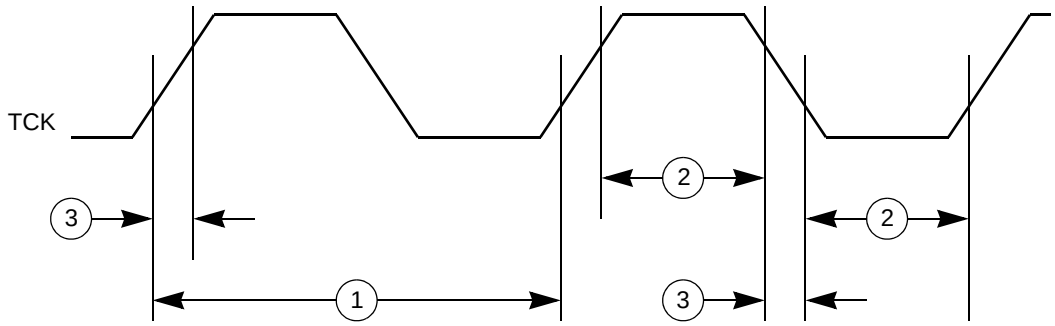


Figure 22. JTAG test clock input timing

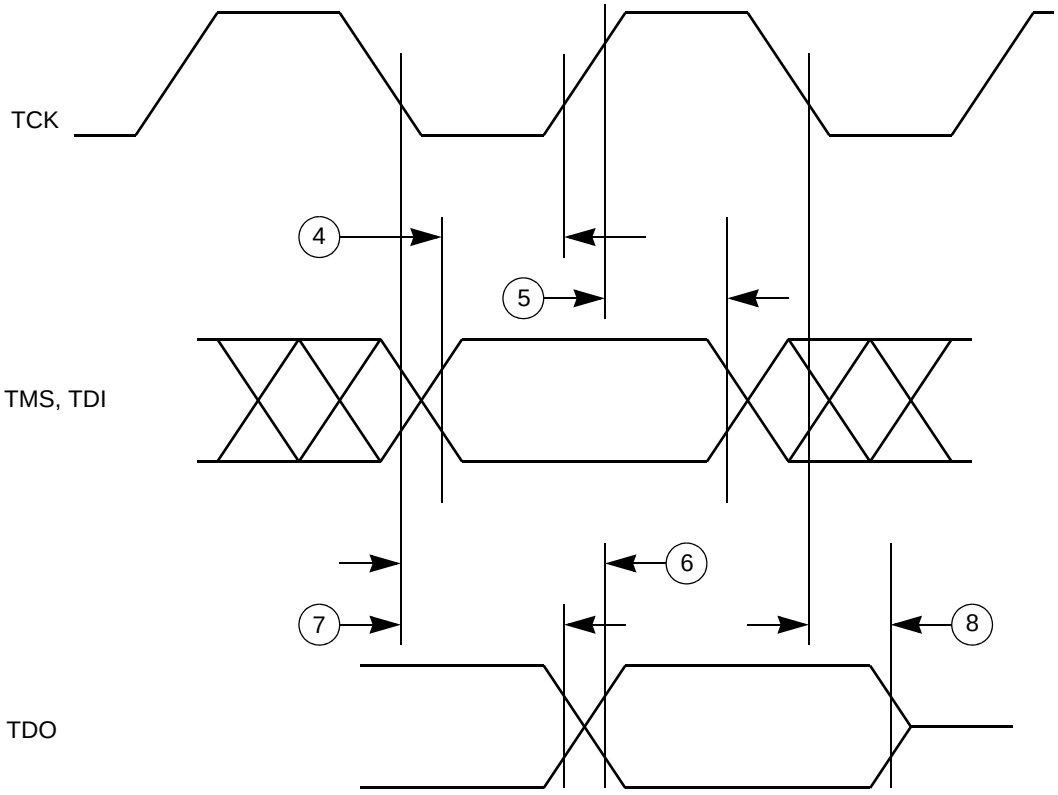
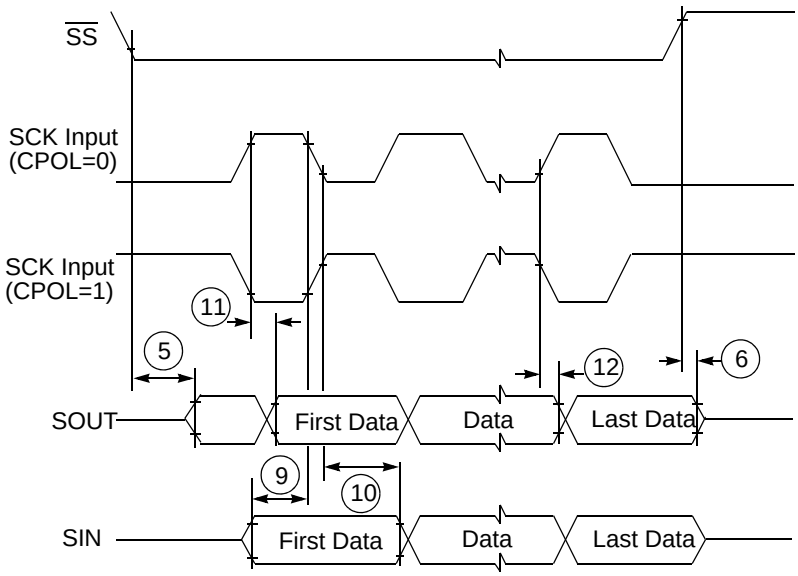
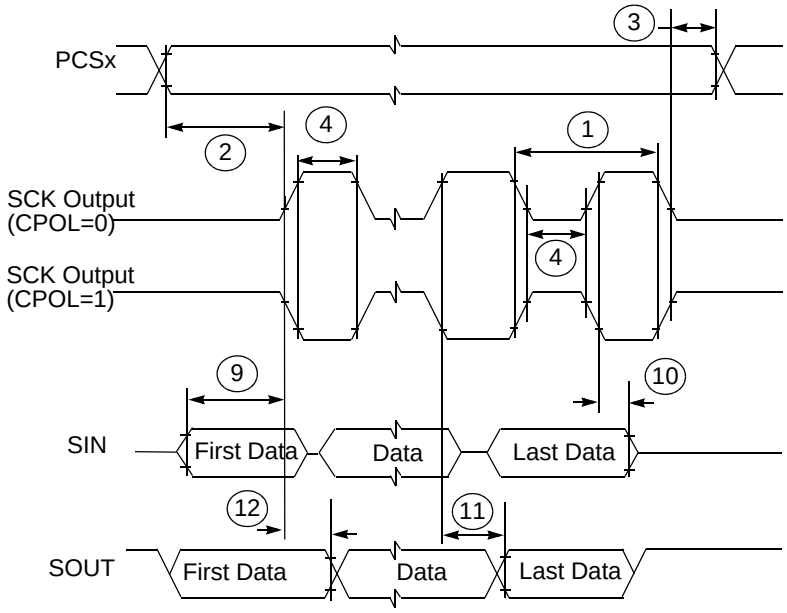


Figure 23. JTAG test access port timing



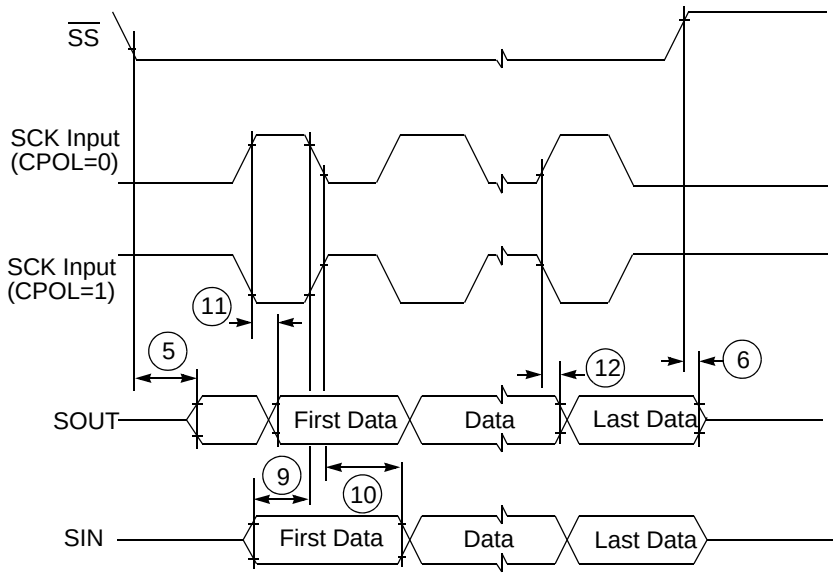
Note: The numbers shown are referenced in Table 39.

Figure 33. DSPI classic SPI timing — slave, CPHA = 1



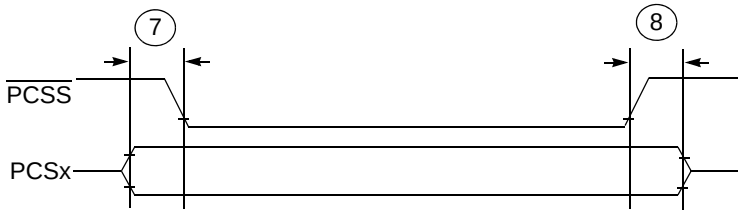
Note: The numbers shown are referenced in Table 39.

Figure 34. DSPI modified transfer format timing — master, CPHA = 0



Note: The numbers shown are referenced in Table 39.

Figure 37. DSPI modified transfer format timing — slave, CPHA = 1



Note: The numbers shown are referenced in Table 39.

Figure 38. DSPI PCS strobe ($\overline{\text{PCSS}}$) timing

4 Package characteristics

4.1 Package mechanical data

Table 41. Revision history (continued)

Revision	Date	Description of changes
5	31 Aug 2010	Editorial changes and improvements. Revised the Overview section. Replaced references to PowerPC with references to Power Architecture. In the feature summary, changed “As much as 128 KB on-chip SRAM” to “128 KB on-chip SRAM”. In the “Feature details” section: • In the “On-chip SRAM with ECC” section, added information about required RAM wait states. • In the PIT section, deleted “32-bit counter for real time interrupt, clocked from main external oscillator” (not supported on this device). • In the flash-memory section, changed “16 KB Test” to “16 KB test sector”, revised the wait state information, and deleted the associated Review_Q&A content. • In the SRAM section, revised the wait state information. In the 144-pin pinout diagram: • Renamed pin 58 (was VDD_HV_ADV0_ADV1, is VDD_HV_ADV). • Renamed pin 59 (was VSS_HV_ADV0_ADV1, is VSS_HV_ADV). In the “144 LQFP pin function summary” table, for pin 39, changed $V_{SS\_LV\_COR}$ to $V_{DD\_LV\_COR}$. In the “Supply pins” table: • Changed the description for $V_{DD\_LV\_COR}$ (was “Voltage regulator supply voltage”, is “Core logic supply”). • Changed the description for $V_{DD\_HV\_PMU}$ (was “Core regulator supply”, is “Voltage regulator supply”). In the “Pin muxing” table: • In the “Pad speed” column headings, changed “SRC = 0” to “SRC = 1” and “SRC = 1” to “SRC = 0” • For port B[6], changed the pad speed for SRC=0 (was M, is F). In the “Thermal characteristics” section, added meaningful values to the thermal-characteristics tables. Added the “SWG electrical specifications” section. In the “Voltage regulator electrical characteristics” section, changed the table title (was “HPREG1, HPREG2, Main LVDs, Digital HVD, and Digital LVD electrical specifications”, is “Voltage regulator electrical characteristics”) and revised the table. In the “BCP68 board schematic example” figure, removed the resistor at the base of the BCP68 transistor. In the “DC electrical characteristics” table: • Changed the guarantee parameter for I_{INJ} (was P, is T). • Added a specification for input leakage current for shared ADC input-only ports. Revised the “Flash memory module life” table. In the “FMPLL electrical characteristics” table, revised the footnote defining f_{SCM} and f_{VCO}. In the “Main oscillator electrical characteristics” table: • Changed the max specification for $g_{mXOSCHS}$ (was 11.8 mA/V, is 13.25 mA/V). • Revised the conditions for $T_{XOSCHSSU}$. In the ‘RC oscillator electrical characteristics” table, deleted the specification for $\Delta_{RCMTRIM}$. Revised the “ADC conversion characteristics” table.
5 (cont.)	31 Aug 2010 (cont.)	In the “$\overline{\text{RESET}}$ pin characteristics” section, changed “n$\overline{\text{RSTIN}}$” to “$\overline{\text{RESET}}$”. Added the “Reset sequence” section. Revised the footnotes in the “Nexus debug port timing” table. In the “Orderable part number summary” table, added a footnote about frequency modulation to the “Speed (MHz)” column heading.

Table 41. Revision history (continued)

Revision	Date	Description of changes
8	27 April 2012	Editorial changes. In the “Device comparison” section, changed “Ambient temperature range using external ballast transistor (BGA)“ from TBD to “–40 to 125 °C“. In the “Block diagram” section, removed one PMU from the figure. In the 257-pin pinout figure, changed cut2 to cut2/3 in Notes. In the pin function summary table, changed cut2 to cut2/3. In the “System pins” table: • Added Note regarding Open Drain Enable. • Added description to RESET pin. In the pin-muxing table: • Added Note about Open Drain. • Changed cut2 to cut2/3. • Changed all entries of column 'Weak pull config during reset’ to ' - ' , except for PCR[2], PCR[3], PCR[4] and PCR[21]. In the “Absolute maximum ratings” table: • Removed the “$V_{SS\_HV\_REG}$” row. • Added the footnote “Internal structures hold the input voltage...” to the V_{IN} maximum specifications. In the “ conditions” table, removed the “$V_{SS\_HV\_REG}$” row. In the “Thermal characteristics” section: • Added the “Thermal characteristics for 100 LQFP package“ table. • Updated values and footnote 1 in the 144 package table. • Updated footnote 1 in the 257 package table. In the “Supply current characteristics“ table: • Added footnote 1 to parameter “$I_{DD\_LV\_TYP}$ + $I_{DD\_LV\_PLL}$“ (symbol “T”). • Changed “$I_{DD\_LV\_STOP}$” at 150C from 80mA to 72mA. • Changed “$I_{DD\_LV\_HALT}$” at 150C from 72mA to 80mA. In the “FMPLL electrical characteristics” table: • Deleted the footnote “This value is true when operating at frequencies above 60 MHz...” from the specification for f_{CS} and f_{DS}. • Changed “f_{SYS}” to “$f_{FMPLLOUT}$” in the entries for the C_{JITTER}, f_{LCK}, f_{UL}, f_{CS}, and f_{DS} specifications. In the “ADC conversion characteristics” table: • Revised the entry for $TUE_{IS1WINJ}$ (was P/T and “Total unadjusted error for IS1WINJ”, is T and “Total unadjusted error for IS1WINJ (single ADC channels)”). • Revised the entry for $TUE_{IS1WWINJ}$ (was “Total unadjusted error for IS1WWINJ”, is “Total unadjusted error for IS1WWINJ (double ADC channels)”). In the “Temperature sensor electrical characteristics“ table, for $T_J = T_A$ to 125 °C, changed Min/Max from values -7/+7 to -10/+10. In the “Input Impedance and ADC Accuracy“ section: • Changed C_S in the text from 3 pF to 7.5 pF. • Changed R_{eq} in the text from 330 kΩ to 133 kΩ. • Removed R_L, R_{SW}, and R_{AD} from the external network design constraint equation and the sentence immediately preceding it. • Changed the C_F constraint value equation constant from 2048 to 8192. • In the “ADC conversion characteristics“ table, changed INL Min/Max values from -2/+2 to -3/+3.

Table 41. Revision history (continued)

Revision	Date	Description of changes
		• Added Table 29 (MPC5643L SWG Specifications) • In Table 29 (MPC5643L SWG Specifications) Added table footnote for Common Mode. Changed text from “internal device pad resistance” to “internal device routing resistance”. • Added Figure 26 in Section 3.20.4, “Nexus timing”. • In Table 30 (Pad AC specifications (3.3 V , IPP_HVE = 0)), removed the row of pad “Pull Up/Downc(3.6 V max)”. • In Table 40 (Orderable part number summary) and Figure 43, updated part numbers (changed ‘PPC’ to ‘SPC’ and ‘F0’ to ‘F2’). • Replaced Figure 39, Figure 40, Figure 41, Figure 42 with the new versions. • InTable 18 (Voltage regulator electrical specifications),changed the symbol of spec external decoupling capacitor from SR to C_{ext}. In Figure 4, changed the ESR range in note text to 1 mW to 100 mW from 30 mW to 150 mW. • In Section 1.5.32, “Sine Wave Generator (SWG)” removed the following text: Frequency range from 1kHz to 50kHz. Sine wave amplitude from 0.47 V to 2.26 V. • In Table 20 (Current consumption characteristics)”,changed symbol from ‘C’ to ‘T’ , added “operating current” to the parameter and updated the maximum value for five additional RunIDD parameters. • In Table 20 (Current consumption characteristics), changed “Conditions” from ‘1.2 V supplies’ to ‘1.2 V supplies during LBIST (full LBIST configuration)’ for all the parameters. • Removed Table “SWG electrical characteristics”. • In Table 18 (Voltage regulator electrical specifications), changed the “Digital supply high voltage detector upper threshold low limit (After a destructive reset initialization phase completion)” from 1.43V to 1.38V. • Added Table 17 (Recommended operating characteristics). • Updated the IDD values in Table 20 (Current consumption characteristics). Changed conditions text from “1.2 supplies during LBIST (full LBIST configuration)” to “1.2 V supplies” for all the IDD parameters except $I_{DD\_LV\_BIST}$+$I_{DD\_LV\_PLL}$. Added footnote in “Conditions” for the DPM mode. • Removed Cut references from the whole document. • In Table 25 (ADC conversion characteristics), changed the sampling frequency value from ‘1 MHz’ to ‘983.6 KHz’.
8.1	07 May 2012	• Deleted the Footer "Preliminary-Subject to Change Without Notice" label.