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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	e200z4
Core Size	32-Bit Dual-Core
Speed	120MHz
Connectivity	CANbus, FlexRay, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	-
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5643lff0mlq1

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1.5.2 Crossbar switch (XBAR)

The XBAR multi-port crossbar switch supports simultaneous connections between four master ports and three slave ports. The crossbar supports a 32-bit address bus width and a 64-bit data bus width.

The crossbar allows four concurrent transactions to occur from any master port to any slave port, although one of those transfers must be an instruction fetch from internal flash memory. If a slave port is simultaneously requested by more than one master port, arbitration logic selects the higher priority master and grants it ownership of the slave port. All other masters requesting that slave port are stalled until the higher priority master completes its transactions.

The crossbar provides the following features:

- 4 masters and 3 slaves supported per each replicated crossbar
  - Masters allocation for each crossbar: e200z4d core with two independent bus interface units (BIU) for I and D access (2 masters), one eDMA, one FlexRay
  - Slaves allocation for each crossbar: a redundant flash-memory controller with 2 slave ports to guarantee maximum flexibility to handle Instruction and Data array, one redundant SRAM controller with 1 slave port each and 1 redundant peripheral bus bridge
- 32-bit address bus and 64-bit data bus
- Programmable arbitration priority
  - Requesting masters can be treated with equal priority and are granted access to a slave port in round-robin method, based upon the ID of the last master to be granted access or a priority order can be assigned by software at application run time
- Temporary dynamic priority elevation of masters

The XBAR is replicated for each processing channel.

1.5.3 Memory Protection Unit (MPU)

The Memory Protection Unit splits the physical memory into 16 different regions. Each master (eDMA, FlexRay, CPU) can be assigned different access rights to each region.

- 16-region MPU with concurrent checks against each master access
- 32-byte granularity for protected address region

The memory protection unit is replicated for each processing channel.

1.5.4 Enhanced Direct Memory Access (eDMA)

The enhanced direct memory access (eDMA) controller is a second-generation module capable of performing complex data movements via 16 programmable channels, with minimal intervention from the host processor. The hardware microarchitecture includes a DMA engine which performs source and destination address calculations, and the actual data movement operations, along with an SRAM-based memory containing the transfer control descriptors (TCD) for the channels. This implementation is used to minimize the overall block size.

The eDMA module provides the following features:

- 16 channels supporting 8-, 16-, and 32-bit value single or block transfers
- Support variable sized queues and circular buffered queue
- Source and destination address registers independently configured to post-increment or stay constant
- Support major and minor loop offset
- Support minor and major loop done signals
- DMA task initiated either by hardware requestor or by software
- Each DMA task can optionally generate an interrupt at completion and retirement of the task
- Signal to indicate closure of last minor loop

- Double buffered PWM registers
  - Integral reload rates from 1 to 16
  - Half cycle reload capability
- Multiple ADC trigger events can be generated per PWM cycle via hardware
- Fault inputs can be assigned to control multiple PWM outputs
- Programmable filters for fault inputs
- Independently programmable PWM output polarity
- Independent top and bottom deadtime insertion
- Each complementary pair can operate with its own PWM frequency and deadtime values
- Individual software control for each PWM output
- All outputs can be forced to a value simultaneously
- PWMX pin can optionally output a third signal from each channel
- Channels not used for PWM generation can be used for buffered output compare functions
- Channels not used for PWM generation can be used for input capture functions
- Enhanced dual edge capture functionality
- Option to supply the source for each complementary PWM signal pair from any of the following:
  - External digital pin
  - Internal timer channel
  - External ADC input, taking into account values set in ADC high- and low-limit registers
- DMA support

1.5.31 eTimer module

The MPC5643L provides three eTimer modules (on the LQFP package eTimer_2 is available internally only without any external I/O access). Six 16-bit general purpose up/down timer/counters per module are implemented with the following features:

- Maximum clock frequency of 120 MHz
- Individual channel capability
  - Input capture trigger
  - Output compare
  - Double buffer (to capture rising edge and falling edge)
  - Separate prescaler for each counter
  - Selectable clock source
  - 0–100% pulse measurement
  - Rotation direction flag (Quad decoder mode)
- Maximum count rate
  - Equals peripheral clock divided by 2 for external event counting
  - Equals peripheral clock for internal clock counting
- Cascadeable counters
- Programmable count modulo
- Quadrature decode capabilities
- Counters can share available input pins
- Count once or repeatedly
- Preloadable counters
- Pins available as GPIO when timer functionality not in use
- DMA support

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	$V_{SS\_HV\_IO}$	$V_{SS\_HV\_IO}$	$V_{DD\_HV\_IO}$	H[2]	H[0]	G[14]	D[3]	C[15]	$V_{DD\_HV\_IO}$	A[12]	H[10]	H[14]	A[10]	B[2]	C[10]	$V_{SS\_HV\_IO}$	$V_{SS\_HV\_IO}$
B	$V_{SS\_HV\_IO}$	$V_{SS\_HV\_IO}$	B[6]	A[14]	F[3]	A[9]	D[4]	D[0]	$V_{SS\_HV\_IO}$	H[12]	E[15]	E[14]	B[3]	F[13]	B[0]	$V_{DD\_HV\_IO}$	$V_{SS\_HV\_IO}$
C	$V_{DD\_HV\_IO}$	NC[1]	$V_{SS\_HV\_IO}$	FCCU_F[1]	D[2]	A[13]	$V_{DD\_HV\_REG\_2}$	$V_{DD\_HV\_REG\_2}$	I[0]	JCOMP	H[11]	I[1]	F[14]	B[1]	$V_{SS\_HV\_IO}$	A[4]	F[12]
D	F[5]	F[4]	A[15]	C[6]	$V_{SS\_LV\_COR}$	$V_{DD\_LV\_COR}$	F[0]	$V_{DD\_HV\_IO}$	$V_{SS\_HV\_IO}$	NC	A[11]	E[13]	F[15]	$V_{DD\_HV\_IO}$	V_{PP_TEST}	D[14]	G[3]
E	MDO0	F[6]	D[1]	NMI										NC	C[14]	G[2]	I[3]
F	H[1]	G[12]	A[7]	A[8]		$V_{DD\_LV\_COR}$	$V_{DD\_LV\_COR}$	$V_{DD\_LV\_COR}$	$V_{DD\_LV\_COR}$	$V_{DD\_LV\_COR}$	$V_{DD\_LV\_COR}$	$V_{DD\_LV\_COR}$		NC	C[13]	I[2]	G[4]
G	H[3]	$V_{DD\_HV\_IO}$	C[5]	A[6]		$V_{DD\_LV\_COR}$	$V_{SS\_LV\_COR}$	$V_{SS\_LV\_COR}$	$V_{SS\_LV\_COR}$	$V_{SS\_LV\_COR}$	$V_{SS\_LV\_COR}$	$V_{DD\_LV\_COR}$		D[12]	H[13]	H[9]	G[6]
H	G[13]	$V_{SS\_HV\_IO}$	C[4]	A[5]		V_{DD_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{DD_LV}		V_{SS_LV}	$V_{DD\_HV\_REG\_1}$	$V_{DD\_HV\_FLA}$	H[6]
J	F[7]	G[15]	$V_{DD\_HV\_REG\_0}$	$V_{DD\_HV\_REG\_0}$		V_{DD_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{DD_LV}		V_{DD_LV}	$V_{DD\_HV\_REG\_1}$	$V_{SS\_HV\_FLA}$	H[15]
K	F[9]	F[8]		C[7]		V_{DD_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{DD_LV}		NC	H[8]	H[7]	A[3]
L	F[10]	F[11]	D[9]	NC		V_{DD_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{DD_LV}		NC	TCK	H[4]	B[4]
M	$V_{DD\_HV\_OSC}$	$V_{DD\_HV\_IO}$	D[8]	NC		V_{DD_LV}	V_{DD_LV}	V_{DD_LV}	V_{DD_LV}	V_{DD_LV}	V_{DD_LV}	V_{DD_LV}		C[11]	B[5]	TMS	H[5]
N	XTAL	$V_{SS\_HV\_IO}$	D[5]	$V_{SS\_LV\_PLL}$										NC	C[12]	A[2]	G[5]
P	$V_{SS\_HV\_OSC}$	$\overline{\text{RESET}}$	D[6]	$V_{DD\_LV\_PLL}$	$V_{DD\_LV\_COR}$	$V_{SS\_LV\_COR}$	B[8]	NC	$V_{SS\_HV\_IO}$	$V_{DD\_HV\_IO}$	B[14]	$V_{DD\_LV\_COR}$	$V_{SS\_LV\_COR}$	$V_{DD\_HV\_IO}$	G[10]	G[8]	G[7]
R	EXTAL	FCCU_F[0]	$V_{SS\_HV\_IO}$	D[7]	B[7]	E[6]	$V_{DD\_HV\_ADR0}$	B[10]	$V_{DD\_HV\_ADR1}$	B[13]	B[15]	C[0]	BCTRL	A[1]	$V_{SS\_HV\_IO}$	D[11]	G[9]
T	$V_{SS\_HV\_IO}$	$V_{DD\_HV\_IO}$	NC	C[1]	E[5]	E[7]	$V_{SS\_HV\_ADR0}$	B[11]	$V_{SS\_HV\_ADR1}$	E[9]	E[10]	E[12]	E[0]	A[0]	D[10]	$V_{DD\_HV\_IO}$	$V_{SS\_HV\_IO}$
U	$V_{SS\_HV\_IO}$	$V_{SS\_HV\_IO}$	NC	E[4]	C[2]	E[2]	B[9]	B[12]	$V_{DD\_HV\_ADV}$	$V_{SS\_HV\_ADV}$	E[11]	NC	NC	$V_{DD\_HV\_PMU}$	G[11]	$V_{SS\_HV\_IO}$	$V_{SS\_HV\_IO}$
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17

1 NC = Not connected (the pin is physically not connected to anything on the device)

Figure 3. MPC5643L 257 MAPBGA pinout (top view)

Table 3 and Table 4 provide the pin function summaries for the 144-pin and 257-pin packages, respectively, listing all the signals multiplexed to each pin.

Table 3. 144 LQFP pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
14	A[5]	SIUL	GPIO[5]	GPIO[5]
		DSPI_1	CS0	CS0
		eTimer_1	ETC[5]	ETC[5]
		DSPI_0	CS7	—
		SIUL	—	EIRQ[5]
15	C[7]	SIUL	GPIO[39]	GPIO[39]
		FlexPWM_0	A[1]	A[1]
		SSCM	DEBUG[7]	—
		DSPI_0	—	SIN
16	$V_{DD\_HV\_REG\_0}$	—		
17	$V_{SS\_LV\_COR}$	—		
18	$V_{DD\_LV\_COR}$	—		
19	F[7]	SIUL	GPIO[87]	GPIO[87]
		NPC	MCKO	—
20	F[8]	SIUL	GPIO[88]	GPIO[88]
		NPC	$\overline{\text{MSEO[1]}}$	—
21	$V_{DD\_HV\_IO}$	—		
22	$V_{SS\_HV\_IO}$	—		
23	F[9]	SIUL	GPIO[89]	GPIO[89]
		NPC	$\overline{\text{MSEO[0]}}$	—
24	F[10]	SIUL	GPIO[90]	GPIO[90]
		NPC	$\overline{\text{EVTO}}$	—
25	F[11]	SIUL	GPIO[91]	GPIO[91]
		NPC	—	$\overline{\text{EVTI}}$
26	D[9]	SIUL	GPIO[57]	GPIO[57]
		FlexPWM_0	X[0]	X[0]
		LINFlexD_1	TXD	—
27	$V_{DD\_HV\_OSC}$	—		
28	$V_{SS\_HV\_OSC}$	—		
29	XTAL	—		
30	EXTAL	—		
31	$\overline{\text{RESET}}$	—		

Table 3. 144 LQFP pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
32	D[8]	SIUL	GPIO[56]	GPIO[56]
		DSPI_1	CS2	—
		eTimer_1	ETC[4]	ETC[4]
		DSPI_0	CS5	—
		FlexPWM_0	—	FAULT[3]
33	D[5]	SIUL	GPIO[53]	GPIO[53]
		DSPI_0	CS3	—
		FlexPWM_0	—	FAULT[2]
34	D[6]	SIUL	GPIO[54]	GPIO[54]
		DSPI_0	CS2	—
		FlexPWM_0	X[3]	X[3]
		FlexPWM_0	—	FAULT[1]
35	$V_{SS\_LV\_PLL0\_PLL1}$	—		
36	$V_{DD\_LV\_PLL0\_PLL1}$	—		
37	D[7]	SIUL	GPIO[55]	GPIO[55]
		DSPI_1	CS3	—
		DSPI_0	CS4	—
		SWG	analog output	—
38	FCCU_F[0]	FCCU	F[0]	F[0]
39	$V_{DD\_LV\_COR}$	—		
40	$V_{SS\_LV\_COR}$	—		
41	C[1]	SIUL	—	GPIO[33]
		ADC_0	—	AN[2]
42	E[4]	SIUL	—	GPIO[68]
		ADC_0	—	AN[7]
43	B[7]	SIUL	—	GPIO[23]
		LINFlexD_0	—	RXD
		ADC_0	—	AN[0]
44	E[5]	SIUL	—	GPIO[69]
		ADC_0	—	AN[8]
45	C[2]	SIUL	—	GPIO[34]
		ADC_0	—	AN[3]
46	E[6]	SIUL	—	GPIO[70]
		ADC_0	—	AN[4]

Table 3. 144 LQFP pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
89	B[4]	SIUL	GPIO[20]	GPIO[20]
		JTAGC	TDO	—
90	$V_{SS\_HV\_IO}$	—		
91	$V_{DD\_HV\_IO}$	—		
92	A[3]	SIUL	GPIO[3]	GPIO[3]
		eTimer_0	ETC[3]	ETC[3]
		DSPI_2	CS0	CS0
		FlexPWM_0	B[3]	B[3]
		MC_RGM	—	ABS[2]
		SIUL	—	EIRQ[3]
93	$V_{DD\_LV\_COR}$	—		
94	$V_{SS\_LV\_COR}$	—		
95	$V_{DD\_HV\_REG\_1}$	—		
96	$V_{SS\_HV\_FLA}$	—		
97	$V_{DD\_HV\_FLA}$	—		
98	G[6]	SIUL	GPIO[102]	GPIO[102]
		FlexPWM_0	A[3]	A[3]
99	D[12]	SIUL	GPIO[60]	GPIO[60]
		FlexPWM_0	X[1]	X[1]
		LINFlexD_1	—	RXD
100	G[4]	SIUL	GPIO[100]	GPIO[100]
		FlexPWM_0	B[2]	B[2]
		eTimer_0	—	ETC[5]
101	C[13]	SIUL	GPIO[45]	GPIO[45]
		eTimer_1	ETC[1]	ETC[1]
		CTU_0	—	EXT_IN
		FlexPWM_0	—	EXT_SYNC
102	G[2]	SIUL	GPIO[98]	GPIO[98]
		FlexPWM_0	X[2]	X[2]
		DSPI_1	CS1	—
103	C[14]	SIUL	GPIO[46]	GPIO[46]
		eTimer_1	ETC[2]	ETC[2]
		CTU_0	EXT_TGR	—

Table 4. 257 MAPBGA pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
A11	H[10]	SIUL	GPIO[122]	GPIO[122]
		FlexPWM_1	X[2]	X[2]
		eTimer_2	ETC[2]	ETC[2]
A12	H[14]	SIUL	GPIO[126]	GPIO[126]
		FlexPWM_1	A[3]	A[3]
		eTimer_2	ETC[4]	ETC[4]
A13	A[10]	SIUL	GPIO[10]	GPIO[10]
		DSPI_2	CS0	CS0
		FlexPWM_0	B[0]	B[0]
		FlexPWM_0	X[2]	X[2]
		SIUL	—	EIRQ[9]
A14	B[2]	SIUL	GPIO[18]	GPIO[18]
		LINFlexD_0	TXD	—
		SSCM	DEBUG[2]	—
		SIUL	—	EIRQ[17]
A15	C[10]	SIUL	GPIO[42]	GPIO[42]
		DSPI_2	CS2	—
		FlexPWM_0	A[3]	A[3]
		FlexPWM_0	—	FAULT[1]
A16	$V_{SS\_HV\_IO\_RING}$	—		
A17	$V_{SS\_HV\_IO\_RING}$	—		
B1	$V_{SS\_HV\_IO\_RING}$	—		
B2	$V_{SS\_HV\_IO\_RING}$	—		
B3	B[6]	SIUL	GPIO[22]	GPIO[22]
		MC_CGM	clk_out	—
		DSPI_2	CS2	—
		SIUL	—	EIRQ[18]
B4	A[14]	SIUL	GPIO[14]	GPIO[14]
		FlexCAN_1	TXD	—
		eTimer_1	ETC[4]	ETC[4]
		SIUL	—	EIRQ[13]
B5	F[3]	SIUL	GPIO[83]	GPIO[83]
		DSPI_0	CS6	—

Table 4. 257 MAPBGA pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
D11	A[11]	SIUL	GPIO[11]	GPIO[11]
		DSPI_2	SCK	SCK
		FlexPWM_0	A[0]	A[0]
		FlexPWM_0	A[2]	A[2]
		SIUL	—	EIRQ[10]
D12	E[13]	SIUL	GPIO[77]	GPIO[77]
		eTimer_0	ETC[5]	ETC[5]
		DSPI_2	CS3	—
		SIUL	—	EIRQ[25]
D13	F[15]	SIUL	GPIO[95]	GPIO[95]
		LINFlexD_1	—	RXD
D14	$V_{DD\_HV\_IO\_RING}$	—		
D15	V_{PP_TEST}[1]	—		
D16	D[14]	SIUL	GPIO[62]	GPIO[62]
		FlexPWM_0	B[1]	B[1]
		eTimer_0	—	ETC[3]
D17	G[3]	SIUL	GPIO[99]	GPIO[99]
		FlexPWM_0	A[2]	A[2]
		eTimer_0	—	ETC[4]
E1	MDO0	—		
E2	F[6]	SIUL	GPIO[86]	GPIO[86]
		NPC	MDO[1]	—
E3	D[1]	SIUL	GPIO[49]	GPIO[49]
		eTimer_1	ETC[2]	ETC[2]
		CTU_0	EXT_TGR	—
		FlexRay	—	CA_RX
E4	$\overline{NMI}$	—		
E14	Not connected	—		
E15	C[14]	SIUL	GPIO[46]	GPIO[46]
		eTimer_1	ETC[2]	ETC[2]
		CTU_0	EXT_TGR	—
E16	G[2]	SIUL	GPIO[98]	GPIO[98]
		FlexPWM_0	X[2]	X[2]
		DSPI_1	CS1	—

Table 4. 257 MAPBGA pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
K17	A[3]	SIUL	GPIO[3]	GPIO[3]
		eTimer_0	ETC[3]	ETC[3]
		DSPI_2	CS0	CS0
		FlexPWM_0	B[3]	B[3]
		MC_RGM	—	ABS[2]
		SIUL	—	EIRQ[3]
L1	F[10]	SIUL	GPIO[90]	GPIO[90]
		NPC	$\overline{\text{EVTO}}$	—
L2	F[11]	SIUL	GPIO[91]	GPIO[91]
		NPC	—	$\overline{\text{EVTI}}$
L3	D[9]	SIUL	GPIO[57]	GPIO[57]
		FlexPWM_0	X[0]	X[0]
		LINFlexD_1	TXD	—
L4	Not connected	—		
L6	V_{DD_LV}	—		
L7	V_{SS_LV}	—		
L8	V_{SS_LV}	—		
L9	V_{SS_LV}	—		
L10	V_{SS_LV}	—		
L11	V_{SS_LV}	—		
L12	V_{DD_LV}	—		
L14	Not connected	—		
L15	TCK	—		
L16	H[4]	SIUL	GPIO[116]	GPIO[116]
		FlexPWM_1	X[0]	X[0]
		eTimer_2	ETC[0]	ETC[0]
L17	B[4]	SIUL	GPIO[20]	GPIO[20]
		JTAGC	TDO	—
M1	$V_{DD\_HV\_OSC}$	—		
M2	$V_{DD\_HV\_IO\_RING}$	—		
M3	D[8]	SIUL	GPIO[56]	GPIO[56]
		DSPI_1	CS2	—
		eTimer_1	ETC[4]	ETC[4]
		DSPI_0	CS5	—
		FlexPWM_0	—	FAULT[3]

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed[1]		Pin #		
								SRC = 1	SRC = 0		144 pkg	257 pkg
A[10]	PCR[10]	SIUL	GPIO[10]	ALT0	GPIO[10]	—	—	M	S		118	A13
		DSPI_2	CS0	ALT1	CS0	PSMI[3]; PADSEL=1						
		FlexPWM_0	B[0]	ALT2	B[0]	PSMI[24]; PADSEL=0						
		FlexPWM_0	X[2]	ALT3	X[2]	PSMI[29]; PADSEL=0						
		SIUL	—	—	EIRQ[9]	—						
A[11]	PCR[11]	SIUL	GPIO[11]	ALT0	GPIO[11]	—	—	M	S		120	D11
		DSPI_2	SCK	ALT1	SCK	PSMI[1]; PADSEL=1						
		FlexPWM_0	A[0]	ALT2	A[0]	PSMI[20]; PADSEL=0						
		FlexPWM_0	A[2]	ALT3	A[2]	PSMI[22]; PADSEL=0						
		SIUL	—	—	EIRQ[10]	—						
A[12]	PCR[12]	SIUL	GPIO[12]	ALT0	GPIO[12]	—	—	M	S		122	A10
		DSPI_2	SOUT	ALT1	—	—						
		FlexPWM_0	A[2]	ALT2	A[2]	PSMI[22]; PADSEL=1						
		FlexPWM_0	B[2]	ALT3	B[2]	PSMI[26]; PADSEL=0						
		SIUL	—	—	EIRQ[11]	—						

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed[1]		Pin #		
								SRC = 1	SRC = 0		144 pkg	257 pkg
H[10]	PCR[122]	SIUL	GPIO[122]	ALT0	GPIO[122]	—	—	M	S		—	A11
		FlexPWM_1	X[2]	ALT1	X[2]	—						
		eTimer_2	ETC[2]	ALT2	ETC[2]	—						
H[11]	PCR[123]	SIUL	GPIO[123]	ALT0	GPIO[123]	—	—	M	S		—	C11
		FlexPWM_1	A[2]	ALT1	A[2]	—						
H[12]	PCR[124]	SIUL	GPIO[124]	ALT0	GPIO[124]	—	—	M	S		—	B10
		FlexPWM_1	B[2]	ALT1	B[2]	—						
H[13]	PCR[125]	SIUL	GPIO[125]	ALT0	GPIO[125]	—	—	M	S		—	G15
		FlexPWM_1	X[3]	ALT1	X[3]	—						
		eTimer_2	ETC[3]	ALT2	ETC[3]	PSMI[42]; PADSEL=0						
H[14]	PCR[126]	SIUL	GPIO[126]	ALT0	GPIO[126]	—	—	M	S		—	A12
		FlexPWM_1	A[3]	ALT1	A[3]	—						
		eTimer_2	ETC[4]	ALT2	ETC[4]	—						
H[15]	PCR[127]	SIUL	GPIO[127]	ALT0	GPIO[127]	—	—	M	S		—	J17
		FlexPWM_1	B[3]	ALT1	B[3]	—						
		eTimer_2	ETC[5]	ALT2	ETC[5]	—						
Port I												
I[0]	PCR[128]	SIUL	GPIO[128]	ALT0	GPIO[128]	—	—	M	S		—	C9
		eTimer_2	ETC[0]	ALT1	ETC[0]	PSMI[39]; PADSEL=1						
		DSPI_0	CS4	ALT2	—	—						
		FlexPWM_1	—	—	FAULT[0]	—						

3 Electrical characteristics

3.1 Introduction

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for this device.

This device is designed to operate at 120 MHz. The electrical specifications are preliminary and are from previous designs, design simulations, or initial evaluation. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications will be published after complete characterization and device qualifications have been completed.

The “Symbol” column of the electrical parameter and timings tables contains an additional column containing “SR”, “CC”, “P”, “C”, “T”, or “D”.

- “SR” identifies system requirements—conditions that must be provided to ensure normal device operation. An example is the input voltage of a voltage regulator.
- “CC” identifies controller characteristics—indicating the characteristics and timing of the signals that the chip provides.
- “P”, “C”, “T”, or “D” apply only to controller characteristics—specifications that define normal device operation. They specify how each characteristic is guaranteed.
  - P: parameter is guaranteed by production testing of each individual device.
  - C: parameter is guaranteed by design characterization. Measurements are taken from a statistically relevant sample size across process variations.
  - T: parameter is guaranteed by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values are shown in the typical (“typ”) column are within this category.
  - D: parameters are derived mainly from simulations.

3.2 Absolute maximum ratings

Table 8. Absolute maximum ratings[1]

Symbol		Parameter	Conditions	Min	Max	Unit
$V_{DD\_HV\_REG}$	SR	3.3 V voltage regulator supply voltage	—	–0.3	3.63[2, 3]	V
$V_{DD\_HV\_IOx}$	SR	3.3 V input/output supply voltage	—	–0.3	3.63[2, 3]	V
$V_{SS\_HV\_IOx}$	SR	Input/output ground voltage	—	–0.1	0.1	V
$V_{DD\_HV\_FLA}$	SR	3.3 V flash supply voltage	—	–0.3	3.63[2, 3]	V
$V_{SS\_HV\_FLA}$	SR	Flash memory ground	—	–0.1	0.1	V
$V_{DD\_HV\_OSC}$	SR	3.3 V crystal oscillator amplifier supply voltage	—	–0.3	3.63[2, 3]	V
$V_{SS\_HV\_OSC}$	SR	3.3 V crystal oscillator amplifier reference voltage	—	–0.1	0.1	V
$V_{DD\_HV\_ADR0}$[3,4] $V_{DD\_HV\_ADR1}$	SR	3.3 V / 5.0 V ADC_0 high reference voltage 3.3 V / 5.0 V ADC_1 high reference voltage	—	–0.3	6.0	V
$V_{SS\_HV\_ADR0}$ $V_{SS\_HV\_ADR1}$	SR	ADC_0 ground and low reference voltage ADC_1 ground and low reference voltage	—	–0.1	0.1	V
$V_{DD\_HV\_ADV}$	SR	3.3 V ADC supply voltage	—	–0.3	3.63[2, 3]	V
$V_{SS\_HV\_ADV}$	SR	3.3 V ADC supply ground	—	–0.1	0.1	V

Table 9. Recommended operating conditions (3.3 V) (continued)

Symbol		Parameter	Conditions	Min[1]	Max	Unit
$V_{SS\_LV\_CORx}$[3]	SR	Internal reference voltage	—	0	0	V
$V_{DD\_LV\_PLL}$[2]	SR	Internal supply voltage	—	—	—	V
$V_{SS\_LV\_PLL}$[3]	SR	Internal reference voltage	—	0	0	V
T_A	SR	Ambient temperature under bias	$f_{CPU} \leq 120$ MHz	–40	125	°C
T_J	SR	Junction temperature under bias	—	–40	150	°C

1 Full functionality cannot be guaranteed when voltage drops below 3.0 V. In particular, ADC electrical characteristics and I/Os DC electrical specification may not be guaranteed.

2 $V_{DD\_HV\_ADR0}$ and $V_{DD\_HV\_ADR1}$ cannot be operated at different voltages, and need to be supplied by the same voltage source.

3 $V_{DD\_HV\_ADRx}$ must always be applied and should be stable before LBIST starts. If this supply is not above its absolute minimum level, LBIST operations can fail.

4 Can be connected to emitter of external NPN. Low voltage supplies are not under user control. They are produced by an on-chip voltage regulator.

5 For the device to function properly, the low voltage grounds ($V_{SS\_LV\_xxx}$) must be shorted to high voltage grounds ($V_{SS\_HV\_xxx}$) and the low voltage supply pins ($V_{DD\_LV\_xxx}$) must be connected to the external ballast emitter, if one is used.

3.4 Thermal characteristics

Table 10. Thermal characteristics for 100 LQFP package[1]

Symbol		Parameter	Conditions	Value	Unit
$R_{\theta JA}$	D	Thermal resistance, junction-to-ambient natural convection[2]	Single layer board – 1s	46	°C/W
			Four layer board – 2s2p	34	
$R_{\theta JMA}$	D	Thermal resistance, junction-to-ambient forced convection at 200 ft/min	Single layer board – 1s	36	°C/W
			Four layer board – 2s2p	28	
$R_{\theta JB}$	D	Thermal resistance junction-to-board[3]	—	19	°C/W
$R_{\theta JC}$	D	Thermal resistance junction-to-case[4]	—	8	°C/W
Ψ_{JT}	D	Junction-to-package-top natural convection[5]	—	2	°C/W

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Junction-to-Ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

3 Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

4 Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

5 Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 14. EMI emission testing specifications

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
V_{EME}	CC	Radiated emissions	Configuration A; frequency range 150 kHz–50 MHz	—	16	—	dBµV
			Configuration A; frequency range 50–150 MHz	—	16	—	
			Configuration A; frequency range 150–500 MHz	—	32	—	
			Configuration A; frequency range 500–1000 MHz	—	25	—	
			Configuration B; frequency range 50–150 MHz	—	15	—	
			Configuration B; frequency range 50–150 MHz	—	21	—	
			Configuration B; frequency range 150–500 MHz	—	30	—	
			Configuration B; frequency range 500–1000 MHz	—	24	—	

EMC testing was performed and documented according to these standards: [IEC61508-2-7.4.5.1.b, IEC61508-2-7.2.3.2.e, IEC61508-2-Table-A.17 (partially), IEC61508-2-Table-B.5(partially),SRS2110]

EME testing was performed and documented according to these standards: [IEC 61967-2 & -4]

EMS testing was performed and documented according to these standards: [IEC 62132-2 & -4]

Refer MPC5643L for detailed information pertaining to the EMC, EME, and EMS testing and results.

3.6 Electrostatic discharge (ESD) characteristics

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n + 1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard.

Table 15. ESD ratings[1, 2]

No.	Symbol		Parameter	Conditions	Class	Max value[3]	Unit
1	$V_{ESD(HBM)}$	SR	Electrostatic discharge (Human Body Model)	T_A = 25 °C conforming to AEC-Q100-002	H1C	2000	V
2	$V_{ESD(MM)}$	SR	Electrostatic discharge (Machine Model)	T_A = 25 °C conforming to AEC-Q100-003	M2	200	V
3	$V_{ESD(CDM)}$	SR	Electrostatic discharge (Charged Device Model)	T_A = 25 °C conforming to AEC-Q100-011	C3A	500 750 (corners)	V

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 18. Voltage regulator electrical specifications (continued)

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
—	D	Digital supply low voltage detector lower threshold	After a destructive reset initialization phase completion	1.080	—	1.140	V
—	D	Digital supply low voltage detector upper threshold	After a destructive reset initialization phase completion	1.16	—	1.22	V
—	D	Digital supply low voltage detector lower threshold	Before a destructive reset initialization phase	1.080	—	1.226	V
—	D	Digital supply low voltage detector upper threshold	Before a destructive reset initialization phase	1.160	—	1.306	V
—	D	POR rising/ falling supply threshold voltage	—	1.6	—	2.6	V
—	SR	Supply ramp rate	—	3 V/s	—	0.5 V/µs	—
—	D	LVD_MAIN: Time constant of RC filter at LVD input	3.3V noise rejection at the input of LVD comparator	1.1	—	—	µs
—	D	HVD_DIG: Time constant of RC filter at LVD input	1.2V noise rejection at the input of LVD comparator	0.1	—	—	µs
—	D	LVD_DIG: Time constant of RC filter at LVD input	1.2V noise rejection at the input of LVD comparator	0.1	—	—	µs

3.14 16 MHz RC oscillator electrical characteristics

Table 24. 16 MHz RC oscillator electrical characteristics

Symbol	C	Parameter	Conditions	Value			Unit
				Min	Typ	Max	
f_{RC}	P	RC oscillator frequency	T_A = 25 °C	—	16	—	MHz
Δ_{RCMVAR}	P	Fast internal RC oscillator variation over temperature and supply with respect to f_{RC} at T_A = 25 °C in high-frequency configuration	—	–6	—	6	%

3.15 ADC electrical characteristics

The device provides a 12-bit Successive Approximation Register (SAR) Analog-to-Digital Converter.

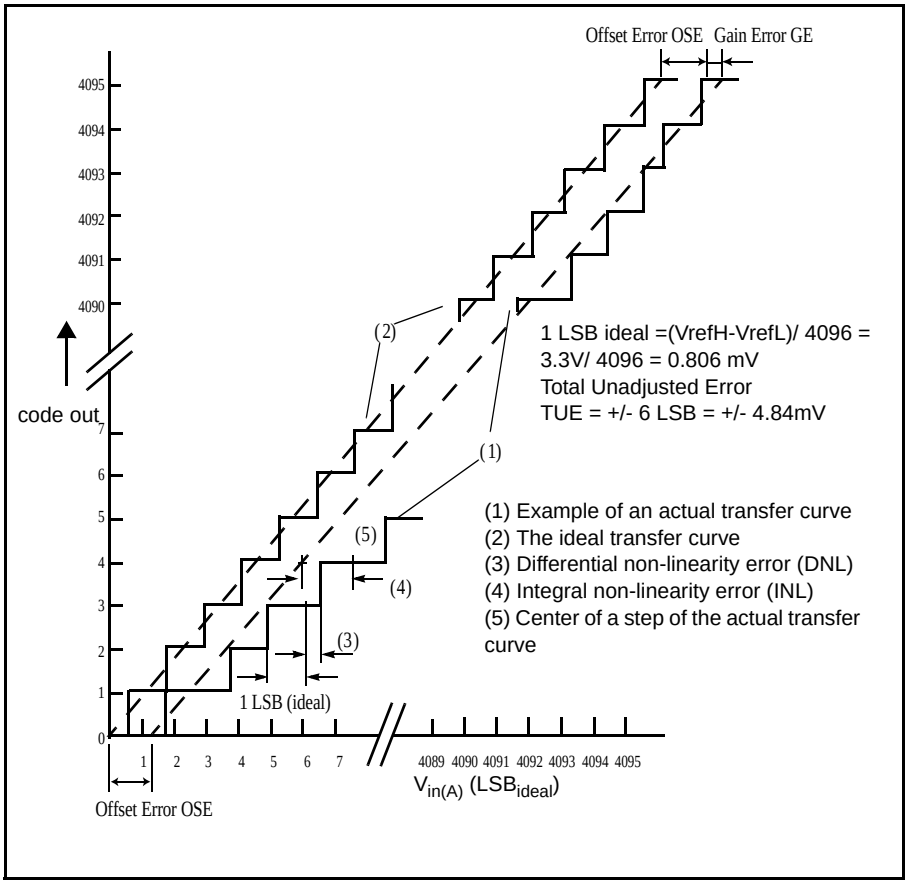

Figure 7. ADC characteristics and error definitions

3.15.1 Input Impedance and ADC Accuracy

To preserve the accuracy of the A/D converter, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device can be effective: the capacitor should be as large as possible, ideally infinite. This capacitor contributes to attenuating the noise present on the input pin; further, it sources charge during the sampling phase, when the analog signal source is a high-impedance source.

A real filter can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC filter). The RC filtering may be limited according to the value of source impedance of the transducer or circuit supplying the analog signal to be measured. The filter at the input pins must be designed taking into account the dynamic characteristics of the input signal (bandwidth) and the equivalent input impedance of the ADC itself.

In fact a current sink contributor is represented by the charge sharing effects with the sampling capacitance: C_S and C_{p2} being substantially a switched capacitance, with a frequency equal to the conversion rate of the ADC, it can be seen as a resistive path to ground. For instance, assuming a conversion rate of 1 MHz, with C_{p2} + CS equal to 7.5 pF, a resistance of 133 kΩ is obtained (R_{EQ} = 1 / (fS*(C_{p2}+C_S)), where fS represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on C_s) and the sum of R_S + R_F, the external circuit must be designed to respect the Equation 4:

$$V_A \bullet \frac{R_S + R_F}{R_{EQ}} < \frac{1}{2} LSB \qquad \textit{Eqn. 4}$$

Equation 4 generates a constraint for external network design, in particular on resistive path. Internal switch resistances (R_{SW} and R_{AD}) can be neglected with respect to external resistances.

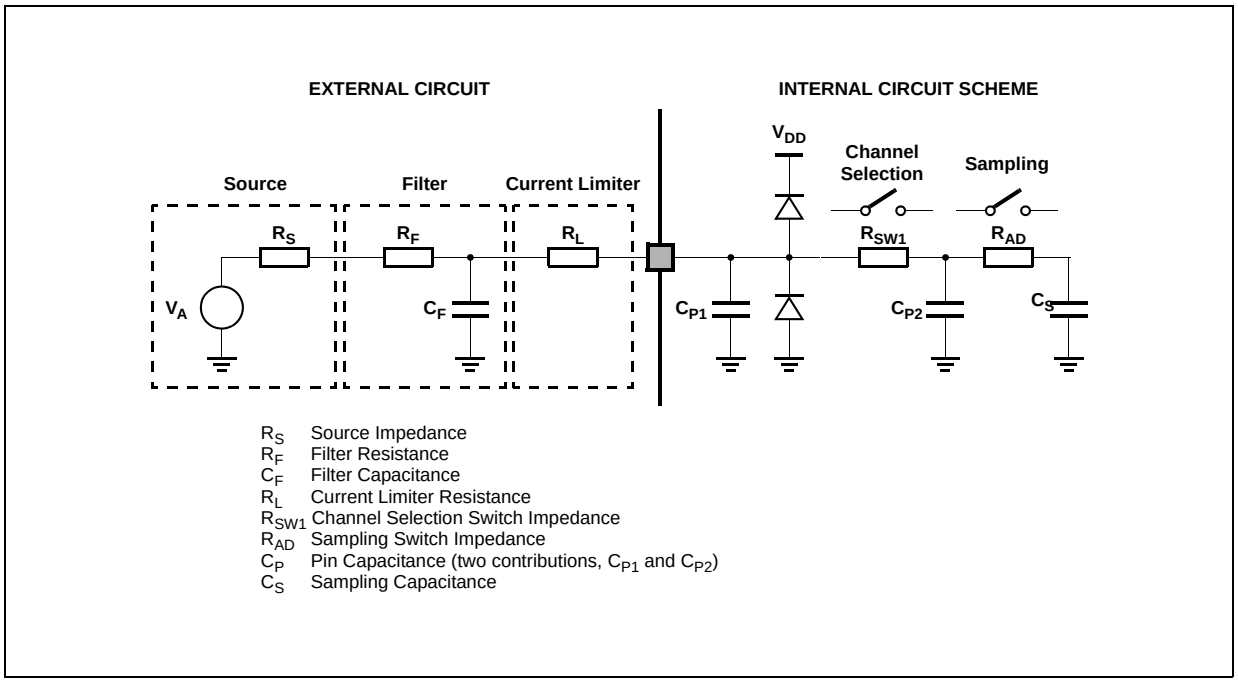

Figure 8. Input Equivalent Circuit

A second aspect involving the capacitance network shall be considered. Assuming the three capacitances C_F, C_{P1} and C_{P2} are initially charged at the source voltage V_A (refer to the equivalent circuit reported in Figure 8): A charge sharing phenomenon is installed when the sampling phase is started (A/D switch close).

Table 25. ADC conversion characteristics

Symbol		Parameter	Conditions[1]	Min	Typ	Max	Unit
f_{CK}	SR	ADC Clock frequency (depends on ADC configuration) (The duty cycle depends on AD_CK[2] frequency)	—	3	—	60	MHz
f_S	SR	Sampling frequency	—	—	—	983.6[3]	KHz
t_{sample}	D	Sample time[4]	60 MHz	383	—	—	ns
t_{eval}	D	Evaluation time[5]	60 MHz	600	—	—	ns
C_S[6]	D	ADC input sampling capacitance	—	—	—	7.32	pF
C_{P1}[6]	D	ADC input pin capacitance 1	—	—	—	5[(7)]	pF
C_{P2}[6]	D	ADC input pin capacitance 2	—	—	—	0.8	pF
R_{SW1}[6]	D	Internal resistance of analog source	V_{REF} range = 4.5 to 5.5 V	—	—	0.3	kΩ
			V_{REF} range = 3.0 to 3.6 V	—	—	875	Ω
R_{AD}[6]	D	Internal resistance of analog source	—	—	—	825	Ω
INL	P	Integral non linearity	—	–3	—	3	LSB
DNL	P	Differential non linearity[8]	—	–1	—	2	LSB
OFS	T	Offset error	—	–6	—	6	LSB
GNE	T	Gain error	—	–6	—	6	LSB
IS1WINJ			(single ADC channel)				
	C	Max positive/negative injection		–3	—	3	mA
IS1WWINJ			(double ADC channel)				
	C	Max positive/negative injection	|Vref_ad0 - Vref_ad1| < 150mV	–3.6	—	3.6	mA
SNR	T	Signal-to-noise ratio	Vref = 3.3V	67	—	—	dB
SNR	T	Signal-to-noise ratio	Vref = 5.0V	69	—	—	dB
THD	T	Total harmonic distortion	—	-65	—	—	dB
SINAD	T	Signal-to-noise and distortion	—	65	—	—	dB
ENOB	T	Effective number of bits	—	10.5	—	—	bits
$TUE_{IS1WINJ}$	T	Total unadjusted error for IS1WINJ (single ADC channels)	Without current injection	–6	—	6	LSB
			With current injection	–8	—	8	LSB
$TUE_{IS1WWINJ}$	P	Total unadjusted error for IS1WWINJ (double ADC channels)	Without current injection	–8	—	8	LSB
	T		With current injection	–10	—	10	LSB

1 T_J = –40 to +150 °C, unless otherwise specified and analog input voltage from V_{AGND} to V_{AREF}.

2 AD_CK clock is always half of the ADC module input clock defined via the auxiliary clock divider for the ADC.

3 This is the maximum frequency that the analog portion of the ADC can attain. A sustained conversion at this frequency is not possible.

[1] Repeated suspends at a high frequency may result in the operation timing out, and the flash module will respond by completing the operation with a fail code (MCR[PEG] = 0), or the operation not able to finish (MCR[DONE] = 1 during Program operation). The minimum time between suspends to ensure this does not occur is T_{PSRT}.

[2] If Erase suspend rate is less than T_{ESRT}, an increase of slope voltage ramp occurs during erase pulse. This improves erase time but reduces cycling figure due to overstress

Table 28. Flash memory module life

No.	Symbol		Parameter	Value			Unit
				Minimum	Typical	Maximum	
1	P/E	C	Number of program/erase cycles per block for 16 KB, 48 KB, and 64 KB blocks over the operating temperature range[1]	100000	—	—	cycles
2	P/E	C	Number of program/erase cycles per block for 128 KB and 256 KB blocks over the operating temperature range[1]	1000	100000[2]	—	cycles
3	Retention	C	Minimum data retention at 85 °C average ambient temperature[3] Blocks with 0–1,000 P/E cycles Blocks with 1,001–10,000 P/E cycles Blocks with 10,001–100,000 P/E cycles	 20 10 5	 — — —	 — — —	years

[1] Operating temperature range is T_J from –40 °C to 150 °C. Typical endurance is evaluated at 25 °C. Product qualification is performed to the minimum specification. For additional information on the Freescale definition of Typical Endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory*.

[2] Typical P/E cycles is 100,000 cycles for 128 KB and 256 KB blocks. For additional information on the Freescale definition of Typical Endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory*.

[3] Ambient temperature averaged over duration of application, not to exceed product operating temperature range.

3.17 SWG electrical characteristics

Table 29. MPC5643L **SWG Specifications**

Symbol	Parameter	Value		
		Minimum	Typical	Maximum
T	Input clock	12 MHz	16 MHz	20 MHz
T	Frequency Range	1kHz	—	50 kHz
T	Peak to Peak[1]	0.4 V	—	2.0V
T	Peak to Peak variation[2]	-6%	—	6%
T	Common Mode[3]	—	1.3 V	—
T	Common Mode variation	-6%	—	6%