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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	e200z4
Core Size	32-Bit Dual-Core
Speed	120MHz
Connectivity	CANbus, FlexRay, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	-
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5643lff0mlq1r

1.5.2 Crossbar switch (XBAR)

The XBAR multi-port crossbar switch supports simultaneous connections between four master ports and three slave ports. The crossbar supports a 32-bit address bus width and a 64-bit data bus width.

The crossbar allows four concurrent transactions to occur from any master port to any slave port, although one of those transfers must be an instruction fetch from internal flash memory. If a slave port is simultaneously requested by more than one master port, arbitration logic selects the higher priority master and grants it ownership of the slave port. All other masters requesting that slave port are stalled until the higher priority master completes its transactions.

The crossbar provides the following features:

- 4 masters and 3 slaves supported per each replicated crossbar
  - Masters allocation for each crossbar: e200z4d core with two independent bus interface units (BIU) for I and D access (2 masters), one eDMA, one FlexRay
  - Slaves allocation for each crossbar: a redundant flash-memory controller with 2 slave ports to guarantee maximum flexibility to handle Instruction and Data array, one redundant SRAM controller with 1 slave port each and 1 redundant peripheral bus bridge
- 32-bit address bus and 64-bit data bus
- Programmable arbitration priority
  - Requesting masters can be treated with equal priority and are granted access to a slave port in round-robin method, based upon the ID of the last master to be granted access or a priority order can be assigned by software at application run time
- Temporary dynamic priority elevation of masters

The XBAR is replicated for each processing channel.

1.5.3 Memory Protection Unit (MPU)

The Memory Protection Unit splits the physical memory into 16 different regions. Each master (eDMA, FlexRay, CPU) can be assigned different access rights to each region.

- 16-region MPU with concurrent checks against each master access
- 32-byte granularity for protected address region

The memory protection unit is replicated for each processing channel.

1.5.4 Enhanced Direct Memory Access (eDMA)

The enhanced direct memory access (eDMA) controller is a second-generation module capable of performing complex data movements via 16 programmable channels, with minimal intervention from the host processor. The hardware microarchitecture includes a DMA engine which performs source and destination address calculations, and the actual data movement operations, along with an SRAM-based memory containing the transfer control descriptors (TCD) for the channels. This implementation is used to minimize the overall block size.

The eDMA module provides the following features:

- 16 channels supporting 8-, 16-, and 32-bit value single or block transfers
- Support variable sized queues and circular buffered queue
- Source and destination address registers independently configured to post-increment or stay constant
- Support major and minor loop offset
- Support minor and major loop done signals
- DMA task initiated either by hardware requestor or by software
- Each DMA task can optionally generate an interrupt at completion and retirement of the task
- Signal to indicate closure of last minor loop

  - EXTEST
  - SAMPLE
  - SAMPLE/PRELOAD
- 3 test data registers: a bypass register, a boundary scan register, and a device identification register. The size of the boundary scan register is parameterized to support a variety of boundary scan chain lengths.
- TAP controller state machine that controls the operation of the data registers, instruction register and associated circuitry

1.5.40 Voltage regulator / Power Management Unit (PMU)

The on-chip voltage regulator module provides the following features:

- Single external rail required
- Single high supply required: nominal 3.3 V both for packaged and Known Good Die option
  - Packaged option requires external ballast transistor due to reduced dissipation capacity at high temperature but can use embedded transistor if power dissipation is maintained within package dissipation capacity (lower frequency of operation)
  - Known Good Die option uses embedded ballast transistor as dissipation capacity is increased to reduce system cost
- All I/Os are at same voltage as external supply (3.3 V nominal)
- Duplicated Low-Voltage Detectors (LVD) to guarantee proper operation at all stages (reset, configuration, normal operation) and, to maximize safety coverage, one LVD can be tested while the other operates (on-line self-testing feature)

1.5.41 Built-In Self-Test (BIST) capability

This device includes the following protection against latent faults:

- Boot-time Memory Built-In Self-Test (MBIST)
- Boot-time scan-based Logic Built-In Self-Test (LBIST)
- Run-time ADC Built-In Self-Test (BIST)
- Run-time Built-In Self Test of LVDs

Table 3. 144 LQFP pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
14	A[5]	SIUL	GPIO[5]	GPIO[5]
		DSPI_1	CS0	CS0
		eTimer_1	ETC[5]	ETC[5]
		DSPI_0	CS7	—
		SIUL	—	EIRQ[5]
15	C[7]	SIUL	GPIO[39]	GPIO[39]
		FlexPWM_0	A[1]	A[1]
		SSCM	DEBUG[7]	—
		DSPI_0	—	SIN
16	$V_{DD\_HV\_REG\_0}$	—		
17	$V_{SS\_LV\_COR}$	—		
18	$V_{DD\_LV\_COR}$	—		
19	F[7]	SIUL	GPIO[87]	GPIO[87]
		NPC	MCKO	—
20	F[8]	SIUL	GPIO[88]	GPIO[88]
		NPC	$\overline{\text{MSEO[1]}}$	—
21	$V_{DD\_HV\_IO}$	—		
22	$V_{SS\_HV\_IO}$	—		
23	F[9]	SIUL	GPIO[89]	GPIO[89]
		NPC	$\overline{\text{MSEO[0]}}$	—
24	F[10]	SIUL	GPIO[90]	GPIO[90]
		NPC	$\overline{\text{EVTO}}$	—
25	F[11]	SIUL	GPIO[91]	GPIO[91]
		NPC	—	$\overline{\text{EVTI}}$
26	D[9]	SIUL	GPIO[57]	GPIO[57]
		FlexPWM_0	X[0]	X[0]
		LINFlexD_1	TXD	—
27	$V_{DD\_HV\_OSC}$	—		
28	$V_{SS\_HV\_OSC}$	—		
29	XTAL	—		
30	EXTAL	—		
31	$\overline{\text{RESET}}$	—		

Table 3. 144 LQFP pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
32	D[8]	SIUL	GPIO[56]	GPIO[56]
		DSPI_1	CS2	—
		eTimer_1	ETC[4]	ETC[4]
		DSPI_0	CS5	—
		FlexPWM_0	—	FAULT[3]
33	D[5]	SIUL	GPIO[53]	GPIO[53]
		DSPI_0	CS3	—
		FlexPWM_0	—	FAULT[2]
34	D[6]	SIUL	GPIO[54]	GPIO[54]
		DSPI_0	CS2	—
		FlexPWM_0	X[3]	X[3]
		FlexPWM_0	—	FAULT[1]
35	$V_{SS\_LV\_PLL0\_PLL1}$	—		
36	$V_{DD\_LV\_PLL0\_PLL1}$	—		
37	D[7]	SIUL	GPIO[55]	GPIO[55]
		DSPI_1	CS3	—
		DSPI_0	CS4	—
		SWG	analog output	—
38	FCCU_F[0]	FCCU	F[0]	F[0]
39	$V_{DD\_LV\_COR}$	—		
40	$V_{SS\_LV\_COR}$	—		
41	C[1]	SIUL	—	GPIO[33]
		ADC_0	—	AN[2]
42	E[4]	SIUL	—	GPIO[68]
		ADC_0	—	AN[7]
43	B[7]	SIUL	—	GPIO[23]
		LINFlexD_0	—	RXD
		ADC_0	—	AN[0]
44	E[5]	SIUL	—	GPIO[69]
		ADC_0	—	AN[8]
45	C[2]	SIUL	—	GPIO[34]
		ADC_0	—	AN[3]
46	E[6]	SIUL	—	GPIO[70]
		ADC_0	—	AN[4]

Table 4. 257 MAPBGA pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
C16	A[4]	SIUL	GPIO[4]	GPIO[4]
		eTimer_1	ETC[0]	ETC[0]
		DSPI_2	CS1	—
		eTimer_0	ETC[4]	ETC[4]
		MC_RGM	—	FAB
		SIUL	—	EIRQ[4]
C17	F[12]	SIUL	GPIO[92]	GPIO[92]
		eTimer_1	ETC[3]	ETC[3]
		SIUL	—	EIRQ[30]
D1	F[5]	SIUL	GPIO[85]	GPIO[85]
		NPC	MDO[2]	—
D2	F[4]	SIUL	GPIO[84]	GPIO[84]
		NPC	MDO[3]	—
D3	A[15]	SIUL	GPIO[15]	GPIO[15]
		eTimer_1	ETC[5]	ETC[5]
		FlexCAN_1	—	RXD
		FlexCAN_0	—	RXD
		SIUL	—	EIRQ[14]
D4	C[6]	SIUL	GPIO[38]	GPIO[38]
		DSPI_0	SOUT	—
		FlexPWM_0	B[1]	B[1]
		SSCM	DEBUG[6]	—
		SIUL	—	EIRQ[24]
D5	$V_{SS\_LV\_CORE\_RING}$	—		
D6	$V_{DD\_LV\_CORE\_RING}$	—		
D7	F[0]	SIUL	GPIO[80]	GPIO[80]
		FlexPWM_0	A[1]	A[1]
		eTimer_0	—	ETC[2]
		SIUL	—	EIRQ[28]
D8	$V_{DD\_HV\_IO\_RING}$	—		
D9	$V_{SS\_HV\_IO\_RING}$	—		
D10	Not connected	—		

Table 5. Supply pins (continued)

Supply			Pin #	
Symbol	**Description**		**144 pkg**	**257 pkg**
$V_{SS\_LV\_COR}$	VSS_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.		17	VSS_HV[2]
$V_{DD\_LV\_COR}$	VDD_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR}$ pin.		18	VDD_LV[1]
V_{SS} 1V2	VSS_LV_PLL0_PLL1 / 1.2 V Decoupling pins for on-chip FMPLL modules. Decoupling capacitor must be connected between this pin and $V_{DD\_LV\_PLL}$.		35	N4
V_{DD} 1V2	VDD_LV_PLL0_PLL1 Decoupling pins for on-chip FMPLL modules. Decoupling capacitor must be connected between this pin and $V_{SS\_LV\_PLL}$.		36	P4
$V_{DD\_LV\_COR}$	VDD_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR}$ pin.		39	VDD_LV[1]
$V_{SS\_LV\_COR}$	VSS_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.		40	VSS_LV[2]
$V_{DD\_LV\_COR}$	VDD_LV_COR Decoupling pins for core logic and Regulator feedback. Decoupling capacitor must be connected between this pins and $V_{SS\_LV\_REGCOR}$.		70	VDD_LV[1]
$V_{SS\_LV\_COR}$	VSS_LV_REGCOR0 Decoupling pins for core logic and Regulator feedback. Decoupling capacitor must be connected between this pins and $V_{DD\_LV\_REGCOR}$.		71	VSS_LV[2]
$V_{DD\_LV\_COR}$	VDD_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR}$ pin.		93	VDD_LV[1]
$V_{SS\_LV\_COR}$	VSS_LV_COR / 1.2 V Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.		94	VSS_LV[2]
V_{DD} 1V2	VDD_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.		131	VDD_LV[1]
V_{SS} 1V2	VSS_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.		132	VSS_LV[2]
V_{DD} 1V2	VDD_LV_COR / Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.		135	VDD_LV[1]
V_{SS} 1V2	VSS_LV_COR / Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.		137	VSS_LV[2]

[1] VDD_LV balls are tied together on the 257 MAPBGA substrate.

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed[1]		Pin #		
								SRC = 1	SRC = 0		144 pkg	257 pkg
A[2]	PCR[2]	SIUL	GPIO[2]	ALT0	GPIO[2]	—	Pull down	M	S		84	N16
		eTimer_0	ETC[2]	ALT1	ETC[2]	PSMI[37]; PADSEL=0						
		FlexPWM_0	A[3]	ALT3	A[3]	PSMI[23]; PADSEL=0						
		DSPI_2	—	—	SIN	PSMI[2]; PADSEL=0						
		MC_RGM	—	—	ABS[0]	—						
		SIUL	—	—	EIRQ[2]	—						
A[3]	PCR[3]	SIUL	GPIO[3]	ALT0	GPIO[3]	—	Pull down	M	S		92	K17
		eTimer_0	ETC[3]	ALT1	ETC[3]	PSMI[38]; PADSEL=0						
		DSPI_2	CS0	ALT2	CS0	PSMI[3]; PADSEL=0						
		FlexPWM_0	B[3]	ALT3	B[3]	PSMI[27]; PADSEL=0						
		MC_RGM	—	—	ABS[2]	—						
		SIUL	—	—	EIRQ[3]	—						
A[4]	PCR[4]	SIUL	GPIO[4]	ALT0	GPIO[4]	—	Pull down	M	S		108	C16
		eTimer_1	ETC[0]	ALT1	ETC[0]	PSMI[9]; PADSEL=0						
		DSPI_2	CS1	ALT2	—	—						
		eTimer_0	ETC[4]	ALT3	ETC[4]	PSMI[7]; PADSEL=0						
		MC_RGM	—	—	FAB	—						
		SIUL	—	—	EIRQ[4]	—						

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed[1]		Pin #		
								SRC = 1	SRC = 0		144 pkg	257 pkg
D[4]	PCR[52]	SIUL	GPIO[52]	ALT0	GPIO[52]	—	—	SYM	S		129	B7
		FlexRay	CB_TR_EN	ALT1	—	—						
		eTimer_1	ETC[5]	ALT2	ETC[5]	PSMI[14]; PADSEL=2						
		FlexPWM_0	B[3]	ALT3	B[3]	PSMI[27]; PADSEL=2						
D[5]	PCR[53]	SIUL	GPIO[53]	ALT0	GPIO[53]	—	—	M	S		33	N3
		DSPI_0	CS3	ALT1	—	—						
		FlexPWM_0	—	—	FAULT[2]	PSMI[18]; PADSEL=0						
D[6]	PCR[54]	SIUL	GPIO[54]	ALT0	GPIO[54]	—	—	M	S		34	P3
		DSPI_0	CS2	ALT1	—	—						
		FlexPWM_0	X[3]	ALT3	X[3]	PSMI[30]; PADSEL=1						
		FlexPWM_0	—	—	FAULT[1]	PSMI[17]; PADSEL=1						
D[7]	PCR[55]	SIUL	GPIO[55]	ALT0	GPIO[55]	—	—	M	S		37	R4
		DSPI_1	CS3	ALT1	—	—						
		DSPI_0	CS4	ALT3	—	—						
		SWG	analog output	—	—	—						
D[8]	PCR[56]	SIUL	GPIO[56]	ALT0	GPIO[56]	—	—	M	S		32	M3
		DSPI_1	CS2	ALT1	—	—						
		eTimer_1	ETC[4]	ALT2	ETC[4]	PSMI[13]; PADSEL=2						
		DSPI_0	CS5	ALT3	—	—						
		FlexPWM_0	—	—	FAULT[3]	PSMI[19]; PADSEL=1						

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed[1]		Pin #		
								SRC = 1	SRC = 0		144 pkg	257 pkg
D[9]	PCR[57]	SIUL	GPIO[57]	ALT0	GPIO[57]	—	—	M	S		26	L3
		FlexPWM_0	X[0]	ALT1	X[0]	—						
		LINFlexD_1	TXD	ALT2	—	—						
D[10]	PCR[58]	SIUL	GPIO[58]	ALT0	GPIO[58]	—	—	M	S		76	T15
		FlexPWM_0	A[0]	ALT1	A[0]	PSMI[20]; PADSEL=1						
		eTimer_0	—	—	ETC[0]	PSMI[35]; PADSEL=1						
D[11]	PCR[59]	SIUL	GPIO[59]	ALT0	GPIO[59]	—	—	M	S		78	R16
		FlexPWM_0	B[0]	ALT1	B[0]	PSMI[24]; PADSEL=1						
		eTimer_0	—	—	ETC[1]	PSMI[36]; PADSEL=1						
D[12]	PCR[60]	SIUL	GPIO[60]	ALT0	GPIO[60]		—	M	S		99	G14
		FlexPWM_0	X[1]	ALT1	X[1]	PSMI[28]; PADSEL=1						
		LINFlexD_1	—	—	RXD	PSMI[32]; PADSEL=1						
D[14]	PCR[62]	SIUL	GPIO[62]	ALT0	GPIO[62]	—	—	M	S		105	D16
		FlexPWM_0	B[1]	ALT1	B[1]	PSMI[25]; PADSEL=2						
		eTimer_0	—	—	ETC[3]	PSMI[38]; PADSEL=1						
Port E												
E[0]	PCR[64]	SIUL	—	ALT0	GPI[64]	—	—	—	—		68	T13
		ADC_1	—	—	AN[5][3]	—						
E[2]	PCR[66]	SIUL	—	ALT0	GPI[66]	—	—	—	—		49	U6
		ADC_0	—	—	AN[5][3]	—						

[2] Adjust resistor at bipolar transistor collector for 3.3V to avoid VCE<VCE_{SAT}

The recommended external ballast transistor is the bipolar transistor BCP68 with the gain range of 85 up to 375 (for IC=500mA, VCE=1V) provided by several suppliers. This includes the gain variations BCP68-10, BCP68-16 and BCP68-25.The most important parameters for the interoperability with the integrated voltage regulator are the DC current gain (hFE) and the temperature coefficient of the gain (XTB). While the specified gain range of most BCP68 vendors is the same, there are slight variations in the temperature coefficient parameter. MPC5643L Voltage regulator operation was simulated against the typical variation on temperature coefficient and against the specified gain range to have a robust design.

Table 18. Voltage regulator electrical specifications

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
	C_{ext}	External decoupling/ stability capacitor	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	12	—	40	µF
	SR	Combined ESR of external capacitor	—	1	—	100	mΩ
	SR	Number of pins for external decoupling/ stability capacitor	—	5	—	—	—
C_{V1V2}	SR	Total capacitance on 1.2 V pins	Ceramic capacitors, taking into account tolerance, aging, voltage and temperature variation	300	—	900	nF
t_{SU}		Start-up time after main supply stabilization	C_{load} = 10 µF × 4	—	—	2.5	ms
—		Main High Voltage Power - Low Voltage Detection, upper threshold	—	—	—	2.93	V
—	D	Main supply low voltage detector, lower threshold	—	2.6	—	—	V
—	D	Digital supply high voltage detector upper threshold	Before a destructive reset initialization phase completion	1.355	—	1.495	V
			After a destructive reset initialization phase completion	1.39	—	1.47	
—	D	Digital supply high voltage detector lower threshold	Before a destructive reset initialization phase completion	1.315	—	1.455	V
			After a destructive reset initialization phase completion	1.35	—	1.38	

Table 18. Voltage regulator electrical specifications (continued)

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
—	D	Digital supply low voltage detector lower threshold	After a destructive reset initialization phase completion	1.080	—	1.140	V
—	D	Digital supply low voltage detector upper threshold	After a destructive reset initialization phase completion	1.16	—	1.22	V
—	D	Digital supply low voltage detector lower threshold	Before a destructive reset initialization phase	1.080	—	1.226	V
—	D	Digital supply low voltage detector upper threshold	Before a destructive reset initialization phase	1.160	—	1.306	V
—	D	POR rising/ falling supply threshold voltage	—	1.6	—	2.6	V
—	SR	Supply ramp rate	—	3 V/s	—	0.5 V/µs	—
—	D	LVD_MAIN: Time constant of RC filter at LVD input	3.3V noise rejection at the input of LVD comparator	1.1	—	—	µs
—	D	HVD_DIG: Time constant of RC filter at LVD input	1.2V noise rejection at the input of LVD comparator	0.1	—	—	µs
—	D	LVD_DIG: Time constant of RC filter at LVD input	1.2V noise rejection at the input of LVD comparator	0.1	—	—	µs

A real filter can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC filter). The RC filtering may be limited according to the value of source impedance of the transducer or circuit supplying the analog signal to be measured. The filter at the input pins must be designed taking into account the dynamic characteristics of the input signal (bandwidth) and the equivalent input impedance of the ADC itself.

In fact a current sink contributor is represented by the charge sharing effects with the sampling capacitance: C_S and C_{p2} being substantially a switched capacitance, with a frequency equal to the conversion rate of the ADC, it can be seen as a resistive path to ground. For instance, assuming a conversion rate of 1 MHz, with C_{p2} + CS equal to 7.5 pF, a resistance of 133 kΩ is obtained (R_{EQ} = 1 / (fS*(C_{p2}+C_S)), where fS represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on C_s) and the sum of R_S + R_F, the external circuit must be designed to respect the Equation 4:

$$V_A \bullet \frac{R_S + R_F}{R_{EQ}} < \frac{1}{2} LSB \qquad \textit{Eqn. 4}$$

Equation 4 generates a constraint for external network design, in particular on resistive path. Internal switch resistances (R_{SW} and R_{AD}) can be neglected with respect to external resistances.

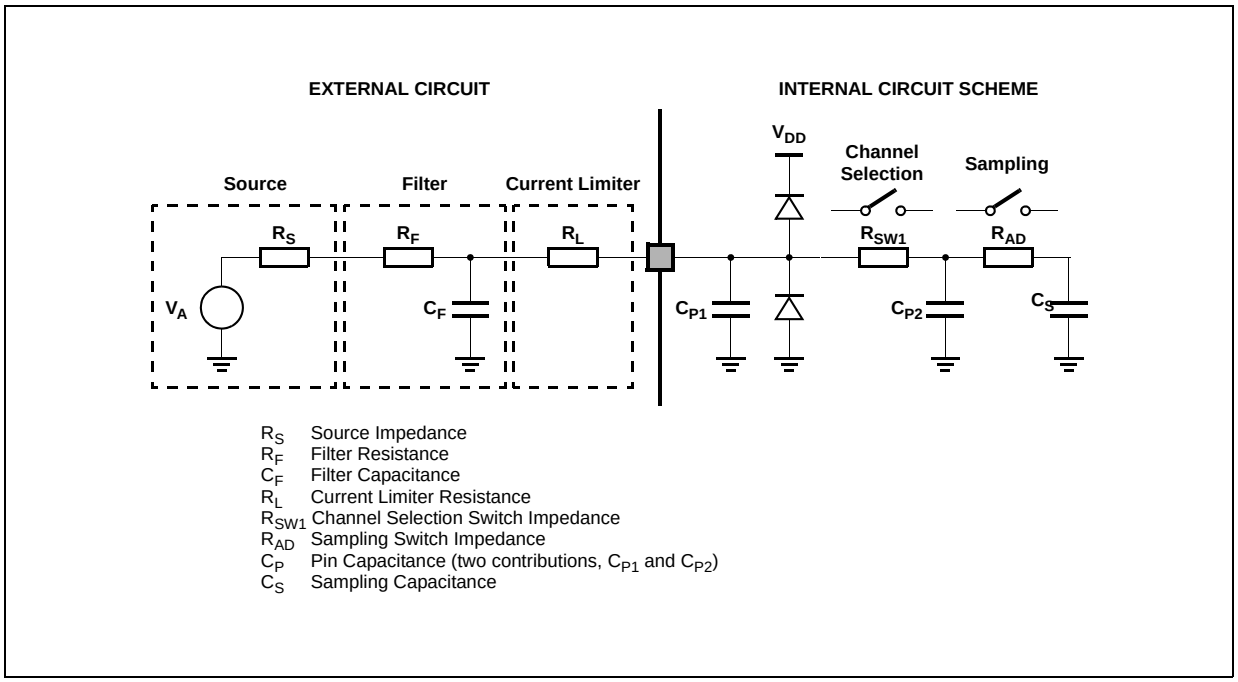


Figure 8. Input Equivalent Circuit

A second aspect involving the capacitance network shall be considered. Assuming the three capacitances C_F, C_{P1} and C_{P2} are initially charged at the source voltage V_A (refer to the equivalent circuit reported in Figure 8): A charge sharing phenomenon is installed when the sampling phase is started (A/D switch close).

4 During the sample time the input capacitance CS can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{sample}. After the end of the sample time t_{sample}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{sample} depend on programming.

5 This parameter does not include the sample time Tsample, but only the time for determining the digital result.

6 See Figure 8.

7 For the 144-pin package

8 No missing codes

3.16 Flash memory electrical characteristics

Table 26. Flash memory program and erase electrical specifications

No.	Symbol		Parameter	Typ[1]	Initial Max[2]	Lifetime Max[3]	Unit
1	$T_{DWPROGRAM}$	*[4]	Double word (64 bits) program time[4]	30	—	500	µs
2	$T_{PPROGRAM}$	*4	Page(128 bits) program time[4]	40	160	500	µs
3	$T_{16KPPERASE}$	*4	16 KB block pre-program and erase time	250	1000	5000	ms
4	$T_{48KPPERASE}$	*4	48 KB block pre-program and erase time	400	1500	5000	ms
5	$T_{64KPPERASE}$	*4	64 KB block pre-program and erase time	450	1800	5000	ms
6	$T_{128KPPERASE}$	*4	128 KB block pre-program and erase time	800	2600	7500	ms
7	$T_{256KPPERASE}$	*4	256 KB block pre-program and erase time	1400	5200	15000	ms

1 Typical program and erase times represent the median performance and assume nominal supply values and operation at 25C. These values are characterized, but not tested.I

2 Initial Max program and erase times provide guidance for time-out limits used in the factory and apply for <100 program/erase cycles, nominal supply values and operation at 25C. These values are verified at production test.

3 Lifetime Max program and erase times apply across the voltage, temperature, and cycling range of product life. These values are characterized, but not tested.

4 Program times are actual hardware programming times and do not include software overhead.

Table 27. Flash memory timing

Symbol		Parameter	Value			Unit
			Min	Typ	Max	
T_{RES}	D	Time from clearing the MCR-ESUS or PSUS bit with EHV = 1 until DONE goes low	—	—	100	ns
T_{DONE}	D	Time from 0 to 1 transition on the MCR-EHV bit initiating a program/erase until the MCR-DONE bit is cleared	—	—	5	ns
T_{PSRT}	D	Time between program suspend resume and the next program suspend request.[1]	100	—	—	µs
T_{ESRT}	D	Time between erase suspend resume and the next erase suspend request.[2]	10			ms

The reset sequences shown in Figure 15 and Figure 16 are triggered by functional reset events. $\overline{\text{RESET}}$ is driven low during these two reset sequences ***only if*** the corresponding functional reset source (which triggered the reset sequence) was enabled to drive $\overline{\text{RESET}}$ low for the duration of the internal reset sequence[1].

3.19.3 Reset sequence trigger mapping

The following table shows the possible trigger events for the different reset sequences. It specifies the reset sequence start conditions as well as the reset sequence end indications that are the basis for the timing data provided in Table 31.

Table 32. Reset sequence trigger — reset sequence

Reset Sequence Trigger	Reset Sequence Start Condition	Reset Sequence End Indication	Reset Sequence				
			Destructive Reset Sequence, BIST enabled[1]	*Destructive Reset Sequence, BIST disabled*[1]	*External Reset Sequence Long, BIST enabled*	*Functional Reset Sequence Long*	*Functional Reset Sequence Short*
All internal destructive reset sources (LVDs or internal HVD during power-up and during operation)	Section 3.19.4.1, Destructive reset	Release of $\overline{\text{RESET}}$[2]	triggers		cannot trigger	cannot trigger	cannot trigger
Assertion of $\overline{\text{RESET}}$[3]	Section 3.19.4.2, External reset via RESET		cannot trigger		triggers[4]	triggers[5]	triggers[6]
All internal functional reset sources configured for long reset	Sequence starts with internal reset trigger	Release of $\overline{\text{RESET}}$[7]	cannot trigger		cannot trigger	triggers	cannot trigger
All internal functional reset sources configured for short reset			cannot trigger		cannot trigger	cannot trigger	triggers

1 Whether BIST is executed or not depends on the chip configuration data stored in the shadow sector of the NVM.

2 End of the internal reset sequence (as specified in Table 31) can only be observed by release of $\overline{\text{RESET}}$ if it is not held low externally beyond the end of the internal sequence which would prolong the internal reset PHASE3 till $\overline{\text{RESET}}$ is released externally.

3 The assertion of $\overline{\text{RESET}}$ can only trigger a reset sequence if the device was running ($\overline{\text{RESET}}$ released) before. $\overline{\text{RESET}}$ does not gate a *Destructive Reset Sequence, BIST enabled* or a *Destructive Reset Sequence, BIST disabled*. However, it can prolong these sequences if $\overline{\text{RESET}}$ is held low externally beyond the end of the internal sequence (beyond PHASE3).

1.See RGM_FBRE register for more details.

4 If $\overline{\text{RESET}}$ is configured for long reset (default) and if BIST is enabled via chip configuration data stored in the shadow sector of the NVM.

5 If $\overline{\text{RESET}}$ is configured for long reset (default) and if BIST is disabled via chip configuration data stored in the shadow sector of the NVM.

6 If $\overline{\text{RESET}}$ is configured for short reset

7 Internal reset sequence can only be observed by state of $\overline{\text{RESET}}$ if bidirectional $\overline{\text{RESET}}$ functionality is enabled for the functional reset source which triggered the reset sequence.

3.19.4 Reset sequence — start condition

The impact of the voltage thresholds on the starting point of the internal reset sequence are becoming important if the voltage rails / signals ramp up with a very slow slew rate compared to the overall reset sequence duration.

3.19.4.1 Destructive reset

Figure 17 shows the voltage threshold that determines the start of the *Destructive Reset Sequence, BIST enabled* and the start for the *Destructive Reset Sequence, BIST disabled*.

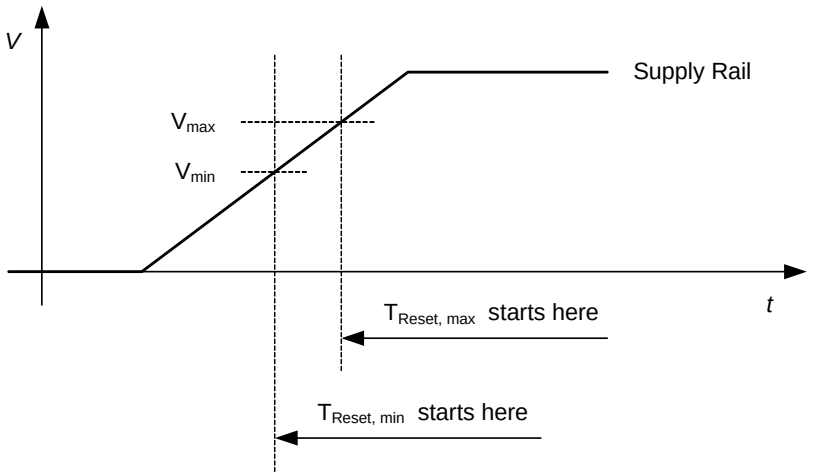


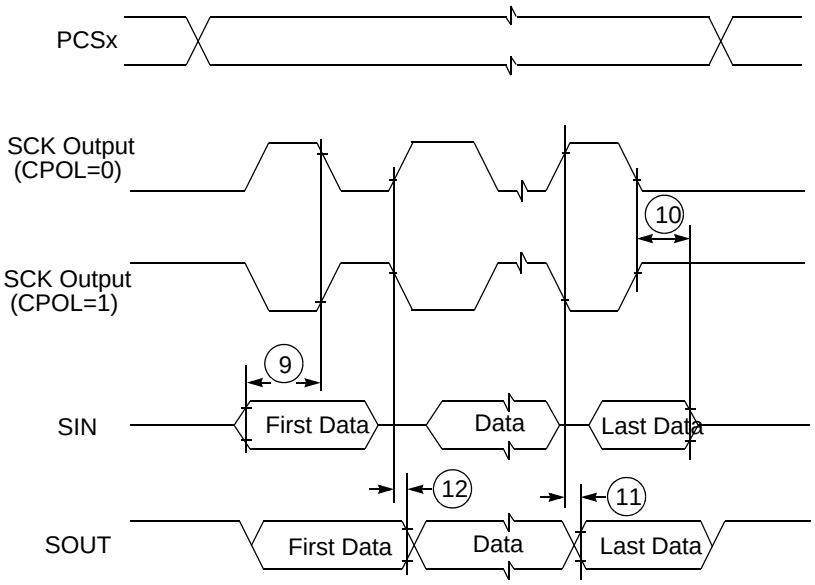
Figure 17. Reset sequence start for Destructive Resets

Table 33. Voltage Thresholds

Variable name	Value
V_{min}	Refer to Table 18
V_{max}	Refer to Table 18
Supply Rail	VDD_HV_PMU

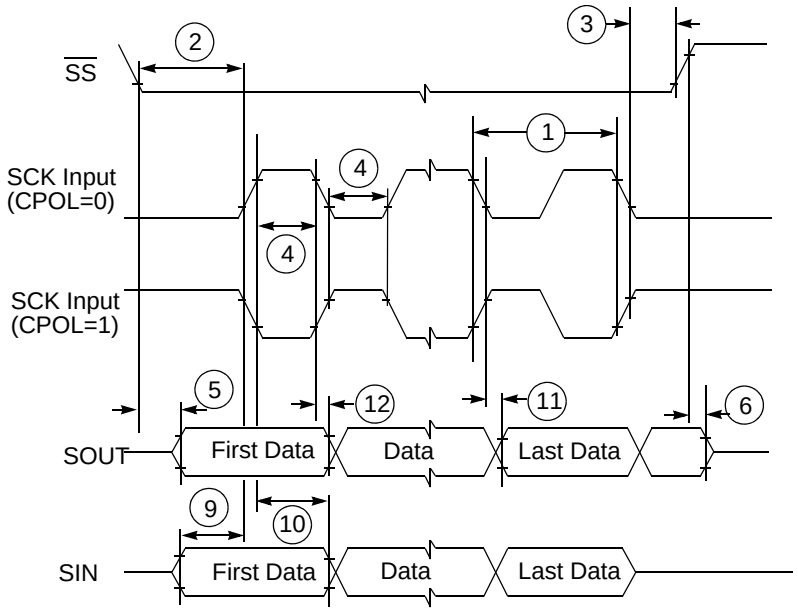
3.19.4.2 External reset via $\overline{\text{RESET}}$

Figure 18 shows the voltage thresholds that determine the start of the reset sequences initiated by the assertion of $\overline{\text{RESET}}$ as specified in Table 32.



Note: The numbers shown are referenced in Table 39.

Figure 31. DSPI classic SPI timing — master, CPHA = 1



Note: The numbers shown are referenced in Table 39.

Figure 32. DSPI classic SPI timing — slave, CPHA = 0

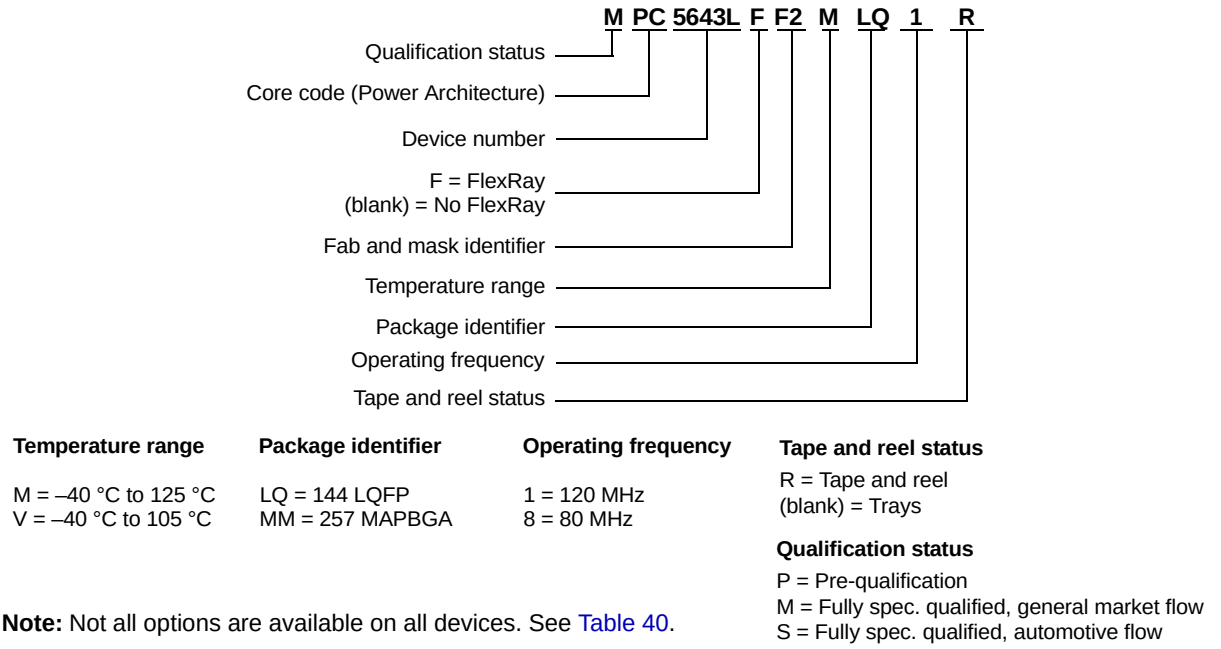
NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

TITLE: PBGA, LOW PROFILE, FINE PITCH, 257 I/O, 14 X 14 PKG, 0.8 MM PITCH (MAP)	CASE NUMBER: 2082–01
	STANDARD: JEDEC MO–275A–JJAC–1
	PACKAGE CODE: IN AGILE | SHEET: 2

Figure 42. 257 MAPBGA package mechanical drawing (2 of 2)

5 Ordering information



Note: Not all options are available on all devices. See Table 40.

Figure 43. Commercial product code structure

Table 40. Orderable part number summary

Part number[1]	Flash/SRAM	Package	Speed (MHz)[2]	Other features
SPC5643LFF2MLQ1	1 MB/128 KB	144 LQFP (Pb free)	120	FlexRay –40–125 °C
SPC5643LFF2MMM1	1 MB/128 KB	257 MAPBGA (Pb free)	120	FlexRay –40–125 °C
SPC5643LF2MLQ1	1 MB/128 KB	144 LQFP (Pb free)	120	No FlexRay –40–125 °C
SPC5643LF2MMM1	1 MB/128 KB	257 MAPBGA (Pb free)	120	No FlexRay –40–125 °C
SPC5643LFF2VLQ1	1 MB/128 KB	144 LQFP (Pb free)	120	FlexRay –40–105 °C
SPC5643LFF2VMM1	1 MB/128 KB	257 MAPBGA (Pb free)	120	FlexRay –40–105 °C
SPC5643LF2VLQ1	1 MB/128 KB	144 LQFP (Pb free)	120	No FlexRay –40–105 °C
SPC5643LF2VMM1	1 MB/128 KB	257 MAPBGA (Pb free)	120	No FlexRay –40–105 °C
SPC5643LFF2MLQ8	1 MB/128 KB	144 LQFP (Pb free)	80	FlexRay –40–125 °C
SPC5643LFF2MMM8	1 MB/128 KB	257 MAPBGA (Pb free)	80	FlexRay –40–125 °C

Table 41. Revision history (continued)

Revision	Date	Description of changes
6 (cont.)	11 Mar 2011 (cont.)	In the “ADC conversion characteristics” table: • Changed DNL min from -2 to -1. • Changed OFS min from -2 to -6. • Changed OFS max from 2 to 6. • Changed GNE min from -2 to -6. • Changed GNE max from 2 to 6. • Changed SNR min from 69 to 67. • Changed TUE min (without current injection) from -6 to -8. • Changed TUE max (without current injection) from 6 to 8. • Changed TUE min (with current injection) from -8 to -10. • Changed TUE max (with current injection) from 8 to 10.
7	25 Mar 2011	In the “Description” section, changed the first paragraph and its bullets to paragraph form only. In the “Voltage regulator electrical specifications“ table, changed the C_{V1V2} Min value from “—“ to 300 nF, and changed the Max value from 300 nF to 900 nF. In the “Supply current characteristics (cut2)“ table, corrected the “$I_{DD\_LV\_TYP}$ + $I_{DD\_LV\_PLL}$“ values as follows: • Changed the maximum value for “T_J = ambient“ from “279 mA+ 2.10 mA*f_{CPU}“ to “279 mA”. • Changed the maximum value for “T_J = 150 °C“ from “318 mA+ 2.30 mA*f_{CPU}“ to 318 mA. • Changed the frequency multiplier “f_{CPU}” in the max value to read “f_{CPU}[MHz]“ for “$I_{DD\_LV\_FULL}$ + $I_{DD\_LV\_PLL}$“ and “$I_{DD\_LV\_TYP}$ + $I_{DD\_LV\_PLL}$“. In the “JTAG pin AC electrical characteristics“ table: • Changed t_{JCYC} min from 100ns to 62.5ns. • Changed t_{JDC} units from “ns” to “%”. In the “Nexus debug port timing“ table: • Changed t_{TCYC} min from 40ns to 62.5 ns. • Changed t_{JOV} parameter description from “TCK Low to TDO Data Valid“ to “TCK Low to TDO/RDY Data Valid“. Changed “DDR” to “Double Data Rate (DDR)“ in the “Nexus DDR Mode output timing“ figure. Changed “TDO” to “TDO/RDY” in the “Nexus TDI, TMS, TDO timing“ figure. Removed “f_{max}” from the “DSPI timing” table.

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