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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | e200z4 |
| Core Size | 32-Bit Dual-Core |
| Speed | 80MHz |
| Connectivity | CANbus, FlexRay, LINbus, SPI, UART/USART |
| Peripherals | DMA, POR, PWM, WDT |
| Number of I/O | - |
| Program Memory Size | 1MB (1M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 128K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 5.5V |
| Data Converters | A/D 32x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 144-LQFP |
| Supplier Device Package | 144-LQFP (20x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5643lff0mlq8 |

**Table 1. MPC5643L device summary (continued)**

| Feature | | MPC5643L |
|---|---|---|
| Memory | Flash | 1 MB, ECC, RWW |
| | Static RAM (SRAM) | 128 KB, ECC |
| Modules | Interrupt Controller (INTC) | 16 interrupt levels, replicated module |
| | Periodic Interrupt Timer (PIT) | 1 × 4 channels |
| | System Timer Module (STM) | 1 × 4 channels, replicated module |
| | Software Watchdog Timer (SWT) | Yes, replicated module |
| | eDMA | 16 channels, replicated module |
| | FlexRay | 1 × 64 message buffers, dual channel |
| | FlexCAN | 2 × 32 message buffers |
| | LINFlexD (UART and LIN with DMA support) | 2 |
| | Clock out | Yes |
| | Fault Collection and Control Unit (FCCU) | Yes |
| | Cross Triggering Unit (CTU) | Yes |
| | eTimer | 3 × 6 channels[1] |
| | FlexPWM | 2 Module 4 × (2 + 1) channels[2] |
| | Analog-to-Digital Converter (ADC) | 2 × 12-bit ADC, 16 channels per ADC<br>(3 internal, 4 shared and 9 external) |
| | Sine Wave Generator (SWG) | 32 point |
| Modules (cont.) | Deserial Serial Peripheral Interface (DSPI) | 3 × DSPI<br>as many as 8 chip selects |
| | Cyclic Redundancy Checker (CRC) unit | Yes |
| | Junction temperature sensor (TSENS) | Yes, replicated module |
| | Digital I/Os | ≥ 16 |
| Supply | Device power supply | 3.3 V with integrated bypassable ballast transistor<br>External ballast transistor not needed for bare die |
| | Analog reference voltage | 3.0 V – 3.6 V and 4.5 V – 5.5 V |
| Clocking | Frequency-modulated phase-locked loop (FMPLL) | 2 |
| | Internal RC oscillator | 16 MHz |
| | External crystal oscillator | 4 – 40 MHz |
| Debug | Nexus | Level 3+ |

## 1.5.32 Sine Wave Generator (SWG)

A digital-to-analog converter is available to generate a sine wave based on 32 stored values for external devices (ex: resolver).

## 1.5.33 Analog-to-Digital Converter module (ADC)

The ADC module features include:

Analog part:

- 2 on-chip ADCs
  - 12-bit resolution SAR architecture
  - Same digital interface as in the MPC5604P family
  - A/D Channels: 9 external, 3 internal and 4 shared with other A/D (total 16 channels)
  - One channel dedicated to each T-sensor to enable temperature reading during application
  - Separated reference for each ADC
  - Shared analog supply voltage for both ADCs
  - One sample and hold unit per ADC
  - Adjustable sampling and conversion time

Digital part:

- 4 analog watchdogs comparing ADC results against predefined levels (low, high, range) before results are stored in the appropriate ADC result location
- 2 modes of operation: CPU Mode or CTU Mode
- CPU mode features
  - Register based interface with the CPU: one result register per channel
  - ADC state machine managing three request flows: regular command, hardware injected command, software injected command
  - Selectable priority between software and hardware injected commands
  - 4 analog watchdogs comparing ADC results against predefined levels (low, high, range)
  - DMA compatible interface
- CTU mode features
  - Triggered mode only
  - 4 independent result queues ($1 \times 16$ entries, $2 \times 8$ entries, $1 \times 4$ entries)
  - Result alignment circuitry (left justified; right justified)
  - 32-bit read mode allows to have channel ID on one of the 16-bit parts
  - DMA compatible interfaces
- Built-in self-test features triggered by software

## 1.5.34 Cross Triggering Unit (CTU)

The ADC cross triggering unit allows automatic generation of ADC conversion requests on user selected conditions without CPU load during the PWM period and with minimized CPU load for dynamic configuration.

The CTU implements the following features:

- Cross triggering between ADC, FlexPWM, eTimer, and external pins
- Double buffered trigger generation unit with as many as 8 independent triggers generated from external triggers
- Maximum operating frequency less than or equal to 120 MHz
- Trigger generation unit configurable in sequential mode or in triggered mode
- Trigger delay unit to compensate the delay of external low pass filter

**Table 4. 257 MAPBGA pin function summary (continued)**

| Pin # | Port/function | Peripheral | Output function | Input function |
|---|---|---|---|---|
| D11 | A[11] | SIUL | GPIO[11] | GPIO[11] |
| | | DSPI_2 | SCK | SCK |
| | | FlexPWM_0 | A[0] | A[0] |
| | | FlexPWM_0 | A[2] | A[2] |
| | | SIUL | — | EIRQ[10] |
| D12 | E[13] | SIUL | GPIO[77] | GPIO[77] |
| | | eTimer_0 | ETC[5] | ETC[5] |
| | | DSPI_2 | CS3 | — |
| | | SIUL | — | EIRQ[25] |
| D13 | F[15] | SIUL | GPIO[95] | GPIO[95] |
| | | LINFlexD_1 | — | RXD |
| D14 | $V_{DD\_HV\_IO\_RING}$ | — | | |
| D15 | $V_{PP\_TEST}$[1] | — | | |
| D16 | D[14] | SIUL | GPIO[62] | GPIO[62] |
| | | FlexPWM_0 | B[1] | B[1] |
| | | eTimer_0 | — | ETC[3] |
| D17 | G[3] | SIUL | GPIO[99] | GPIO[99] |
| | | FlexPWM_0 | A[2] | A[2] |
| | | eTimer_0 | — | ETC[4] |
| E1 | MDO0 | — | | |
| E2 | F[6] | SIUL | GPIO[86] | GPIO[86] |
| | | NPC | MDO[1] | — |
| E3 | D[1] | SIUL | GPIO[49] | GPIO[49] |
| | | eTimer_1 | ETC[2] | ETC[2] |
| | | CTU_0 | EXT_TGR | — |
| | | FlexRay | — | CA_RX |
| E4 | $\overline{NMI}$ | — | | |
| E14 | Not connected | — | | |
| E15 | C[14] | SIUL | GPIO[46] | GPIO[46] |
| | | eTimer_1 | ETC[2] | ETC[2] |
| | | CTU_0 | EXT_TGR | — |
| E16 | G[2] | SIUL | GPIO[98] | GPIO[98] |
| | | FlexPWM_0 | X[2] | X[2] |
| | | DSPI_1 | CS1 | — |

**Table 4. 257 MAPBGA pin function summary (continued)**

| Pin # | Port/function | Peripheral | Output function | Input function |
|---|---|---|---|---|
| K17 | A[3] | SIUL | GPIO[3] | GPIO[3] |
| | | eTimer_0 | ETC[3] | ETC[3] |
| | | DSPI_2 | CS0 | CS0 |
| | | FlexPWM_0 | B[3] | B[3] |
| | | MC_RGM | — | ABS[2] |
| | | SIUL | — | EIRQ[3] |
| L1 | F[10] | SIUL | GPIO[90] | GPIO[90] |
| | | NPC | $\overline{\text{EVTO}}$ | — |
| L2 | F[11] | SIUL | GPIO[91] | GPIO[91] |
| | | NPC | — | $\overline{\text{EVTI}}$ |
| L3 | D[9] | SIUL | GPIO[57] | GPIO[57] |
| | | FlexPWM_0 | X[0] | X[0] |
| | | LINFlexD_1 | TXD | — |
| L4 | Not connected | — | | |
| L6 | $V_{DD\_LV}$ | — | | |
| L7 | $V_{SS\_LV}$ | — | | |
| L8 | $V_{SS\_LV}$ | — | | |
| L9 | $V_{SS\_LV}$ | — | | |
| L10 | $V_{SS\_LV}$ | — | | |
| L11 | $V_{SS\_LV}$ | — | | |
| L12 | $V_{DD\_LV}$ | — | | |
| L14 | Not connected | — | | |
| L15 | TCK | — | | |
| L16 | H[4] | SIUL | GPIO[116] | GPIO[116] |
| | | FlexPWM_1 | X[0] | X[0] |
| | | eTimer_2 | ETC[0] | ETC[0] |
| L17 | B[4] | SIUL | GPIO[20] | GPIO[20] |
| | | JTAGC | TDO | — |
| M1 | $V_{DD\_HV\_OSC}$ | — | | |
| M2 | $V_{DD\_HV\_IO\_RING}$ | — | | |
| M3 | D[8] | SIUL | GPIO[56] | GPIO[56] |
| | | DSPI_1 | CS2 | — |
| | | eTimer_1 | ETC[4] | ETC[4] |
| | | DSPI_0 | CS5 | — |
| | | FlexPWM_0 | — | FAULT[3] |

**Table 7. Pin muxing (continued)**

| Port name | PCR | Peripheral | Alternate output function | Output mux sel | Input functions | Input mux select | Weak pull config during reset | Pad speed[1] | | Pin # | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | SRC = 1 | SRC = 0 | | 144 pkg | 257 pkg |
| A[5] | PCR[5] | SIUL | GPIO[5] | ALT0 | GPIO[5] | — | — | M | S | | 14 | H4 |
| | | DSPI_1 | CS0 | ALT1 | CS0 | — | | | | | | |
| | | eTimer_1 | ETC[5] | ALT2 | ETC[5] | PSMI[14]; PADSEL=0 | | | | | | |
| | | DSPI_0 | CS7 | ALT3 | — | — | | | | | | |
| | | SIUL | — | — | EIRQ[5] | — | | | | | | |
| A[6] | PCR[6] | SIUL | GPIO[6] | ALT0 | GPIO[6] | — | — | M | S | | 2 | G4 |
| | | DSPI_1 | SCK | ALT1 | SCK | — | | | | | | |
| | | SIUL | — | — | EIRQ[6] | — | | | | | | |
| A[7] | PCR[7] | SIUL | GPIO[7] | ALT0 | GPIO[7] | — | — | M | S | | 10 | F3 |
| | | DSPI_1 | SOUT | ALT1 | — | — | | | | | | |
| | | SIUL | — | — | EIRQ[7] | — | | | | | | |
| A[8] | PCR[8] | SIUL | GPIO[8] | ALT0 | GPIO[8] | — | — | M | S | | 12 | F4 |
| | | DSPI_1 | — | — | SIN | — | | | | | | |
| | | SIUL | — | — | EIRQ[8] | — | | | | | | |
| A[9] | PCR[9] | SIUL | GPIO[9] | ALT0 | GPIO[9] | — | — | M | S | | 134 | B6 |
| | | DSPI_2 | CS1 | ALT1 | — | — | | | | | | |
| | | FlexPWM_0 | B[3] | ALT3 | B[3] | PSMI[27]; PADSEL=1 | | | | | | |
| | | FlexPWM_0 | — | — | FAULT[0] | PSMI[16]; PADSEL=0 | | | | | | |

**Table 7. Pin muxing (continued)**

| Port name | PCR | Peripheral | Alternate output function | Output mux sel | Input functions | Input mux select | Weak pull config during reset | Pad speed[1] | | Pin # | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | SRC = 1 | SRC = 0 | | 144 pkg | 257 pkg |
| A[10] | PCR[10] | SIUL | GPIO[10] | ALT0 | GPIO[10] | — | — | M | S | | 118 | A13 |
| | | DSPI_2 | CS0 | ALT1 | CS0 | PSMI[3]; PADSEL=1 | | | | | | |
| | | FlexPWM_0 | B[0] | ALT2 | B[0] | PSMI[24]; PADSEL=0 | | | | | | |
| | | FlexPWM_0 | X[2] | ALT3 | X[2] | PSMI[29]; PADSEL=0 | | | | | | |
| | | SIUL | — | — | EIRQ[9] | — | | | | | | |
| A[11] | PCR[11] | SIUL | GPIO[11] | ALT0 | GPIO[11] | — | — | M | S | | 120 | D11 |
| | | DSPI_2 | SCK | ALT1 | SCK | PSMI[1]; PADSEL=1 | | | | | | |
| | | FlexPWM_0 | A[0] | ALT2 | A[0] | PSMI[20]; PADSEL=0 | | | | | | |
| | | FlexPWM_0 | A[2] | ALT3 | A[2] | PSMI[22]; PADSEL=0 | | | | | | |
| | | SIUL | — | — | EIRQ[10] | — | | | | | | |
| A[12] | PCR[12] | SIUL | GPIO[12] | ALT0 | GPIO[12] | — | — | M | S | | 122 | A10 |
| | | DSPI_2 | SOUT | ALT1 | — | — | | | | | | |
| | | FlexPWM_0 | A[2] | ALT2 | A[2] | PSMI[22]; PADSEL=1 | | | | | | |
| | | FlexPWM_0 | B[2] | ALT3 | B[2] | PSMI[26]; PADSEL=0 | | | | | | |
| | | SIUL | — | — | EIRQ[11] | — | | | | | | |

**Table 7. Pin muxing (continued)**

| Port name | PCR | Peripheral | Alternate output function | Output mux sel | Input functions | Input mux select | Weak pull config during reset | Pad speed[1] | | Pin # | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | SRC = 1 | SRC = 0 | | 144 pkg | 257 pkg |
| C[5] | PCR[37] | SIUL | GPIO[37] | ALT0 | GPIO[37] | — | — | M | S | | 13 | G3 |
| | | DSPI_0 | SCK | ALT1 | SCK | — | | | | | | |
| | | SSCM | DEBUG[5] | ALT3 | — | — | | | | | | |
| | | FlexPWM_0 | — | — | FAULT[3] | PSMI[19]; PADSEL=0 | | | | | | |
| | | SIUL | — | — | EIRQ[23] | — | | | | | | |
| C[6] | PCR[38] | SIUL | GPIO[38] | ALT0 | GPIO[38] | — | — | M | S | | 142 | D4 |
| | | DSPI_0 | SOUT | ALT1 | — | — | | | | | | |
| | | FlexPWM_0 | B[1] | ALT2 | B[1] | PSMI[25]; PADSEL=0 | | | | | | |
| | | SSCM | DEBUG[6] | ALT3 | — | — | | | | | | |
| | | SIUL | — | — | EIRQ[24] | — | | | | | | |
| C[7] | PCR[39] | SIUL | GPIO[39] | ALT0 | GPIO[39] | — | — | M | S | | 15 | K4 |
| | | FlexPWM_0 | A[1] | ALT2 | A[1] | PSMI[21]; PADSEL=0 | | | | | | |
| | | SSCM | DEBUG[7] | ALT3 | — | — | | | | | | |
| | | DSPI_0 | — | — | SIN | — | | | | | | |
| C[10] | PCR[42] | SIUL | GPIO[42] | ALT0 | GPIO[42] | — | — | M | S | | 111 | A15 |
| | | DSPI_2 | CS2 | ALT1 | — | — | | | | | | |
| | | FlexPWM_0 | A[3] | ALT3 | A[3] | PSMI[23]; PADSEL=1 | | | | | | |
| | | FlexPWM_0 | — | — | FAULT[1] | PSMI[17]; PADSEL=0 | | | | | | |
| C[11] | PCR[43] | SIUL | GPIO[43] | ALT0 | GPIO[43] | — | — | M | S | | 80 | M14 |
| | | eTimer_0 | ETC[4] | ALT1 | ETC[4] | PSMI[7]; PADSEL=1 | | | | | | |
| | | DSPI_2 | CS2 | ALT2 | — | — | | | | | | |

**Table 7. Pin muxing (continued)**

| Port name | PCR | Peripheral | Alternate output function | Output mux sel | Input functions | Input mux select | Weak pull config during reset | Pad speed[1] | | Pin # | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | SRC = 1 | SRC = 0 | | 144 pkg | 257 pkg |
| G[9] | PCR[105] | SIUL | GPIO[105] | ALT0 | GPIO[105] | — | — | M | S | | 79 | R17 |
| | | FlexRay | DBG1 | ALT1 | — | — | | | | | | |
| | | DSPI_1 | CS1 | ALT2 | — | — | | | | | | |
| | | FlexPWM_0 | — | — | FAULT[1] | PSMI[17]; PADSEL=2 | | | | | | |
| | | SIUL | — | — | EIRQ[29] | — | | | | | | |
| G[10] | PCR[106] | SIUL | GPIO[106] | ALT0 | GPIO[106] | — | — | M | S | | 77 | P15 |
| | | FlexRay | DBG2 | ALT1 | — | — | | | | | | |
| | | DSPI_2 | CS3 | ALT2 | — | — | | | | | | |
| | | FlexPWM_0 | — | — | FAULT[2] | PSMI[18]; PADSEL=1 | | | | | | |
| G[11] | PCR[107] | SIUL | GPIO[107] | ALT0 | GPIO[107] | — | — | M | S | | 75 | U15 |
| | | FlexRay | DBG3 | ALT1 | — | — | | | | | | |
| | | FlexPWM_0 | — | — | FAULT[3] | PSMI[19]; PADSEL=2 | | | | | | |
| G[12] | PCR[108] | SIUL | GPIO[108] | ALT0 | GPIO[108] | — | — | F | S | | — | F2 |
| | | NPC | MDO[11] | ALT2 | — | — | | | | | | |
| G[13] | PCR[109] | SIUL | GPIO[109] | ALT0 | GPIO[109] | — | — | F | S | | — | H1 |
| | | NPC | MDO[10] | ALT2 | — | — | | | | | | |
| G[14] | PCR[110] | SIUL | GPIO[110] | ALT0 | GPIO[110] | — | — | F | S | | — | A6 |
| | | NPC | MDO[9] | ALT2 | — | — | | | | | | |
| G[15] | PCR[111] | SIUL | GPIO[111] | ALT0 | GPIO[111] | — | — | F | S | | — | J2 |
| | | NPC | MDO[8] | ALT2 | — | — | | | | | | |
| Port H | | | | | | | | | | | | |
| H[0] | PCR[112] | SIUL | GPIO[112] | ALT0 | GPIO[112] | — | — | F | S | | — | A5 |
| | | NPC | MDO[7] | ALT2 | — | — | | | | | | |

**Table 7. Pin muxing (continued)**

| Port name | PCR | Peripheral | Alternate output function | Output mux sel | Input functions | Input mux select | Weak pull config during reset | Pad speed[1] | | Pin # | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | SRC = 1 | SRC = 0 | | 144 pkg | 257 pkg |
| H[1] | PCR[113] | SIUL | GPIO[113] | ALT0 | GPIO[113] | — | — | F | S | | — | F1 |
| | | NPC | MDO[6] | ALT2 | — | — | | | | | | |
| H[2] | PCR[114] | SIUL | GPIO[114] | ALT0 | GPIO[114] | — | — | F | S | | — | A4 |
| | | NPC | MDO[5] | ALT2 | — | — | | | | | | |
| H[3] | PCR[115] | SIUL | GPIO[115] | ALT0 | GPIO[115] | — | — | F | S | | — | G1 |
| | | NPC | MDO[4] | ALT2 | — | — | | | | | | |
| H[4] | PCR[116] | SIUL | GPIO[116] | ALT0 | GPIO[116] | — | — | M | S | | — | L16 |
| | | FlexPWM_1 | X[0] | ALT1 | X[0] | — | | | | | | |
| | | eTimer_2 | ETC[0] | ALT2 | ETC[0] | PSMI[39]; PADSEL=0 | | | | | | |
| H[5] | PCR[117] | SIUL | GPIO[117] | ALT0 | GPIO[117] | — | — | M | S | | — | M17 |
| | | FlexPWM_1 | A[0] | ALT1 | A[0] | — | | | | | | |
| | | DSPI_0 | CS4 | ALT3 | — | — | | | | | | |
| H[6] | PCR[118] | SIUL | GPIO[118] | ALT0 | GPIO[118] | — | — | M | S | | — | H17 |
| | | FlexPWM_1 | B[0] | ALT1 | B[0] | — | | | | | | |
| | | DSPI_0 | CS5 | ALT3 | — | — | | | | | | |
| H[7] | PCR[119] | SIUL | GPIO[119] | ALT0 | GPIO[119] | — | — | M | S | | — | K16 |
| | | FlexPWM_1 | X[1] | ALT1 | X[1] | — | | | | | | |
| | | eTimer_2 | ETC[1] | ALT2 | ETC[1] | PSMI[40]; PADSEL=0 | | | | | | |
| H[8] | PCR[120] | SIUL | GPIO[120] | ALT0 | GPIO[120] | — | — | M | S | | — | K15 |
| | | FlexPWM_1 | A[1] | ALT1 | A[1] | — | | | | | | |
| | | DSPI_0 | CS6 | ALT3 | — | — | | | | | | |
| H[9] | PCR[121] | SIUL | GPIO[121] | ALT0 | GPIO[121] | — | — | M | S | | — | G16 |
| | | FlexPWM_1 | B[1] | ALT1 | B[1] | — | | | | | | |
| | | DSPI_0 | CS7 | ALT3 | — | — | | | | | | |

**Table 14. EMI emission testing specifications**

| Symbol | | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{EME}$ | CC | Radiated emissions | Configuration A; frequency range 150 kHz–50 MHz | — | 16 | — | dBµV |
| | | | Configuration A; frequency range 50–150 MHz | — | 16 | — | |
| | | | Configuration A; frequency range 150–500 MHz | — | 32 | — | |
| | | | Configuration A; frequency range 500–1000 MHz | — | 25 | — | |
| | | | Configuration B; frequency range 50–150 MHz | — | 15 | — | |
| | | | Configuration B; frequency range 50–150 MHz | — | 21 | — | |
| | | | Configuration B; frequency range 150–500 MHz | — | 30 | — | |
| | | | Configuration B; frequency range 500–1000 MHz | — | 24 | — | |

EMC testing was performed and documented according to these standards: [IEC61508-2-7.4.5.1.b, IEC61508-2-7.2.3.2.e, IEC61508-2-Table-A.17 (partially), IEC61508-2-Table-B.5(partially),SRS2110]

EME testing was performed and documented according to these standards: [IEC 61967-2 & -4]

EMS testing was performed and documented according to these standards: [IEC 62132-2 & -4]

Refer MPC5643L for detailed information pertaining to the EMC, EME, and EMS testing and results.

## 3.6 Electrostatic discharge (ESD) characteristics

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × ($n$ + 1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard.

**Table 15. ESD ratings[1, 2]**

| No. | Symbol | | Parameter | Conditions | Class | Max value[3] | Unit |
|---|---|---|---|---|---|---|---|
| 1 | $V_{ESD(HBM)}$ | SR | Electrostatic discharge (Human Body Model) | $T_A$ = 25 °C conforming to AEC-Q100-002 | H1C | 2000 | V |
| 2 | $V_{ESD(MM)}$ | SR | Electrostatic discharge (Machine Model) | $T_A$ = 25 °C conforming to AEC-Q100-003 | M2 | 200 | V |
| 3 | $V_{ESD(CDM)}$ | SR | Electrostatic discharge (Charged Device Model) | $T_A$ = 25 °C conforming to AEC-Q100-011 | C3A | 500<br>750 (corners) | V |

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

[2] Adjust resistor at bipolar transistor collector for 3.3V to avoid VCE<$VCE_{SAT}$

The recommended external ballast transistor is the bipolar transistor BCP68 with the gain range of 85 up to 375 (for IC=500mA, VCE=1V) provided by several suppliers. This includes the gain variations BCP68-10, BCP68-16 and BCP68-25.The most important parameters for the interoperability with the integrated voltage regulator are the DC current gain (hFE) and the temperature coefficient of the gain (XTB). While the specified gain range of most BCP68 vendors is the same, there are slight variations in the temperature coefficient parameter. MPC5643L Voltage regulator operation was simulated against the typical variation on temperature coefficient and against the specified gain range to have a robust design.

**Table 18. Voltage regulator electrical specifications**

| Symbol | | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| | $C_{ext}$ | External decoupling/ stability capacitor | Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations. | 12 | — | 40 | µF |
| | SR | Combined ESR of external capacitor | — | 1 | — | 100 | mΩ |
| | SR | Number of pins for external decoupling/ stability capacitor | — | 5 | — | — | — |
| $C_{V1V2}$ | SR | Total capacitance on 1.2 V pins | Ceramic capacitors, taking into account tolerance, aging, voltage and temperature variation | 300 | — | 900 | nF |
| $t_{SU}$ | | Start-up time after main supply stabilization | $C_{load}$ = 10 µF × 4 | — | — | 2.5 | ms |
| — | | Main High Voltage Power - Low Voltage Detection, upper threshold | — | — | — | 2.93 | V |
| — | D | Main supply low voltage detector, lower threshold | — | 2.6 | — | — | V |
| — | D | Digital supply high voltage detector upper threshold | Before a destructive reset initialization phase completion | 1.355 | — | 1.495 | V |
| | | | After a destructive reset initialization phase completion | 1.39 | — | 1.47 | |
| — | D | Digital supply high voltage detector lower threshold | Before a destructive reset initialization phase completion | 1.315 | — | 1.455 | V |
| | | | After a destructive reset initialization phase completion | 1.35 | — | 1.38 | |

**Table 23. FMPLL electrical characteristics (continued)**

| Symbol | | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $t_{lpll}$ | D | FMPLL lock time [6, 7] | — | — | — | 200 | µs |
| $t_{dc}$ | D | Duty cycle of reference | — | 40 | — | 60 | % |
| $C_{JITTER}$ | T | CLKOUT period jitter[8,9,10,11] | Long-term jitter (avg. over 2 ms interval), $f_{FMPLLOUT}$ maximum | –6 | — | 6 | ns |
| $\Delta t_{PKJIT}$ | T | Single period jitter (peak to peak) | PHI @ 120 MHz, Input clock @ 4 MHz | — | — | 175 | ps |
| | | | PHI @ 100 MHz, Input clock @ 4 MHz | — | — | 185 | ps |
| | | | PHI @ 80 MHz, Input clock @ 4 MHz | — | — | 200 | ps |
| $\Delta t_{LTJIT}$ | T | Long term jitter | PHI @ 16 MHz, Input clock @ 4 MHz | — | — | ±6 | ns |
| $f_{LCK}$ | D | Frequency LOCK range | — | –6 | — | 6 | % $f_{FMPLLOUT}$ |
| $f_{UL}$ | D | Frequency un-LOCK range | — | –18 | — | 18 | % $f_{FMPLLOUT}$ |
| $f_{CS}$ $f_{DS}$ | D | Modulation depth | Center spread | ±0.25 | — | ±2.0 | % $f_{FMPLLOUT}$ |
| | | | Down spread | –0.5 | — | -8.0 | |
| $f_{MOD}$ | D | Modulation frequency[12] | — | — | — | 100 | kHz |

1 Considering operation with FMPLL not bypassed.

2 With FM; the value does not include a possible +2% modulation

3 “Loss of Reference Frequency” window is the reference frequency range outside of which the FMPLL is in self clocked mode.

4 Self clocked mode frequency is the frequency that the FMPLL operates at when the reference frequency falls outside the $f_{LOR}$ window.

5 $f_{VCO}$ is the frequency at the output of the VCO; its range is 256–512 MHz.
$f_{SCM}$ is the self-clocked mode frequency (free running frequency); its range is 20–150 MHz.
$f_{SYS} = f_{VCO} \div ODF$

6 This value is determined by the crystal manufacturer and board design. For 4 MHz to 20 MHz crystals specified for this FMPLL, load capacitors should not exceed these limits.

7 This specification applies to the period required for the FMPLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR).

8 This value is determined by the crystal manufacturer and board design.

9 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum $f_{SYS}$. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FMPLL circuitry via $V_{DDPLL}$ and $V_{SSPLL}$ and variation in crystal oscillator frequency increase the $C_{JITTER}$ percentage for a given interval.

10 Proper PC board layout procedures must be followed to achieve specifications.

11 Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of $C_{JITTER}$ and either $f_{CS}$ or $f_{DS}$ (depending on whether center spread or down spread modulation is enabled).

12 Modulation depth is attenuated from depth setting when operating at modulation frequencies above 50 kHz.

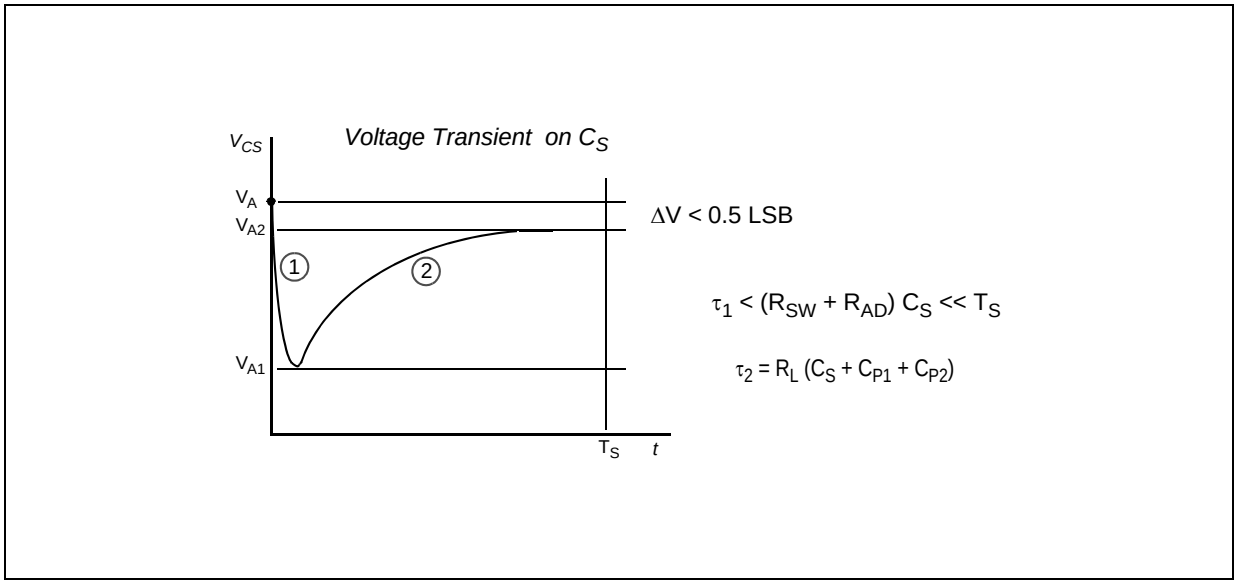



**Figure 9. Transient Behavior during Sampling Phase**

In particular two different transient periods can be distinguished:

- A first and quick charge transfer from the internal capacitance $C_{P1}$ and $C_{P2}$ to the sampling capacitance $C_S$ occurs ($C_S$ is supposed initially completely discharged): considering a worst case (since the time constant in reality would be faster) in which $C_{P2}$ is reported in parallel to $C_{P1}$ (call $C_P = C_{P1} + C_{P2}$), the two capacitances $C_P$ and $C_S$ are in series, and the time constant is

$$\tau_1 = (R_{SW} + R_{AD}) \bullet \frac{C_P \bullet C_S}{C_P + C_S} \qquad \textit{Eqn. 5}$$

  Equation 5 can again be simplified considering only $C_S$ as an additional worst condition. In reality, the transient is faster, but the A/D converter circuitry has been designed to be robust also in the very worst case: the sampling time $T_S$ is always much longer than the internal time constant:

$$\tau_1 < (R_{SW} + R_{AD}) \bullet C_S \ll T_S \qquad \textit{Eqn. 6}$$

  The charge of $C_{P1}$ and $C_{P2}$ is redistributed also on $C_S$, determining a new value of the voltage $V_{A1}$ on the capacitance according to Equation 7:

$$V_{A1} \bullet (C_S + C_{P1} + C_{P2}) = V_A \bullet (C_{P1} + C_{P2}) \qquad \textit{Eqn. 7}$$

- A second charge transfer involves also $C_F$ (that is typically bigger than the on-chip capacitance) through the resistance $R_L$: again considering the worst case in which $C_{P2}$ and $C_S$ were in parallel to $C_{P1}$ (since the time constant in reality would be faster), the time constant is:

$$\tau_2 < R_L \bullet (C_S + C_{P1} + C_{P2}) \qquad \textit{Eqn. 8}$$

  In this case, the time constant depends on the external circuit: in particular imposing that the transient is completed well before the end of sampling time $T_S$, a constraints on $R_L$ sizing is obtained:

$$10 \bullet \tau_2 = 10 \bullet R_L \bullet (C_S + C_{P1} + C_{P2}) < T_S \qquad \textit{Eqn. 9}$$

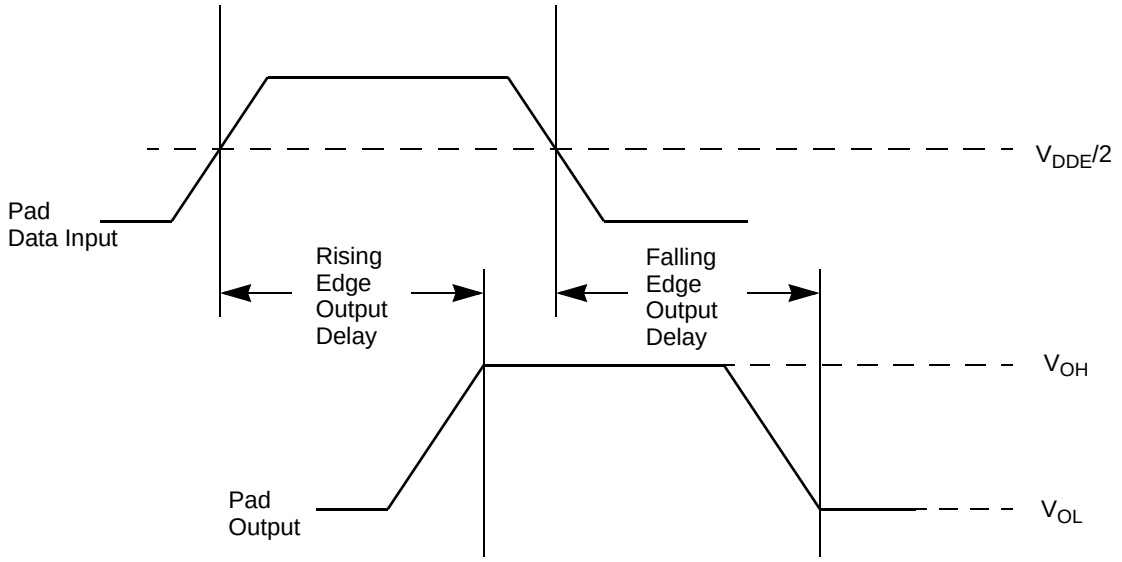



**Figure 11. Pad output delay**

## 3.19 Reset sequence

This section shows the duration for different reset sequences. It describes the different reset sequences and it specifies the start conditions and the end indication for the reset sequences.

### 3.19.1 Reset sequence duration

Table 31 specifies the minimum and the maximum reset sequence duration for the five different reset sequences described in Section 3.19.2, Reset sequence description.

**Table 31. RESET sequences**

| No. | Symbol | | Parameter | Conditions | $T_{Reset}$ | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max[1] | |
| 1 | $T_{DRB}$ | CC | Destructive Reset Sequence, BIST enabled | | 28 | 34 | 39 | ms |
| 2 | $T_{DR}$ | CC | Destructive Reset Sequence, BIST disabled | — | 500 | 4200 | 5000 | µs |
| 3 | $T_{ERLB}$ | CC | External Reset Sequence Long, BIST enabled | | 28 | 32 | 37 | ms |
| 4 | $T_{FRL}$ | CC | Functional Reset Sequence Long | — | 35 | 150 | 400 | µs |
| 5 | $T_{FRS}$ | CC | Functional Reset Sequence Short | — | 1 | 4 | 10 | µs |

1 The maximum value is applicable only if the reset sequence duration is not prolonged by an extended assertion of $\overline{\text{RESET}}$ by an external reset generator.

### 3.19.2 Reset sequence description

The figures in this section show the internal states of the chip during the five different reset sequences. The doted lines in the figures indicate the starting point and the end point for which the duration is specified in Table 31. The start point and end point

conditions as well as the reset trigger mapping to the different reset sequences is specified in Section 3.19.3, Reset sequence trigger mapping.

With the beginning of DRUN mode the first instruction is fetched and executed. At this point application execution starts and the internal reset sequence is finished.

The figures below show the internal states of the chip during the execution of the reset sequence and the possible states of the signal pin $\overline{\text{RESET}}$.

## NOTE

$\overline{\text{RESET}}$ is a bidirectional pin. The voltage level on this pin can either be driven low by an external reset generator or by the chip internal reset circuitry. A high level on this pin can only be generated by an external pull up resistor which is strong enough to overdrive the weak internal pull down resistor. The rising edge on $\overline{\text{RESET}}$ in the following figures indicates the time when the device stops driving it low. The reset sequence durations given in table Table 31 are applicable only if the internal reset sequence is not prolonged by an external reset generator keeping $\overline{\text{RESET}}$ asserted low beyond the last PHASE3.

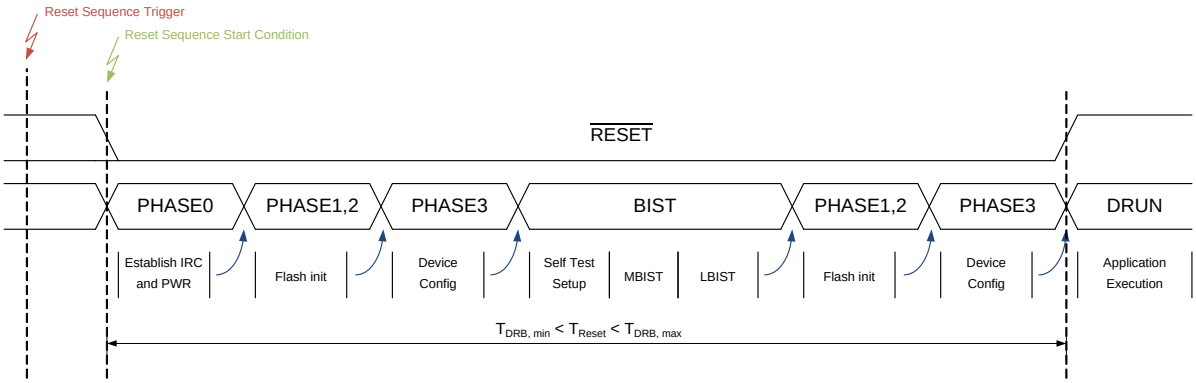



**Figure 12. Destructive Reset Sequence, BIST enabled**

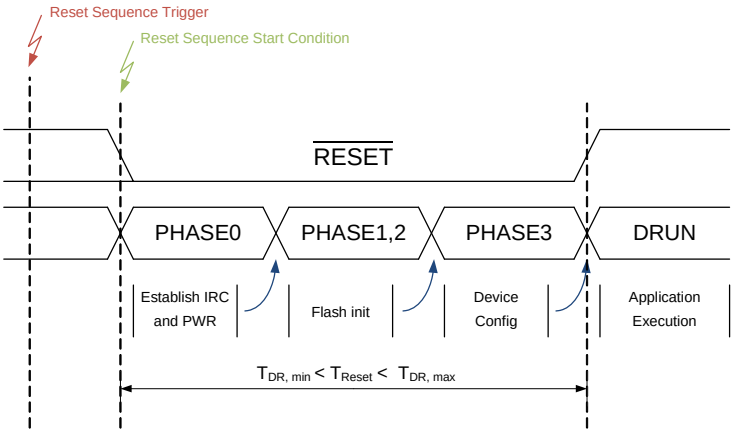



**Figure 13. Destructive Reset Sequence, BIST disabled**

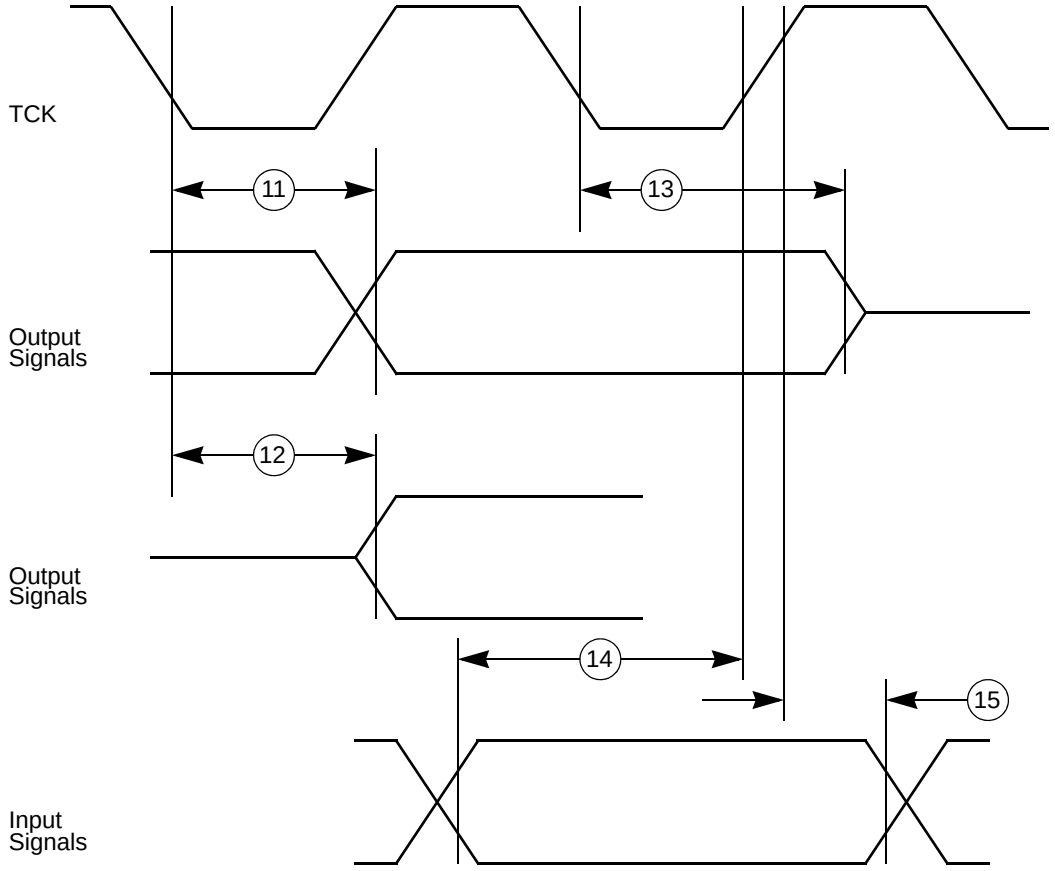



**Figure 24. JTAG boundary scan timing**

## 3.20.4 Nexus timing

**Table 37. Nexus debug port timing[1]**

| No. | Symbol | | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|---|---|
| 1 | $t_{MCYC}$ | D | MCKO Cycle Time | — | 15.6 | — | ns |
| 2 | $t_{MDC}$ | D | MCKO Duty Cycle | — | 40 | 60 | % |
| 3 | $t_{MDOV}$ | D | MCKO Low to MDO, $\overline{\text{MSEO}}$, $\overline{\text{EVTO}}$ Data Valid[2] | — | –0.1 | 0.25 | $t_{MCYC}$ |
| 4 | $t_{EVTIPW}$ | D | $\overline{\text{EVTI}}$ Pulse Width | — | 4.0 | — | $t_{TCYC}$ |
| 5 | $t_{EVTOPW}$ | D | $\overline{\text{EVTO}}$ Pulse Width | — | 1 | | $t_{MCYC}$ |
| 6 | $t_{TCYC}$ | D | TCK Cycle Time[3] | — | 62.5 | — | ns |
| 7 | $t_{TDC}$ | D | TCK Duty Cycle | — | 40 | 60 | % |
| 8 | $t_{NTDIS}$, $t_{NTMSS}$ | D | TDI, TMS Data Setup Time | — | 8 | — | ns |
| 9 | $t_{NTDIH}$, $t_{NTMSH}$ | D | TDI, TMS Data Hold Time | | 5 | — | ns |
| 10 | $t_{JOV}$ | D | TCK Low to TDO/RDY Data Valid | | 0 | 25 | ns |

1 JTAG specifications in this table apply when used for debug functionality. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal.

2 For all Nexus modes except DDR mode, MDO, $\overline{\text{MSEO}}$, and $\overline{\text{EVTO}}$ data is held valid until next MCKO low cycle.

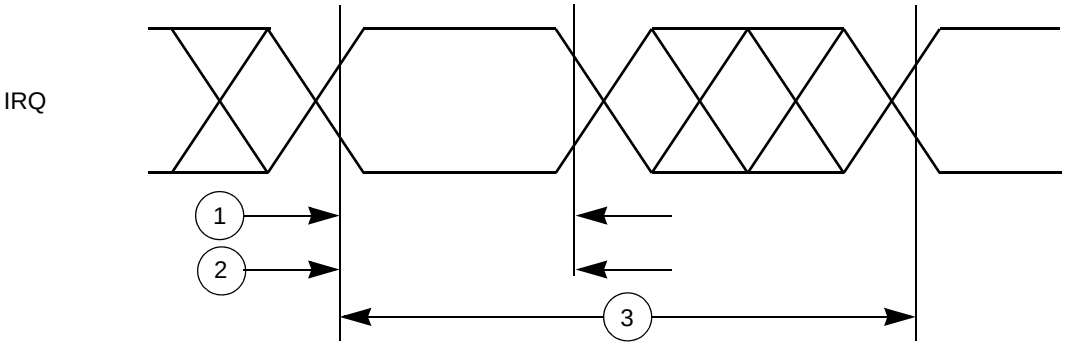



**Figure 29. External interrupt timing**

## 3.20.6 DSPI timing

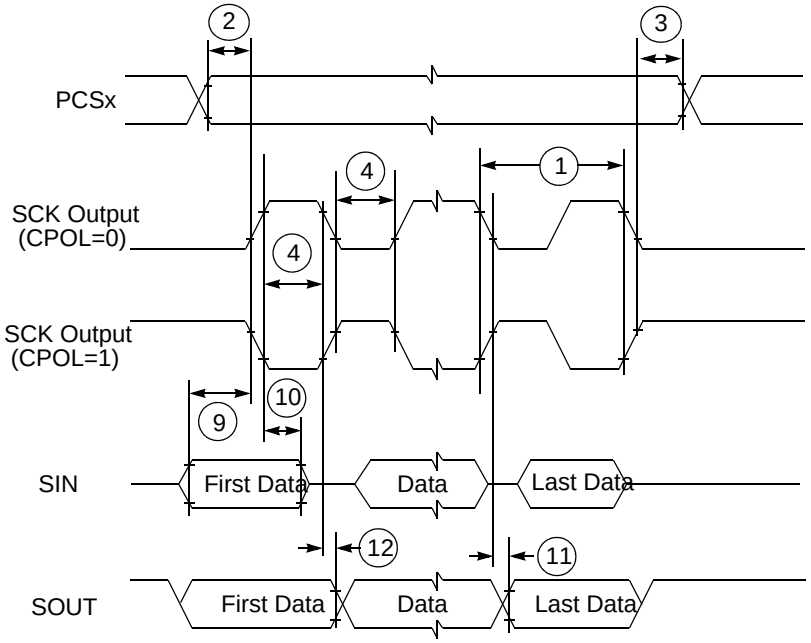
**Table 39. DSPI timing**

| No. | Symbol | | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|---|---|
| 1 | $t_{SCK}$ | D | DSPI cycle time | Master (MTFE = 0) | 62 | — | ns |
| | | D | | Slave (MTFE = 0) | 62 | — | |
| | | D | | Slave Receive Only Mode[1] | 16 | — | |
| 2 | $t_{CSC}$ | D | PCS to SCK delay | — | 16 | — | ns |
| 3 | $t_{ASC}$ | D | After SCK delay | — | 16 | — | ns |
| 4 | $t_{SDC}$ | D | SCK duty cycle | — | $t_{SCK}/2$ - 10 | $t_{SCK}/2$ + 10 | ns |
| 5 | $t_A$ | D | Slave access time | $\overline{SS}$ active to SOUT valid | — | 40 | ns |
| 6 | $t_{DIS}$ | D | Slave SOUT disable time | $\overline{SS}$ inactive to SOUT High-Z or invalid | — | 10 | ns |
| 7 | $t_{PCSC}$ | D | PCSx to $\overline{PCSS}$ time | — | 13 | — | ns |
| 8 | $t_{PASC}$ | D | $\overline{PCSS}$ to PCSx time | — | 13 | — | ns |
| 9 | $t_{SUI}$ | D | Data setup time for inputs | Master (MTFE = 0) | 20 | — | ns |
| | | | | Slave | 2 | — | |
| | | | | Master (MTFE = 1, CPHA = 0) | 5 | — | |
| | | | | Master (MTFE = 1, CPHA = 1) | 20 | — | |
| 10 | $t_{HI}$ | D | Data hold time for inputs | Master (MTFE = 0) | –5 | — | ns |
| | | | | Slave | 4 | — | |
| | | | | Master (MTFE = 1, CPHA = 0) | 11 | — | |
| | | | | Master (MTFE = 1, CPHA = 1) | –5 | — | |
| 11 | $t_{SUO}$ | D | Data valid (after SCK edge) | Master (MTFE = 0) | — | 4 | ns |
| | | | | Slave | — | 23 | |
| | | | | Master (MTFE = 1, CPHA = 0) | — | 12 | |
| | | | | Master (MTFE = 1, CPHA = 1) | — | 4 | |

**Table 39. DSPI timing (continued)**

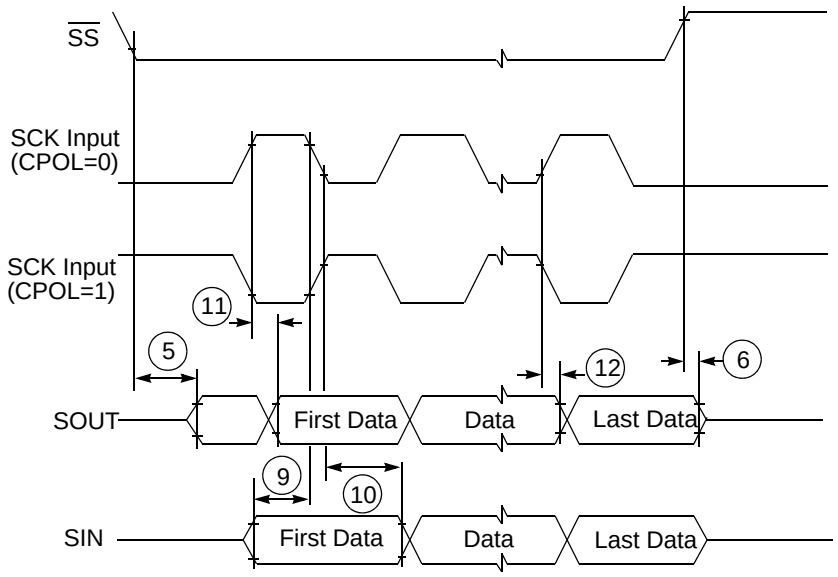
| No. | Symbol | | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|---|---|
| 12 | $t_{HO}$ | D | Data hold time for outputs | Master (MTFE = 0) | –2 | — | ns |
| | | | | Slave | 6 | — | |
| | | | | Master (MTFE = 1, CPHA = 0) | 6 | — | |
| | | | | Master (MTFE = 1, CPHA = 1) | –2 | — | |

1 Slave Receive Only Mode can operate at a maximum frequency of 60 MHz. In this mode, the DSPI can receive data on SIN, but no valid data is transmitted on SOUT.



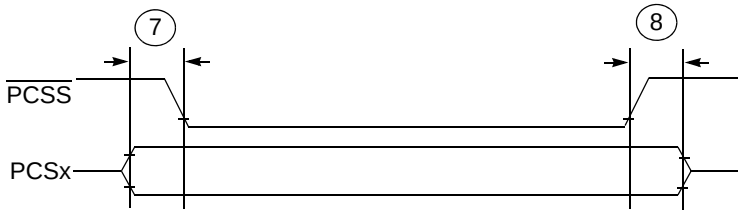

**Note:** The numbers shown are referenced in Table 39.

**Figure 30. DSPI classic SPI timing — master, CPHA = 0**




**Note:** The numbers shown are referenced in Table 39.

**Figure 37. DSPI modified transfer format timing — slave, CPHA = 1**




**Note:** The numbers shown are referenced in Table 39.

**Figure 38. DSPI PCS strobe ($\overline{\text{PCSS}}$) timing**

# 4 Package characteristics

## 4.1 Package mechanical data

**Table 41. Revision history (continued)**

| Revision | Date | Description of changes |
|---|---|---|
| 8 | 27 April 2012 | Editorial changes.<br>In the “Device comparison” section, changed “Ambient temperature range using external ballast transistor (BGA)“ from TBD to “–40 to 125 °C“.<br>In the “Block diagram” section, removed one PMU from the figure.<br>In the 257-pin pinout figure, changed cut2 to cut2/3 in Notes.<br>In the pin function summary table, changed cut2 to cut2/3.<br>In the “System pins” table:<br>• Added Note regarding Open Drain Enable.<br>• Added description to RESET pin.<br>In the pin-muxing table:<br>• Added Note about Open Drain.<br>• Changed cut2 to cut2/3.<br>• Changed all entries of column 'Weak pull config during reset’ to ' - ' , except for PCR[2], PCR[3], PCR[4] and PCR[21].<br>In the “Absolute maximum ratings” table:<br>• Removed the “$V_{SS\_HV\_REG}$” row.<br>• Added the footnote “Internal structures hold the input voltage...” to the $V_{IN}$ maximum specifications.<br>In the “ conditions” table, removed the “$V_{SS\_HV\_REG}$” row.<br>In the “Thermal characteristics” section:<br>• Added the “Thermal characteristics for 100 LQFP package“ table.<br>• Updated values and footnote 1 in the 144 package table.<br>• Updated footnote 1 in the 257 package table.<br>In the “Supply current characteristics“ table:<br>• Added footnote 1 to parameter “$I_{DD\_LV\_TYP}$ + $I_{DD\_LV\_PLL}$“ (symbol “T”).<br>• Changed “$I_{DD\_LV\_STOP}$” at 150C from 80mA to 72mA.<br>• Changed “$I_{DD\_LV\_HALT}$” at 150C from 72mA to 80mA.<br>In the “FMPLL electrical characteristics” table:<br>• Deleted the footnote “This value is true when operating at frequencies above 60 MHz...” from the specification for $f_{CS}$ and $f_{DS}$.<br>• Changed “$f_{SYS}$” to “$f_{FMPLLOUT}$” in the entries for the $C_{JITTER}$, $f_{LCK}$, $f_{UL}$, $f_{CS}$, and $f_{DS}$ specifications.<br>In the “ADC conversion characteristics” table:<br>• Revised the entry for $TUE_{IS1WINJ}$ (was P/T and “Total unadjusted error for IS1WINJ”, is T and “Total unadjusted error for IS1WINJ (single ADC channels)”).<br>• Revised the entry for $TUE_{IS1WWINJ}$ (was “Total unadjusted error for IS1WWINJ”, is “Total unadjusted error for IS1WWINJ (double ADC channels)”).<br>In the “Temperature sensor electrical characteristics“ table, for $T_J = T_A$ to 125 °C, changed Min/Max from values -7/+7 to -10/+10.<br>In the “Input Impedance and ADC Accuracy“ section:<br>• Changed $C_S$ in the text from 3 pF to 7.5 pF.<br>• Changed $R_{eq}$ in the text from 330 kΩ to 133 kΩ.<br>• Removed $R_L$, $R_{SW}$, and $R_{AD}$ from the external network design constraint equation and the sentence immediately preceding it.<br>• Changed the $C_F$ constraint value equation constant from 2048 to 8192.<br>• In the “ADC conversion characteristics“ table, changed INL Min/Max values from -2/+2 to -3/+3. |