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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Dual-Core
Speed	64MHz
Connectivity	CANbus, FlexRay, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	-
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=spc5643lff2mll6

Table 1. MPC5643L device summary (continued)

Feature		MPC5643L
Packages	LQFP	144 pins
	MAPBGA	257 MAPBGA
Temperature	Temperature range (junction)	–40 to 150 °C
	Ambient temperature range using external ballast transistor (LQFP)	–40 to 125 °C
	Ambient temperature range using external ballast transistor (BGA)	–40 to 125 °C

1 The third eTimer (eTimer_2) is available with external I/O access only in the BGA package, on the LQFP package eTimer_2 is available internally only without any external I/O access.

2 The second FlexPWM module is available only in the BGA package.

1.4 Block diagram

Figure 1 shows a top-level block diagram of the MPC5643L device.

- Single-cycle read responses (0 AHB data-phase wait states) for hits in the buffers. The buffers implement a least-recently-used replacement algorithm to maximize performance.
- Programmable response for read-while-write sequences including support for stall-while-write, optional stall notification interrupt, optional flash operation abort , and optional abort notification interrupt.
- Separate and independent configurable access timing (on a per bank basis) to support use across a wide range of platforms and frequencies.
- Support of address-based read access timing for emulation of other memory types.
- Support for reporting of single- and multi-bit error events.
- Typical operating configuration loaded into programming model by system reset.

The platform flash controller is replicated for each processor.

1.5.8 Platform Static RAM Controller (SRAMC)

The SRAMC module is the platform SRAM array controller, with integrated error detection and correction.

The main features of the SRAMC provide connectivity for the following interfaces:

- XBAR Slave Port (64-bit data path)
- ECSM (ECC Error Reporting, error injection and configuration)
- SRAM array

The following functions are implemented:

- ECC encoding (32-bit boundary for data and complete address bus)
- ECC decoding (32-bit boundary and entire address)
- Address translation from the AHB protocol on the XBAR to the SRAM array

The platform SRAM controller is replicated for each processor.

1.5.9 Memory subsystem access time

Every memory access the CPU performs requires at least one system clock cycle for the data phase of the access. Slower memories or peripherals may require additional data phase wait states. Additional data phase wait states may also occur if the slave being accessed is not parked on the requesting master in the crossbar.

Table 2 shows the number of additional data phase wait states required for a range of memory accesses.

Table 2. Platform memory access time summary

AHB transfer	Data phase wait states	Description
e200z4d instruction fetch	0	Flash memory prefetch buffer hit (page hit)
e200z4d instruction fetch	3	Flash memory prefetch buffer miss (based on 4-cycle random flash array access time)
e200z4d data read	0–1	SRAM read
e200z4d data write	0	SRAM 32-bit write

Table 2. Platform memory access time summary (continued)

AHB transfer	Data phase wait states	Description
e200z4d data write	0	SRAM 64-bit write (executed as 2 x 32-bit writes)
e200z4d data write	0–2	SRAM 8-,16-bit write (Read-modify-Write for ECC)
e200z4d flash memory read	0	Flash memory prefetch buffer hit (page hit)
e200z4d flash memory read	3	Flash memory prefetch buffer miss (at 120 MHz; includes 1 cycle of program flash memory controller arbitration)

1.5.10 Error Correction Status Module (ECSM)

The ECSM on this device manages the ECC configuration and reporting for the platform memories (flash memory and SRAM). It does not implement the actual ECC calculation. A detected error (double error for flash memory or SRAM) is also reported to the FCCU. The following errors and indications are reported into the ECSM dedicated registers:

- ECC error status and configuration for flash memory and SRAM
- ECC error reporting for flash memory
- ECC error reporting for SRAM
- ECC error injection for SRAM

1.5.11 Peripheral bridge (PBRIDGE)

The PBRIDGE implements the following features:

- Duplicated periphery
- Master access privilege level per peripheral (per master: read access enable; write access enable)
- Checker applied on PBRIDGE output toward periphery
- Byte endianess swap capability

1.5.12 Interrupt Controller (INTC)

The INTC provides priority-based preemptive scheduling of interrupt requests, suitable for statically scheduled hard real-time systems.

For high-priority interrupt requests, the time from the assertion of the interrupt request from the peripheral to when the processor is executing the interrupt service routine (ISR) has been minimized. The INTC provides a unique vector for each interrupt request source for quick determination of which ISR needs to be executed. It also provides an ample number of priorities so that lower priority ISRs do not delay the execution of higher priority ISRs. To allow the appropriate priorities for each source of interrupt request, the priority of each interrupt request is software configurable.

The INTC supports the priority ceiling protocol for coherent accesses. By providing a modifiable priority mask, the priority can be raised temporarily so that all tasks which share the resource can not preempt each other.

The INTC provides the following features:

- Duplicated periphery
- Unique 9-bit vector per interrupt source
- 16 priority levels with fixed hardware arbitration within priority levels for each interrupt source
- Priority elevation for shared resource

The INTC is replicated for each processor.

Table 4. 257 MAPBGA pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
D11	A[11]	SIUL	GPIO[11]	GPIO[11]
		DSPI_2	SCK	SCK
		FlexPWM_0	A[0]	A[0]
		FlexPWM_0	A[2]	A[2]
		SIUL	—	EIRQ[10]
D12	E[13]	SIUL	GPIO[77]	GPIO[77]
		eTimer_0	ETC[5]	ETC[5]
		DSPI_2	CS3	—
		SIUL	—	EIRQ[25]
D13	F[15]	SIUL	GPIO[95]	GPIO[95]
		LINFlexD_1	—	RXD
D14	$V_{DD\_HV\_IO\_RING}$	—		
D15	V_{PP_TEST}[1]	—		
D16	D[14]	SIUL	GPIO[62]	GPIO[62]
		FlexPWM_0	B[1]	B[1]
		eTimer_0	—	ETC[3]
D17	G[3]	SIUL	GPIO[99]	GPIO[99]
		FlexPWM_0	A[2]	A[2]
		eTimer_0	—	ETC[4]
E1	MDO0	—		
E2	F[6]	SIUL	GPIO[86]	GPIO[86]
		NPC	MDO[1]	—
E3	D[1]	SIUL	GPIO[49]	GPIO[49]
		eTimer_1	ETC[2]	ETC[2]
		CTU_0	EXT_TGR	—
		FlexRay	—	CA_RX
E4	$\overline{NMI}$	—		
E14	Not connected	—		
E15	C[14]	SIUL	GPIO[46]	GPIO[46]
		eTimer_1	ETC[2]	ETC[2]
		CTU_0	EXT_TGR	—
E16	G[2]	SIUL	GPIO[98]	GPIO[98]
		FlexPWM_0	X[2]	X[2]
		DSPI_1	CS1	—

Table 4. 257 MAPBGA pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
K17	A[3]	SIUL	GPIO[3]	GPIO[3]
		eTimer_0	ETC[3]	ETC[3]
		DSPI_2	CS0	CS0
		FlexPWM_0	B[3]	B[3]
		MC_RGM	—	ABS[2]
		SIUL	—	EIRQ[3]
L1	F[10]	SIUL	GPIO[90]	GPIO[90]
		NPC	$\overline{\text{EVTO}}$	—
L2	F[11]	SIUL	GPIO[91]	GPIO[91]
		NPC	—	$\overline{\text{EVTI}}$
L3	D[9]	SIUL	GPIO[57]	GPIO[57]
		FlexPWM_0	X[0]	X[0]
		LINFlexD_1	TXD	—
L4	Not connected	—		
L6	V_{DD_LV}	—		
L7	V_{SS_LV}	—		
L8	V_{SS_LV}	—		
L9	V_{SS_LV}	—		
L10	V_{SS_LV}	—		
L11	V_{SS_LV}	—		
L12	V_{DD_LV}	—		
L14	Not connected	—		
L15	TCK	—		
L16	H[4]	SIUL	GPIO[116]	GPIO[116]
		FlexPWM_1	X[0]	X[0]
		eTimer_2	ETC[0]	ETC[0]
L17	B[4]	SIUL	GPIO[20]	GPIO[20]
		JTAGC	TDO	—
M1	$V_{DD\_HV\_OSC}$	—		
M2	$V_{DD\_HV\_IO\_RING}$	—		
M3	D[8]	SIUL	GPIO[56]	GPIO[56]
		DSPI_1	CS2	—
		eTimer_1	ETC[4]	ETC[4]
		DSPI_0	CS5	—
		FlexPWM_0	—	FAULT[3]

Table 5. Supply pins (continued)

Supply			Pin #	
Symbol	**Description**		**144 pkg**	**257 pkg**
$V_{SS\_LV\_COR}$	VSS_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.		17	VSS_HV[2]
$V_{DD\_LV\_COR}$	VDD_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR}$ pin.		18	VDD_LV[1]
V_{SS} 1V2	VSS_LV_PLL0_PLL1 / 1.2 V Decoupling pins for on-chip FMPLL modules. Decoupling capacitor must be connected between this pin and $V_{DD\_LV\_PLL}$.		35	N4
V_{DD} 1V2	VDD_LV_PLL0_PLL1 Decoupling pins for on-chip FMPLL modules. Decoupling capacitor must be connected between this pin and $V_{SS\_LV\_PLL}$.		36	P4
$V_{DD\_LV\_COR}$	VDD_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR}$ pin.		39	VDD_LV[1]
$V_{SS\_LV\_COR}$	VSS_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.		40	VSS_LV[2]
$V_{DD\_LV\_COR}$	VDD_LV_COR Decoupling pins for core logic and Regulator feedback. Decoupling capacitor must be connected between this pins and $V_{SS\_LV\_REGCOR}$.		70	VDD_LV[1]
$V_{SS\_LV\_COR}$	VSS_LV_REGCOR0 Decoupling pins for core logic and Regulator feedback. Decoupling capacitor must be connected between this pins and $V_{DD\_LV\_REGCOR}$.		71	VSS_LV[2]
$V_{DD\_LV\_COR}$	VDD_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR}$ pin.		93	VDD_LV[1]
$V_{SS\_LV\_COR}$	VSS_LV_COR / 1.2 V Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.		94	VSS_LV[2]
V_{DD} 1V2	VDD_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.		131	VDD_LV[1]
V_{SS} 1V2	VSS_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.		132	VSS_LV[2]
V_{DD} 1V2	VDD_LV_COR / Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.		135	VDD_LV[1]
V_{SS} 1V2	VSS_LV_COR / Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.		137	VSS_LV[2]

[1] VDD_LV balls are tied together on the 257 MAPBGA substrate.

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed[1]		Pin #		
								SRC = 1	SRC = 0		144 pkg	257 pkg
B[7]	PCR[23]	SIUL	—	ALT0	GPI[23]	—	—	—	—		43	R5
		LINFlexD_0	—	—	RXD	PSMI[31]; PADSEL=1						
		ADC_0	—	—	AN[0][3]	—						
B[8]	PCR[24]	SIUL	—	ALT0	GPI[24]	—	—	—	—		47	P7
		eTimer_0	—	—	ETC[5]	PSMI[8]; PADSEL=2						
		ADC_0	—	—	AN[1][3]	—						
B[9]	PCR[25]	SIUL	—	ALT0	GPI[25]	—	—	—	—		52	U7
		ADC_0 ADC_1	—	—	AN[11][3]	—						
B[10]	PCR[26]	SIUL	—	ALT0	GPI[26]	—	—	—	—		53	R8
		ADC_0 ADC_1	—	—	AN[12][3]	—						
B[11]	PCR[27]	SIUL	—	ALT0	GPI[27]	—	—	—	—		54	T8
		ADC_0 ADC_1	—	—	AN[13][3]	—						
B[12]	PCR[28]	SIUL	—	ALT0	GPI[28]	—	—	—	—		55	U8
		ADC_0 ADC_1	—	—	AN[14][3]	—						
B[13]	PCR[29]	SIUL	—	ALT0	GPI[29]	—	—	—	—		60	R10
		LINFlexD_1	—	—	RXD	PSMI[32]; PADSEL=0						
		ADC_1	—	—	AN[0][3]	—						

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed[1]		Pin #		
								SRC = 1	SRC = 0		144 pkg	257 pkg
G[3]	PCR[99]	SIUL	GPIO[99]	ALT0	GPIO[99]	—	—	M	S		104	D17
		FlexPWM_0	A[2]	ALT1	A[2]	PSMI[22]; PADSEL=2						
		eTimer_0	—	—	ETC[4]	PSMI[7]; PADSEL=3						
G[4]	PCR[100]	SIUL	GPIO[100]	ALT0	GPIO[100]	—	—	M	S		100	F17
		FlexPWM_0	B[2]	ALT1	B[2]	PSMI[26]; PADSEL=2						
		eTimer_0	—	—	ETC[5]	PSMI[8]; PADSEL=3						
G[5]	PCR[101]	SIUL	GPIO[101]	ALT0	GPIO[101]	—	—	M	S		85	N17
		FlexPWM_0	X[3]	ALT1	X[3]	PSMI[30]; PADSEL=2						
		DSPI_2	CS3	ALT2	—	—						
G[6]	PCR[102]	SIUL	GPIO[102]	ALT0	GPIO[102]	—	—	M	S		98	G17
		FlexPWM_0	A[3]	ALT1	A[3]	PSMI[23]; PADSEL=3						
G[7]	PCR[103]	SIUL	GPIO[103]	ALT0	GPIO[103]		—	M	S		83	P17
		FlexPWM_0	B[3]	ALT1	B[3]	PSMI[27]; PADSEL=3						
G[8]	PCR[104]	SIUL	GPIO[104]	ALT0	GPIO[104]	—	—	M	S		81	P16
		FlexRay	DBG0	ALT1	—	—						
		DSPI_0	CS1	ALT2	—	—						
		FlexPWM_0	—	—	FAULT[0]	PSMI[16]; PADSEL=2						
		SIUL	—	—	EIRQ[21]	—						

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed[1]		Pin #		
								SRC = 1	SRC = 0		144 pkg	257 pkg
H[1]	PCR[113]	SIUL	GPIO[113]	ALT0	GPIO[113]	—	—	F	S		—	F1
		NPC	MDO[6]	ALT2	—	—						
H[2]	PCR[114]	SIUL	GPIO[114]	ALT0	GPIO[114]	—	—	F	S		—	A4
		NPC	MDO[5]	ALT2	—	—						
H[3]	PCR[115]	SIUL	GPIO[115]	ALT0	GPIO[115]	—	—	F	S		—	G1
		NPC	MDO[4]	ALT2	—	—						
H[4]	PCR[116]	SIUL	GPIO[116]	ALT0	GPIO[116]	—	—	M	S		—	L16
		FlexPWM_1	X[0]	ALT1	X[0]	—						
		eTimer_2	ETC[0]	ALT2	ETC[0]	PSMI[39]; PADSEL=0						
H[5]	PCR[117]	SIUL	GPIO[117]	ALT0	GPIO[117]	—	—	M	S		—	M17
		FlexPWM_1	A[0]	ALT1	A[0]	—						
		DSPI_0	CS4	ALT3	—	—						
H[6]	PCR[118]	SIUL	GPIO[118]	ALT0	GPIO[118]	—	—	M	S		—	H17
		FlexPWM_1	B[0]	ALT1	B[0]	—						
		DSPI_0	CS5	ALT3	—	—						
H[7]	PCR[119]	SIUL	GPIO[119]	ALT0	GPIO[119]	—	—	M	S		—	K16
		FlexPWM_1	X[1]	ALT1	X[1]	—						
		eTimer_2	ETC[1]	ALT2	ETC[1]	PSMI[40]; PADSEL=0						
H[8]	PCR[120]	SIUL	GPIO[120]	ALT0	GPIO[120]	—	—	M	S		—	K15
		FlexPWM_1	A[1]	ALT1	A[1]	—						
		DSPI_0	CS6	ALT3	—	—						
H[9]	PCR[121]	SIUL	GPIO[121]	ALT0	GPIO[121]	—	—	M	S		—	G16
		FlexPWM_1	B[1]	ALT1	B[1]	—						
		DSPI_0	CS7	ALT3	—	—						

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed[1]		Pin #		
								SRC = 1	SRC = 0		144 pkg	257 pkg
I[1]	PCR[129]	SIUL	GPIO[129]	ALT0	GPIO[129]	—	—	M	S		—	C12
		eTimer_2	ETC[1]	ALT1	ETC[1]	PSMI[40]; PADSEL=1						
		DSPI_0	CS5	ALT2	—	—						
		FlexPWM_1	—	—	FAULT[1]	—						
I[2]	PCR[130]	SIUL	GPIO[130]	ALT0	GPIO[130]	—	—	M	S		—	F16
		eTimer_2	ETC[2]	ALT1	ETC[2]	PSMI[41]; PADSEL=1						
		DSPI_0	CS6	ALT2	—	—						
		FlexPWM_1	—	—	FAULT[2]	—						
I[3]	PCR[131]	SIUL	GPIO[131]	ALT0	GPIO[131]	—	—	M	S		—	E17
		eTimer_2	ETC[3]	ALT1	ETC[3]	PSMI[42]; PADSEL=1						
		DSPI_0	CS7	ALT2	—	—						
		CTU_0	EXT_TGR	ALT3	—	—						
		FlexPWM_1	—	—	FAULT[3]	—						
$\overline{\text{RDY}}$	PCR[132]	SIUL	GPIO[132]	ALT0	GPIO[132]	—	—	F	S		—	K3
		NPC	$\overline{\text{RDY}}$	ALT2	—	—						

1 Programmable via the SRC (Slew Rate Control) bit in the respective Pad Configuration Register; S = Slow, M = Medium, F = Fast, SYM = Symmetric (for FlexRay)

2 The default function of this pin out of reset is ALT1 (TDO).

3 Analog

NOTE

Open Drain can be configured by the PCRn for all pins used as output (except FCCU_F[0] and FCCU_F[1]).

Table 8. Absolute maximum ratings[1] (continued)

Symbol		Parameter	Conditions	Min	Max	Unit
TV_{DD}	SR	Supply ramp rate	—	3.0×10^{-6} (3.0 V/sec)	0.5 V/µs	V/µs
V_{IN}	SR	Voltage on any pin with respect to ground ($V_{SS\_HV\_IOx}$)	—	–0.3	6.0[5]	V
			Relative to V_{DD}	–0.3	V_{DD} + 0.3[5,6]	
I_{INJPAD}	SR	Injected input current on any pin during overload condition	—	–10	10	mA
I_{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	–50	50	mA
T_{STG}	SR	Storage temperature	—	–55	150	°C

1 Functional operating conditions are given in the DC electrical characteristics. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.

2 5.3 V for 10 hours cumulative over lifetime of device, 3.3 V +10% for time remaining.

3 Voltage overshoots during a high-to-low or low-to-high transition must not exceed 10 seconds per instance.

4 6.4 V for 10 hours cumulative time, 6.0 V for time remaining.

5 Internal structures hold the input voltage less than the maximum voltage on all pads powered by VDDE supplies, if the maximum injection current specification is met and VDDE is within the operating voltage specifications.

6 Only when V_{DD} < 5.2 V.

3.3 Recommended operating conditions

Table 9. Recommended operating conditions (3.3 V)

Symbol		Parameter	Conditions	Min[1]	Max	Unit
$V_{DD\_HV\_REG}$	SR	3.3 V voltage regulator supply voltage	—	3.0	3.63	V
$V_{DD\_HV\_IOx}$	SR	3.3 V input/output supply voltage	—	3.0	3.63	V
$V_{SS\_HV\_IOx}$	SR	Input/output ground voltage	—	0	0	V
$V_{DD\_HV\_FLA}$	SR	3.3 V flash supply voltage	—	3.0	3.63	V
$V_{SS\_HV\_FLA}$	SR	Flash memory ground	—	0	0	V
$V_{DD\_HV\_OSC}$	SR	3.3 V crystal oscillator amplifier supply voltage	—	3.0	3.63	V
$V_{SS\_HV\_OSC}$	SR	3.3 V crystal oscillator amplifier reference voltage	—	0	0	V
$V_{DD\_HV\_ADR0}$[2,3] $V_{DD\_HV\_ADR1}$	SR	3.3 V / 5.0 V ADC_0 high reference voltage 3.3 V / 5.0 V ADC_1 high reference voltage	—	4.5 to 5.5 or 3.0 to 3.63		V
$V_{DD\_HV\_ADV}$	SR	3.3 V ADC supply voltage	—	3.0	3.63	V
$V_{SS\_HV\_AD0}$ $V_{SS\_HV\_AD1}$	SR	ADC_0 ground and low reference voltage ADC_1 ground and low reference voltage	—	0	0	V
$V_{SS\_HV\_ADV}$	SR	3.3 V ADC supply ground	—	0	0	V
$V_{DD\_LV\_REGCOR}$[4]	SR	Internal supply voltage	—	—	—	V
$V_{SS\_LV\_REGCOR}$[5]	SR	Internal reference voltage	—	0	0	V
$V_{DD\_LV\_CORx}$[2]	SR	Internal supply voltage	—	—	—	V

[3] Data based on characterization results, not tested in production.

3.7 Static latch-up (LU)

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with the EIA/JESD 78 IC latch-up standard.

Table 16. Latch-up results

No.	Symbol		Parameter	Conditions	Class
1	LU	SR	Static latch-up class	T_A = 125 °C conforming to JESD 78	II level A

3.8 Voltage regulator electrical characteristics

The voltage regulator is composed of the following blocks:

- High power regulator HPREG1 (internal ballast to support core current)
- High power regulator HPREG2 (external NPN to support core current)
- Low voltage detector (LVD_MAIN_1) for 3.3 V supply to IO (V_{DDIO})
- Low voltage detector (LVD_MAIN_2) for 3.3 V supply (V_{DDREG})
- Low voltage detector (LVD_MAIN_3) for 3.3 V flash supply ($V_{DDFLASH}$)
- Low voltage detector (LVD_DIG_MAIN) for 1.2 V digital core supply (HPV_{DD})
- Low voltage detector (LVD_DIG_BKUP) for the self-test of LVD_DIG_MAIN
- High voltage detector (HVD_DIG_MAIN) for 1.2 V digital CORE supply (HPV_{DD})
- High voltage detector (HVD_DIG_BKUP) for the self-test of HVD_DIG_MAIN.
- Power on Reset (POR)

HPREG1 uses an internal ballast to support the core current. HPREG2 is used only when external NPN transistor is present on board to supply core current. The MPC5643L always powers up using HPREG1 if an external NPN transistor is present. Then the MPC5643L makes a transition from HPREG1 to HPREG2. This transition is dynamic. Once HPREG2 is fully operational, the controller part of HPREG1 is switched off.

The following bipolar transistors are supported:

- BCP68 from ON Semiconductor
- BCX68 from Infineon

Table 17. Recommended operating characteristics

Symbol	Parameter	Value	Unit
$h_{FE}(\beta)$	DC current gain (Beta)	85 - 375	—
P_D	Maximum power dissipation @ T_A=25°C[1]	1.5	W
I_{CMaxDC}	Maximum peak collector current	1.0	A
VCE_{SAT}	Collector-to-emitter saturation voltage(Max)	600[2]	mV
V_{BE}	Base-to-emitter voltage (Max)	1.0	V

[1] derating factor 12mW/degC

Table 20. Current consumption characteristics

Symbol		Parameter	Conditions[1]	Min	Typ	Max	Unit
$I_{DD\_LV\_FULL}$ + $I_{DD\_LV\_PLL}$	T	Operating current	1.2 V supplies T_J = 25 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	50 mA+ 2.18 mA*f_{CPU}[MHz]	mA
			1.2 V supplies T_J = 150 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	80 mA+ 2.50 mA*f_{CPU}[MHz]	
$I_{DD\_LV\_TYP}$ [2] + $I_{DD\_LV\_PLL}$ [2]	T	Operating current	1.2 V supplies T_J = 25 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	26 + 2.10 mA*f_{CPU}[MHz]	mA
			1.2 V supplies T_J = 150 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	41 mA+ 2.30 mA*f_{CPU}[MHz]	
$I_{DD\_LV\_BIST}$ + $I_{DD\_LV\_PLL}$	T	Operating current	1.2 V supplies during LBIST (full LBIST configuration) T_J = 25 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	250	mA
			1.2 V supplies during LBIST (full LBIST configuration) T_J = 150 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	290	
$I_{DD\_LV\_TYP}$ [2] + $I_{DD\_LV\_PLL}$ [2]	P	Operating current	1.2 V supplies T_J = 25 °C $V_{DD\_LV\_COR}$ = 1.32 V LSM mode	—	—	279	mA
			T_J = 150 °C $V_{DD\_LV\_COR}$ = 1.32 V LSM mode	—	—	318	mA
$I_{DD\_LV\_TYP}$ + $I_{DD\_LV\_PLL}$ [2]	T	Operating current	1.2V supplies Tj=105°C $V_{DD\_LV\_COR}$ = 1.2V LSM mode	—	—	275	mA
			1.2V supplies Tj=125°C $V_{DD\_LV\_COR}$ = 1.2V LSM mode	—	—	299	mA

A real filter can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC filter). The RC filtering may be limited according to the value of source impedance of the transducer or circuit supplying the analog signal to be measured. The filter at the input pins must be designed taking into account the dynamic characteristics of the input signal (bandwidth) and the equivalent input impedance of the ADC itself.

In fact a current sink contributor is represented by the charge sharing effects with the sampling capacitance: C_S and C_{p2} being substantially a switched capacitance, with a frequency equal to the conversion rate of the ADC, it can be seen as a resistive path to ground. For instance, assuming a conversion rate of 1 MHz, with C_{p2} + CS equal to 7.5 pF, a resistance of 133 kΩ is obtained (R_{EQ} = 1 / (fS*(C_{p2}+C_S)), where fS represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on C_s) and the sum of R_S + R_F, the external circuit must be designed to respect the Equation 4:

$$V_A \bullet \frac{R_S + R_F}{R_{EQ}} < \frac{1}{2} LSB \qquad \textit{Eqn. 4}$$

Equation 4 generates a constraint for external network design, in particular on resistive path. Internal switch resistances (R_{SW} and R_{AD}) can be neglected with respect to external resistances.

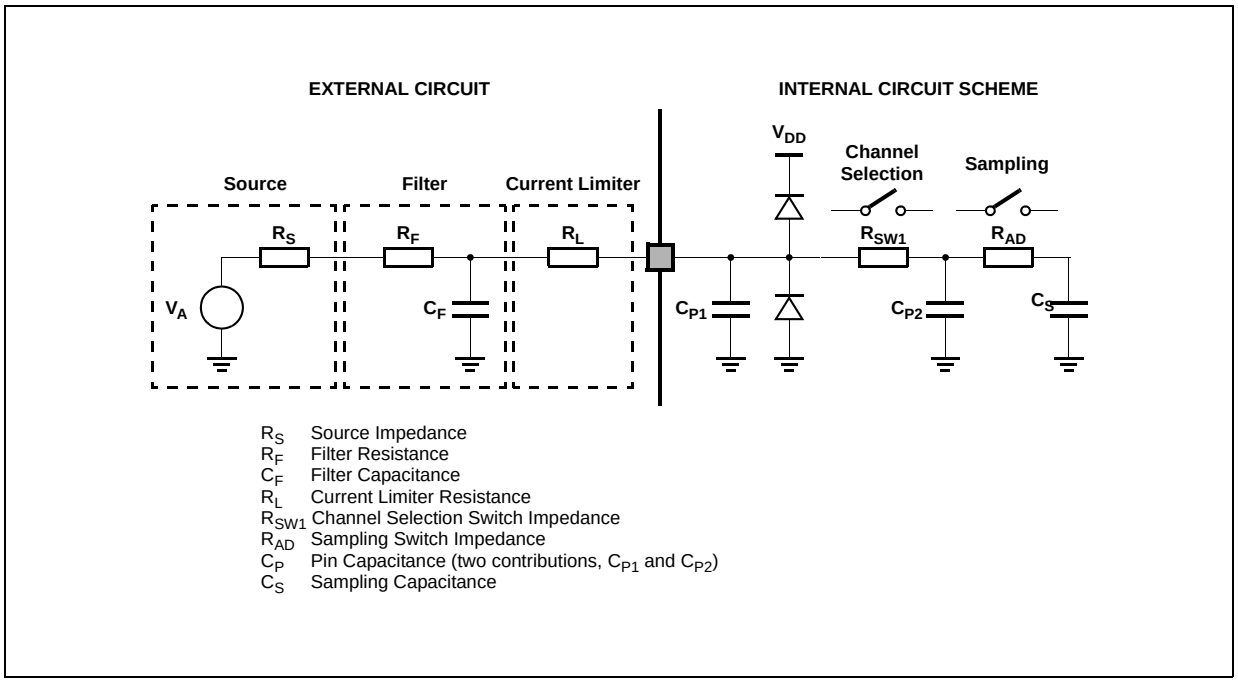


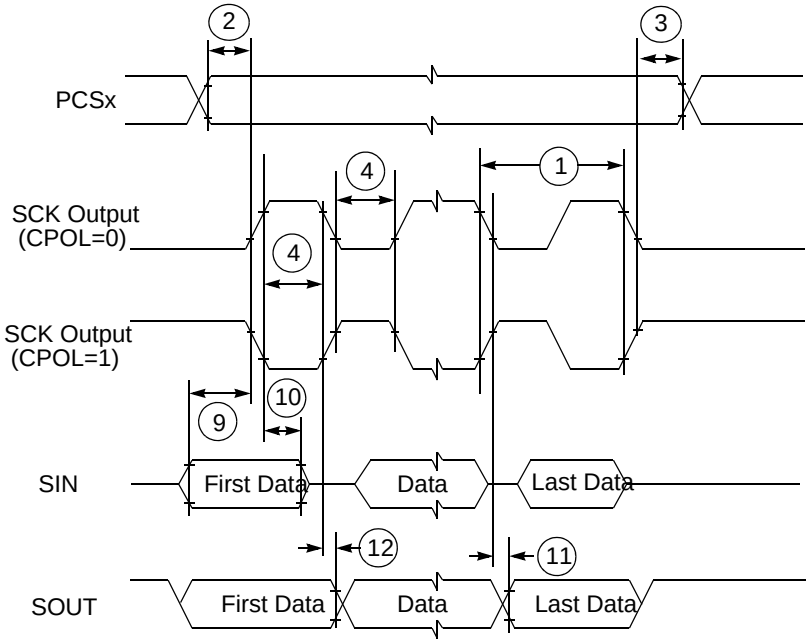
Figure 8. Input Equivalent Circuit

A second aspect involving the capacitance network shall be considered. Assuming the three capacitances C_F, C_{P1} and C_{P2} are initially charged at the source voltage V_A (refer to the equivalent circuit reported in Figure 8): A charge sharing phenomenon is installed when the sampling phase is started (A/D switch close).

Table 39. DSPI timing (continued)

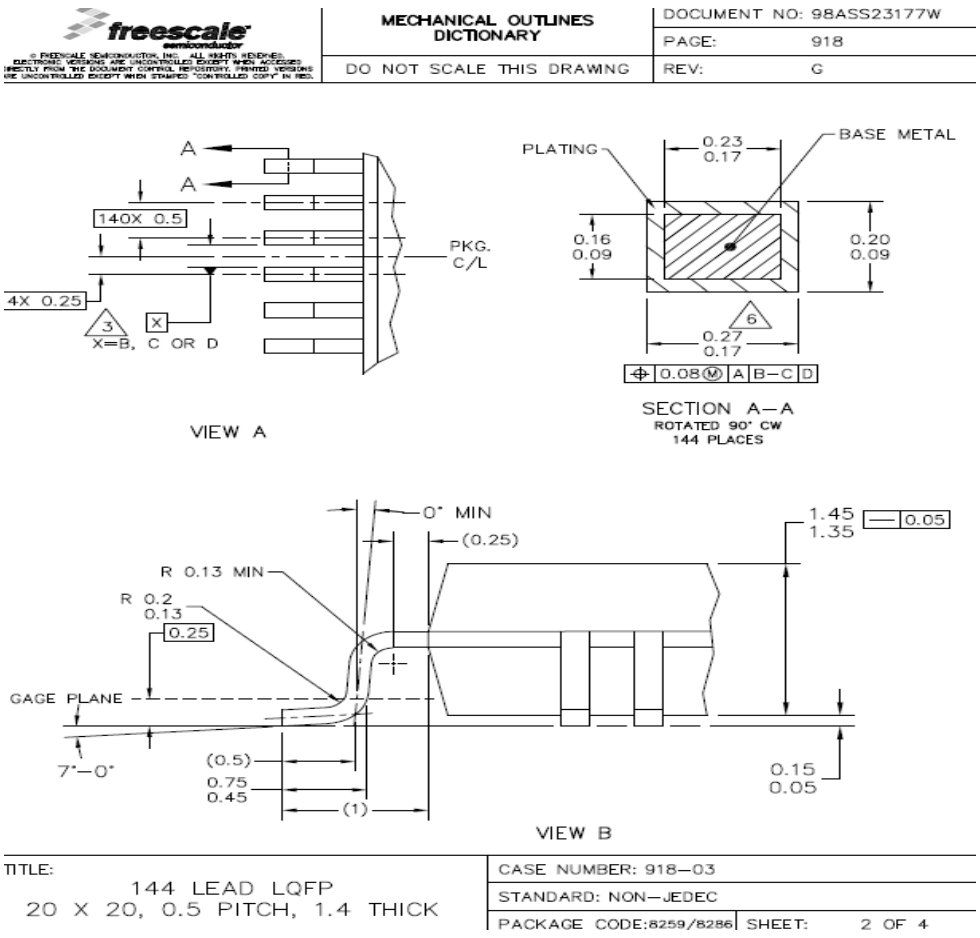
No.	Symbol		Parameter	Conditions	Min	Max	Unit
12	t_{HO}	D	Data hold time for outputs	Master (MTFE = 0)	–2	—	ns
				Slave	6	—	
				Master (MTFE = 1, CPHA = 0)	6	—	
				Master (MTFE = 1, CPHA = 1)	–2	—	

1 Slave Receive Only Mode can operate at a maximum frequency of 60 MHz. In this mode, the DSPI can receive data on SIN, but no valid data is transmitted on SOUT.



Note: The numbers shown are referenced in Table 39.

Figure 30. DSPI classic SPI timing — master, CPHA = 0



NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DATUMS B, C AND D TO BE DETERMINED AT DATUM PLANE H.
4. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE SIZE BY A MAXIMUM OF 0.1 mm.
5. THIS DIMENSIONS DO NOT INCLUDE MOLD PROTRUSIONS. THE MAXIMUM ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THIS DIMENSIONS ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
6. THIS DIMENSION DOES NOT INCLUDE DAM BAR PROTRUSION. PROTRUSIONS SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.35. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL BE 0.07 MM.
7. THIS DIMENSIONS ARE DETERMINED AT THE SEATING PLANE, DATUM A.

Figure 40. 144 LQFP package mechanical drawing (2 of 2)

Table 40. Orderable part number summary (continued)

Part number[1]	Flash/SRAM	Package	Speed (MHz)[2]	Other features
SPC5643LF2MLQ8	1 MB/128 KB	144 LQFP (Pb free)	80	No FlexRay –40–125 °C
SPC5643LF2MMM8	1 MB/128 KB	257 MAPBGA (Pb free)	80	No FlexRay –40–125 °C
SPC5643LFF2VLQ8	1 MB/128 KB	144 LQFP (Pb free)	80	FlexRay –40–105 °C
SPC5643LFF2VMM8	1 MB/128 KB	257 MAPBGA (Pb free)	80	FlexRay –40–105 °C
SPC5643LF2VLQ8	1 MB/128 KB	144 LQFP (Pb free)	80	No FlexRay –40–105 °C
SPC5643LF2VMM8	1 MB/128 KB	257 MAPBGA (Pb free)	80	No FlexRay –40–105 °C

1 All packaged devices are SPC, rather than MPC or SPC, until product qualifications are complete. The unpackaged device prefix is PCC, rather than SCC, until product qualification is complete. Not all configurations are available in the SPC parts.

2 This speed rating does not include the ±2% for frequency modulation.

6 Document revision history

Table 41 summarizes revisions to this document.

Table 41. Revision history

Revision	Date	Description of changes
1	2 Mar 2009	Initial release.
2	5 May 2009	Updated, Advance Information. —Revised SINAD/SNR specifications. — Updated pinout and pin multiplexing information.
3	5 Oct 2009	Updated, Advance Information, Public release. — Throughout this document, added information for 257 MAPBGA package. — Updated Table 1, MPC5643L device summary. — Updated Section 1.3, Feature Details. — Updated pin-out and pin multiplexing tables. — In Section 3, Electrical characteristics, added symbols for signal characterization methods. — In Table 8, updated maximum ratings. — In Table 10 and Table 11, removed moving-air thermal characteristics. — Updated Section 3.8, Voltage regulator electrical characteristics. — Updated Section 3.14, ADC electrical characteristics. — Updated Section 3.15, Flash memory electrical characteristics. — Updated Section 3.17.1, RESET pin characteristics. — Removed External interrupt timing (IRQ pin) timing specifications. — Updated Section 3.17.6, DSPI timing. — Updated Section 5, Ordering information.

Table 41. Revision history (continued)

Revision	Date	Description of changes
6 (cont.)	11 Mar 2011 (cont.)	In the “ADC conversion characteristics” table: • Changed DNL min from -2 to -1. • Changed OFS min from -2 to -6. • Changed OFS max from 2 to 6. • Changed GNE min from -2 to -6. • Changed GNE max from 2 to 6. • Changed SNR min from 69 to 67. • Changed TUE min (without current injection) from -6 to -8. • Changed TUE max (without current injection) from 6 to 8. • Changed TUE min (with current injection) from -8 to -10. • Changed TUE max (with current injection) from 8 to 10.
7	25 Mar 2011	In the “Description” section, changed the first paragraph and its bullets to paragraph form only. In the “Voltage regulator electrical specifications“ table, changed the C_{V1V2} Min value from “—“ to 300 nF, and changed the Max value from 300 nF to 900 nF. In the “Supply current characteristics (cut2)“ table, corrected the “$I_{DD\_LV\_TYP}$ + $I_{DD\_LV\_PLL}$“ values as follows: • Changed the maximum value for “T_J = ambient“ from “279 mA+ 2.10 mA*f_{CPU}“ to “279 mA”. • Changed the maximum value for “T_J = 150 °C“ from “318 mA+ 2.30 mA*f_{CPU}“ to 318 mA. • Changed the frequency multiplier “f_{CPU}” in the max value to read “f_{CPU}[MHz]“ for “$I_{DD\_LV\_FULL}$ + $I_{DD\_LV\_PLL}$“ and “$I_{DD\_LV\_TYP}$ + $I_{DD\_LV\_PLL}$“. In the “JTAG pin AC electrical characteristics“ table: • Changed t_{JCYC} min from 100ns to 62.5ns. • Changed t_{JDC} units from “ns” to “%”. In the “Nexus debug port timing“ table: • Changed t_{TCYC} min from 40ns to 62.5 ns. • Changed t_{JOV} parameter description from “TCK Low to TDO Data Valid“ to “TCK Low to TDO/RDY Data Valid“. Changed “DDR” to “Double Data Rate (DDR)“ in the “Nexus DDR Mode output timing“ figure. Changed “TDO” to “TDO/RDY” in the “Nexus TDI, TMS, TDO timing“ figure. Removed “f_{max}” from the “DSPI timing” table.

Table 41. Revision history (continued)

Revision	Date	Description of changes
		• Added Table 29 (MPC5643L SWG Specifications) • In Table 29 (MPC5643L SWG Specifications) Added table footnote for Common Mode. Changed text from “internal device pad resistance” to “internal device routing resistance”. • Added Figure 26 in Section 3.20.4, “Nexus timing”. • In Table 30 (Pad AC specifications (3.3 V , IPP_HVE = 0)), removed the row of pad “Pull Up/Downc(3.6 V max)”. • In Table 40 (Orderable part number summary) and Figure 43, updated part numbers (changed ‘PPC’ to ‘SPC’ and ‘F0’ to ‘F2’). • Replaced Figure 39, Figure 40, Figure 41, Figure 42 with the new versions. • InTable 18 (Voltage regulator electrical specifications),changed the symbol of spec external decoupling capacitor from SR to C_{ext}. In Figure 4, changed the ESR range in note text to 1 mW to 100 mW from 30 mW to 150 mW. • In Section 1.5.32, “Sine Wave Generator (SWG)” removed the following text: Frequency range from 1kHz to 50kHz. Sine wave amplitude from 0.47 V to 2.26 V. • In Table 20 (Current consumption characteristics)”,changed symbol from ‘C’ to ‘T’ , added “operating current” to the parameter and updated the maximum value for five additional RunIDD parameters. • In Table 20 (Current consumption characteristics), changed “Conditions” from ‘1.2 V supplies’ to ‘1.2 V supplies during LBIST (full LBIST configuration)’ for all the parameters. • Removed Table “SWG electrical characteristics”. • In Table 18 (Voltage regulator electrical specifications), changed the “Digital supply high voltage detector upper threshold low limit (After a destructive reset initialization phase completion)” from 1.43V to 1.38V. • Added Table 17 (Recommended operating characteristics). • Updated the IDD values in Table 20 (Current consumption characteristics). Changed conditions text from “1.2 supplies during LBIST (full LBIST configuration)” to “1.2 V supplies” for all the IDD parameters except $I_{DD\_LV\_BIST}$+$I_{DD\_LV\_PLL}$. Added footnote in “Conditions” for the DPM mode. • Removed Cut references from the whole document. • In Table 25 (ADC conversion characteristics), changed the sampling frequency value from ‘1 MHz’ to ‘983.6 KHz’.
8.1	07 May 2012	• Deleted the Footer "Preliminary-Subject to Change Without Notice" label.

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