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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Dual-Core
Speed	120MHz
Connectivity	CANbus, FlexRay, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	-
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5643lff2mlq1

1 Introduction

1.1 Document overview

This document describes the features of the family and options available within the family members, and highlights important electrical and physical characteristics of the devices.

This document provides electrical specifications, pin assignments, and package diagrams for the MPC5643L series of microcontroller units (MCUs). For functional characteristics, see the *MPC5643L Microcontroller Reference Manual*. For use of the MPC5643Lin a fail-safe system according to safety standard ISO26262, see the *Safety Application Guide for MPC5643L*.

1.2 Description

The MPC5643L series microcontrollers are system-on-chip devices that are built on Power Architecture technology and contain enhancements that improve the architecture's fit in embedded applications, include additional instruction support for digital signal processing (DSP) and integrate technologies such as an enhanced time processor unit, enhanced queued analog-to-digital converter, Controller Area Network, and an enhanced modular input-output system.

The MPC5643L family of 32-bit microcontrollers is the latest achievement in integrated automotive application controllers. It belongs to an expanding range of automotive-focused products designed to address electrical hydraulic power steering (EHPS), electric power steering (EPS) and airbag applications. The advanced and cost-efficient host processor core of the MPC5643L automotive controller family complies with the Power Architecture embedded category. It operates at speeds as high as 120 MHz and offers high-performance processing optimized for low power consumption. It capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with users' implementations.

1.3 Device comparison

Table 1. MPC5643L device summary

Feature		MPC5643L
CPU	Type	2 × e200z4 (in lock-step or decoupled operation)
	Architecture	Harvard
	Execution speed	0–120 MHz (+2% FM)
	DMIPS intrinsic performance	>240 MIPS
	SIMD (DSP + FPU)	Yes
	MMU	16 entry
	Instruction set PPC	Yes
	Instruction set VLE	Yes
	Instruction cache	4 KB, EDC
	MPU-16 regions	Yes, replicated module
	Semaphore unit (SEMA4)	Yes
Buses	Core bus	AHB, 32-bit address, 64-bit data
	Internal periphery bus	32-bit address, 32-bit data
Crossbar	Master × slave ports	Lock Step Mode: 4 × 3 Decoupled Parallel Mode: 6 × 3

- Transfer control descriptors mapped inside the SRAM

The eDMA controller is replicated for each processing channel.

1.5.5 On-chip flash memory with ECC

This device includes programmable, non-volatile flash memory. The non-volatile memory (NVM) can be used for instruction storage or data storage, or both. The flash memory module interfaces with the system bus through a dedicated flash memory array controller. It supports a 64-bit data bus width at the system bus port, and a 128-bit read data interface to flash memory. The module contains four 128-bit prefetch buffers. Prefetch buffer hits allow no-wait responses. Buffer misses incur a 3 wait state response at 120 MHz.

The flash memory module provides the following features

- 1 MB of flash memory in unique multi-partitioned hard macro
- Sectorization: 16 KB + 2 × 48 KB + 16 KB + 2 × 64 KB + 2 × 128 KB + 2 × 256 KB
- EEPROM emulation (in software) within same module but on different partition
- 16 KB test sector and 16 KB shadow block for test, censorship device and user option bits
- Wait states:
  - 3 wait states for frequencies =< 120 MHz
  - 2 wait states for frequencies =< 80 MHz
  - 1 wait state for frequencies =< 60 MHz
- Flash memory line 128-bit wide with 8-bit ECC on 64-bit word (total 144 bits)
- Accessed via a 64-bit wide bus for write and a 128-bit wide array for read operations
- 1-bit error correction, 2-bit error detection

1.5.6 On-chip SRAM with ECC

The MPC5643L SRAM provides a general-purpose single port memory.

ECC handling is done on a 32-bit boundary for data and it is extended to the address to have the highest possible diagnostic coverage including the array internal address decoder.

The SRAM module provides the following features:

- System SRAM: 128 KB
- ECC on 32-bit word (syndrome of 7 bits)
  - ECC covers SRAM bus address
- 1-bit error correction, 2-bit error detection
- Wait states:
  - 1 wait state for frequencies =< 120 MHz
  - 0 wait states for frequencies =< 80 MHz

1.5.7 Platform flash memory controller

The following list summarizes the key features of the flash memory controller:

- Single AHB port interface supports a 64-bit data bus. All AHB aligned and unaligned reads within the 32-bit container are supported. Only aligned word writes are supported.
- Array interfaces support a 128-bit read data bus and a 64-bit write data bus for each bank.
- Code flash (bank0) interface provides configurable read buffering and page prefetch support.
  - Four page-read buffers (each 128 bits wide) and a prefetch controller support speculative reading and optimized flash access.

Table 2. Platform memory access time summary (continued)

AHB transfer	Data phase wait states	Description
e200z4d data write	0	SRAM 64-bit write (executed as 2 x 32-bit writes)
e200z4d data write	0–2	SRAM 8-,16-bit write (Read-modify-Write for ECC)
e200z4d flash memory read	0	Flash memory prefetch buffer hit (page hit)
e200z4d flash memory read	3	Flash memory prefetch buffer miss (at 120 MHz; includes 1 cycle of program flash memory controller arbitration)

1.5.10 Error Correction Status Module (ECSM)

The ECSM on this device manages the ECC configuration and reporting for the platform memories (flash memory and SRAM). It does not implement the actual ECC calculation. A detected error (double error for flash memory or SRAM) is also reported to the FCCU. The following errors and indications are reported into the ECSM dedicated registers:

- ECC error status and configuration for flash memory and SRAM
- ECC error reporting for flash memory
- ECC error reporting for SRAM
- ECC error injection for SRAM

1.5.11 Peripheral bridge (PBRIDGE)

The PBRIDGE implements the following features:

- Duplicated periphery
- Master access privilege level per peripheral (per master: read access enable; write access enable)
- Checker applied on PBRIDGE output toward periphery
- Byte endianess swap capability

1.5.12 Interrupt Controller (INTC)

The INTC provides priority-based preemptive scheduling of interrupt requests, suitable for statically scheduled hard real-time systems.

For high-priority interrupt requests, the time from the assertion of the interrupt request from the peripheral to when the processor is executing the interrupt service routine (ISR) has been minimized. The INTC provides a unique vector for each interrupt request source for quick determination of which ISR needs to be executed. It also provides an ample number of priorities so that lower priority ISRs do not delay the execution of higher priority ISRs. To allow the appropriate priorities for each source of interrupt request, the priority of each interrupt request is software configurable.

The INTC supports the priority ceiling protocol for coherent accesses. By providing a modifiable priority mask, the priority can be raised temporarily so that all tasks which share the resource can not preempt each other.

The INTC provides the following features:

- Duplicated periphery
- Unique 9-bit vector per interrupt source
- 16 priority levels with fixed hardware arbitration within priority levels for each interrupt source
- Priority elevation for shared resource

The INTC is replicated for each processor.

- Double buffered PWM registers
  - Integral reload rates from 1 to 16
  - Half cycle reload capability
- Multiple ADC trigger events can be generated per PWM cycle via hardware
- Fault inputs can be assigned to control multiple PWM outputs
- Programmable filters for fault inputs
- Independently programmable PWM output polarity
- Independent top and bottom deadtime insertion
- Each complementary pair can operate with its own PWM frequency and deadtime values
- Individual software control for each PWM output
- All outputs can be forced to a value simultaneously
- PWMX pin can optionally output a third signal from each channel
- Channels not used for PWM generation can be used for buffered output compare functions
- Channels not used for PWM generation can be used for input capture functions
- Enhanced dual edge capture functionality
- Option to supply the source for each complementary PWM signal pair from any of the following:
  - External digital pin
  - Internal timer channel
  - External ADC input, taking into account values set in ADC high- and low-limit registers
- DMA support

1.5.31 eTimer module

The MPC5643L provides three eTimer modules (on the LQFP package eTimer_2 is available internally only without any external I/O access). Six 16-bit general purpose up/down timer/counters per module are implemented with the following features:

- Maximum clock frequency of 120 MHz
- Individual channel capability
  - Input capture trigger
  - Output compare
  - Double buffer (to capture rising edge and falling edge)
  - Separate prescaler for each counter
  - Selectable clock source
  - 0–100% pulse measurement
  - Rotation direction flag (Quad decoder mode)
- Maximum count rate
  - Equals peripheral clock divided by 2 for external event counting
  - Equals peripheral clock for internal clock counting
- Cascadeable counters
- Programmable count modulo
- Quadrature decode capabilities
- Counters can share available input pins
- Count once or repeatedly
- Preloadable counters
- Pins available as GPIO when timer functionality not in use
- DMA support

Table 3. 144 LQFP pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
14	A[5]	SIUL	GPIO[5]	GPIO[5]
		DSPI_1	CS0	CS0
		eTimer_1	ETC[5]	ETC[5]
		DSPI_0	CS7	—
		SIUL	—	EIRQ[5]
15	C[7]	SIUL	GPIO[39]	GPIO[39]
		FlexPWM_0	A[1]	A[1]
		SSCM	DEBUG[7]	—
		DSPI_0	—	SIN
16	$V_{DD\_HV\_REG\_0}$	—		
17	$V_{SS\_LV\_COR}$	—		
18	$V_{DD\_LV\_COR}$	—		
19	F[7]	SIUL	GPIO[87]	GPIO[87]
		NPC	MCKO	—
20	F[8]	SIUL	GPIO[88]	GPIO[88]
		NPC	$\overline{\text{MSEO[1]}}$	—
21	$V_{DD\_HV\_IO}$	—		
22	$V_{SS\_HV\_IO}$	—		
23	F[9]	SIUL	GPIO[89]	GPIO[89]
		NPC	$\overline{\text{MSEO[0]}}$	—
24	F[10]	SIUL	GPIO[90]	GPIO[90]
		NPC	$\overline{\text{EVTO}}$	—
25	F[11]	SIUL	GPIO[91]	GPIO[91]
		NPC	—	$\overline{\text{EVTI}}$
26	D[9]	SIUL	GPIO[57]	GPIO[57]
		FlexPWM_0	X[0]	X[0]
		LINFlexD_1	TXD	—
27	$V_{DD\_HV\_OSC}$	—		
28	$V_{SS\_HV\_OSC}$	—		
29	XTAL	—		
30	EXTAL	—		
31	$\overline{\text{RESET}}$	—		

2.4 Pin muxing

Table 7 defines the pin list and muxing for this device.

Each entry of Table 7 shows all the possible configurations for each pin, via the alternate functions. The default function assigned to each pin after reset is indicated by ALT0.

NOTE

Pins labeled “NC” are to be left unconnected. Any connection to an external circuit or voltage may cause unpredictable device behavior or damage.

Pins labeled “Reserved” are to be tied to ground. Not doing so may cause unpredictable device behavior.

Table 7. Pin muxing

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed[1]		Pin #		
								SRC = 1	SRC = 0		144 pkg	257 pkg
Port A												
A[0]	PCR[0]	SIUL	GPIO[0]	ALT0	GPIO[0]	—	—	M	S		73	T14
		eTimer_0	ETC[0]	ALT1	ETC[0]	PSMI[35]; PADSEL=0						
		DSPI_2	SCK	ALT2	SCK	PSMI[1]; PADSEL=0						
		SIUL	—	—	EIRQ[0]	—						
A[1]	PCR[1]	SIUL	GPIO[1]	ALT0	GPIO[1]	—	—	M	S		74	R14
		eTimer_0	ETC[1]	ALT1	ETC[1]	PSMI[36]; PADSEL=0						
		DSPI_2	SOUT	ALT2	—	—						
		SIUL	—	—	EIRQ[1]	—						

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed[1]		Pin #		
								SRC = 1	SRC = 0		144 pkg	257 pkg
A[2]	PCR[2]	SIUL	GPIO[2]	ALT0	GPIO[2]	—	Pull down	M	S		84	N16
		eTimer_0	ETC[2]	ALT1	ETC[2]	PSMI[37]; PADSEL=0						
		FlexPWM_0	A[3]	ALT3	A[3]	PSMI[23]; PADSEL=0						
		DSPI_2	—	—	SIN	PSMI[2]; PADSEL=0						
		MC_RGM	—	—	ABS[0]	—						
		SIUL	—	—	EIRQ[2]	—						
A[3]	PCR[3]	SIUL	GPIO[3]	ALT0	GPIO[3]	—	Pull down	M	S		92	K17
		eTimer_0	ETC[3]	ALT1	ETC[3]	PSMI[38]; PADSEL=0						
		DSPI_2	CS0	ALT2	CS0	PSMI[3]; PADSEL=0						
		FlexPWM_0	B[3]	ALT3	B[3]	PSMI[27]; PADSEL=0						
		MC_RGM	—	—	ABS[2]	—						
		SIUL	—	—	EIRQ[3]	—						
A[4]	PCR[4]	SIUL	GPIO[4]	ALT0	GPIO[4]	—	Pull down	M	S		108	C16
		eTimer_1	ETC[0]	ALT1	ETC[0]	PSMI[9]; PADSEL=0						
		DSPI_2	CS1	ALT2	—	—						
		eTimer_0	ETC[4]	ALT3	ETC[4]	PSMI[7]; PADSEL=0						
		MC_RGM	—	—	FAB	—						
		SIUL	—	—	EIRQ[4]	—						

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed[1]		Pin #		
								SRC = 1	SRC = 0		144 pkg	257 pkg
A[5]	PCR[5]	SIUL	GPIO[5]	ALT0	GPIO[5]	—	—	M	S		14	H4
		DSPI_1	CS0	ALT1	CS0	—						
		eTimer_1	ETC[5]	ALT2	ETC[5]	PSMI[14]; PADSEL=0						
		DSPI_0	CS7	ALT3	—	—						
		SIUL	—	—	EIRQ[5]	—						
A[6]	PCR[6]	SIUL	GPIO[6]	ALT0	GPIO[6]	—	—	M	S		2	G4
		DSPI_1	SCK	ALT1	SCK	—						
		SIUL	—	—	EIRQ[6]	—						
A[7]	PCR[7]	SIUL	GPIO[7]	ALT0	GPIO[7]	—	—	M	S		10	F3
		DSPI_1	SOUT	ALT1	—	—						
		SIUL	—	—	EIRQ[7]	—						
A[8]	PCR[8]	SIUL	GPIO[8]	ALT0	GPIO[8]	—	—	M	S		12	F4
		DSPI_1	—	—	SIN	—						
		SIUL	—	—	EIRQ[8]	—						
A[9]	PCR[9]	SIUL	GPIO[9]	ALT0	GPIO[9]	—	—	M	S		134	B6
		DSPI_2	CS1	ALT1	—	—						
		FlexPWM_0	B[3]	ALT3	B[3]	PSMI[27]; PADSEL=1						
		FlexPWM_0	—	—	FAULT[0]	PSMI[16]; PADSEL=0						

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed[1]		Pin #		
								SRC = 1	SRC = 0		144 pkg	257 pkg
A[13]	PCR[13]	SIUL	GPIO[13]	ALT0	GPIO[13]	—	—	M	S		136	C6
		FlexPWM_0	B[2]	ALT2	B[2]	PSMI[26]; PADSEL=1						
		DSPI_2	—	—	SIN	PSMI[2]; PADSEL=1						
		FlexPWM_0	—	—	FAULT[0]	PSMI[16]; PADSEL=1						
		SIUL	—	—	EIRQ[12]	—						
A[14]	PCR[14]	SIUL	GPIO[14]	ALT0	GPIO[14]	—	—	M	S		143	B4
		FlexCAN_1	TXD	ALT1	—	—						
		eTimer_1	ETC[4]	ALT2	ETC[4]	PSMI[13]; PADSEL=0						
		SIUL	—	—	EIRQ[13]	—						
A[15]	PCR[15]	SIUL	GPIO[15]	ALT0	GPIO[15]	—	—	M	S		144	D3
		eTimer_1	ETC[5]	ALT2	ETC[5]	PSMI[14]; PADSEL=1						
		FlexCAN_1	—	—	RXD	PSMI[34]; PADSEL=0						
		FlexCAN_0	—	—	RXD	PSMI[33]; PADSEL=0						
		SIUL	—	—	EIRQ[14]	—						
Port B												
B[0]	PCR[16]	SIUL	GPIO[16]	ALT0	GPIO[16]	—	—	M	S		109	B15
		FlexCAN_0	TXD	ALT1	—	—						
		eTimer_1	ETC[2]	ALT2	ETC[2]	PSMI[11]; PADSEL=0						
		SSCM	DEBUG[0]	ALT3	—	—						
		SIUL	—	—	EIRQ[15]	—						

3.4.1 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from Equation 1:

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad \textit{Eqn. 1}$$

where:

T_A = ambient temperature for the package (^oC)
$R_{\theta JA}$ = junction to ambient thermal resistance ($^oC/W$)
P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed in Equation 2 as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad \textit{Eqn. 2}$$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
$R_{\theta JC}$ = junction to case thermal resistance (°C/W)
$R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using Equation 3:

$$T_J = T_T + (\Psi_{JT} \times P_D) \quad \textit{Eqn. 3}$$

where:

T_T = thermocouple temperature on top of the package (°C)
Ψ_{JT} = thermal characterization parameter (°C/W)
P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

3.4.1.1 References

Semiconductor Equipment and Materials International
3081 Zanker Road

Table 19. DC electrical characteristics[1] (continued)

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
V_{OH_M}	P	Medium, high level output voltage	I_{OH} = –2 mA	$V_{DD\_HV\_IOx}$ – 0.8	—	—	V
V_{OL_F}	P	Fast, high level output voltage	I_{OL} = 11 mA	—	—	0.5	V
V_{OH_F}	P	Fast, high level output voltage	I_{OH} = –11 mA	$V_{DD\_HV\_IOx}$ – 0.8	—	—	V
V_{OL_SYM}	P	Symmetric, high level output voltage	I_{OL} = 1.5 mA	—	—	0.5	V
V_{OH_SYM}	P	Symmetric, high level output voltage	I_{OH} = –1.5 mA	$V_{DD\_HV\_IOx}$ – 0.8	—	—	V
I_{INJ}	T	DC injection current per pin (all bi-directional ports)	—	–1	—	1	mA
I_{PU}	P	Equivalent pull-up current	$V_{IN} = V_{IL}$	–130	—	—	µA
			$V_{IN} = V_{IH}$	—	—	–10	
I_{PD}	P	Equivalent pull-down current	$V_{IN} = V_{IL}$	10	—	—	µA
			$V_{IN} = V_{IH}$	—	—	130	
I_{IL}	P	Input leakage current (all bidirectional ports)	T_J = –40 to +150 °C	-1	—	1	µA
		Input leakage current (all ADC input-only ports)[4]		-0.25	—	0.25	
		Input leakage current (shared ADC input-only ports)		-0.3	—	0.3	
V_{ILR}	P	$\overline{\text{RESET}}$, low level input voltage	—	–0.1[2]	—	0.35 $V_{DD\_HV\_IOx}$	V
V_{IHR}	P	$\overline{\text{RESET}}$, high level input voltage	—	0.65 $V_{DD\_HV\_IOx}$	—	$V_{DD\_HV\_IOx}$+0.1[2]	V
V_{HYSR}	D	$\overline{\text{RESET}}$, Schmitt trigger hysteresis	—	0.1 $V_{DD\_HV\_IOx}$	—	—	V
V_{OLR}	D	$\overline{\text{RESET}}$, low level output voltage	I_{OL} = 2 mA	—	—	0.5	V
I_{PD}	D	$\overline{\text{RESET}}$, equivalent pull-down current	$V_{IN} = V_{IL}$	10	—	—	µA
			$V_{IN} = V_{IH}$	—	—	130	

1 These specifications are design targets and subject to change per device characterization.

2 “SR” parameter values must not exceed the absolute maximum ratings shown in Table 8.

3 The max input voltage on the ADC pins is the ADC reference voltage VDD_HV_ADRx.

4 Measured values are applicable to all modes of the pad i.e. IBE = 0/1 and / or APC= 0/1.

3.10 Supply current characteristics

Current consumption data is given in Table 20. These specifications are design targets and are subject to change per device characterization.

Table 23. FMPLL electrical characteristics (continued)

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
t_{lpll}	D	FMPLL lock time [6, 7]	—	—	—	200	µs
t_{dc}	D	Duty cycle of reference	—	40	—	60	%
C_{JITTER}	T	CLKOUT period jitter[8,9,10,11]	Long-term jitter (avg. over 2 ms interval), $f_{FMPLLOUT}$ maximum	–6	—	6	ns
Δt_{PKJIT}	T	Single period jitter (peak to peak)	PHI @ 120 MHz, Input clock @ 4 MHz	—	—	175	ps
			PHI @ 100 MHz, Input clock @ 4 MHz	—	—	185	ps
			PHI @ 80 MHz, Input clock @ 4 MHz	—	—	200	ps
Δt_{LTJIT}	T	Long term jitter	PHI @ 16 MHz, Input clock @ 4 MHz	—	—	±6	ns
f_{LCK}	D	Frequency LOCK range	—	–6	—	6	% $f_{FMPLLOUT}$
f_{UL}	D	Frequency un-LOCK range	—	–18	—	18	% $f_{FMPLLOUT}$
f_{CS} f_{DS}	D	Modulation depth	Center spread	±0.25	—	±2.0	% $f_{FMPLLOUT}$
			Down spread	–0.5	—	-8.0	
f_{MOD}	D	Modulation frequency[12]	—	—	—	100	kHz

1 Considering operation with FMPLL not bypassed.

2 With FM; the value does not include a possible +2% modulation

3 “Loss of Reference Frequency” window is the reference frequency range outside of which the FMPLL is in self clocked mode.

4 Self clocked mode frequency is the frequency that the FMPLL operates at when the reference frequency falls outside the f_{LOR} window.

5 f_{VCO} is the frequency at the output of the VCO; its range is 256–512 MHz.
f_{SCM} is the self-clocked mode frequency (free running frequency); its range is 20–150 MHz.
$f_{SYS} = f_{VCO} \div ODF$

6 This value is determined by the crystal manufacturer and board design. For 4 MHz to 20 MHz crystals specified for this FMPLL, load capacitors should not exceed these limits.

7 This specification applies to the period required for the FMPLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR).

8 This value is determined by the crystal manufacturer and board design.

9 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{SYS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FMPLL circuitry via V_{DDPLL} and V_{SSPLL} and variation in crystal oscillator frequency increase the C_{JITTER} percentage for a given interval.

10 Proper PC board layout procedures must be followed to achieve specifications.

11 Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of C_{JITTER} and either f_{CS} or f_{DS} (depending on whether center spread or down spread modulation is enabled).

12 Modulation depth is attenuated from depth setting when operating at modulation frequencies above 50 kHz.

The reset sequences shown in Figure 15 and Figure 16 are triggered by functional reset events. $\overline{\text{RESET}}$ is driven low during these two reset sequences ***only if*** the corresponding functional reset source (which triggered the reset sequence) was enabled to drive $\overline{\text{RESET}}$ low for the duration of the internal reset sequence[1].

3.19.3 Reset sequence trigger mapping

The following table shows the possible trigger events for the different reset sequences. It specifies the reset sequence start conditions as well as the reset sequence end indications that are the basis for the timing data provided in Table 31.

Table 32. Reset sequence trigger — reset sequence

Reset Sequence Trigger	Reset Sequence Start Condition	Reset Sequence End Indication	Reset Sequence				
			Destructive Reset Sequence, BIST enabled[1]	*Destructive Reset Sequence, BIST disabled*[1]	*External Reset Sequence Long, BIST enabled*	*Functional Reset Sequence Long*	*Functional Reset Sequence Short*
All internal destructive reset sources (LVDs or internal HVD during power-up and during operation)	Section 3.19.4.1, Destructive reset	Release of $\overline{\text{RESET}}$[2]	triggers		cannot trigger	cannot trigger	cannot trigger
Assertion of $\overline{\text{RESET}}$[3]	Section 3.19.4.2, External reset via RESET		cannot trigger		triggers[4]	triggers[5]	triggers[6]
All internal functional reset sources configured for long reset	Sequence starts with internal reset trigger	Release of $\overline{\text{RESET}}$[7]	cannot trigger		cannot trigger	triggers	cannot trigger
All internal functional reset sources configured for short reset			cannot trigger		cannot trigger	cannot trigger	triggers

1 Whether BIST is executed or not depends on the chip configuration data stored in the shadow sector of the NVM.

2 End of the internal reset sequence (as specified in Table 31) can only be observed by release of $\overline{\text{RESET}}$ if it is not held low externally beyond the end of the internal sequence which would prolong the internal reset PHASE3 till $\overline{\text{RESET}}$ is released externally.

3 The assertion of $\overline{\text{RESET}}$ can only trigger a reset sequence if the device was running ($\overline{\text{RESET}}$ released) before. $\overline{\text{RESET}}$ does not gate a *Destructive Reset Sequence, BIST enabled* or a *Destructive Reset Sequence, BIST disabled*. However, it can prolong these sequences if $\overline{\text{RESET}}$ is held low externally beyond the end of the internal sequence (beyond PHASE3).

1.See RGM_FBRE register for more details.

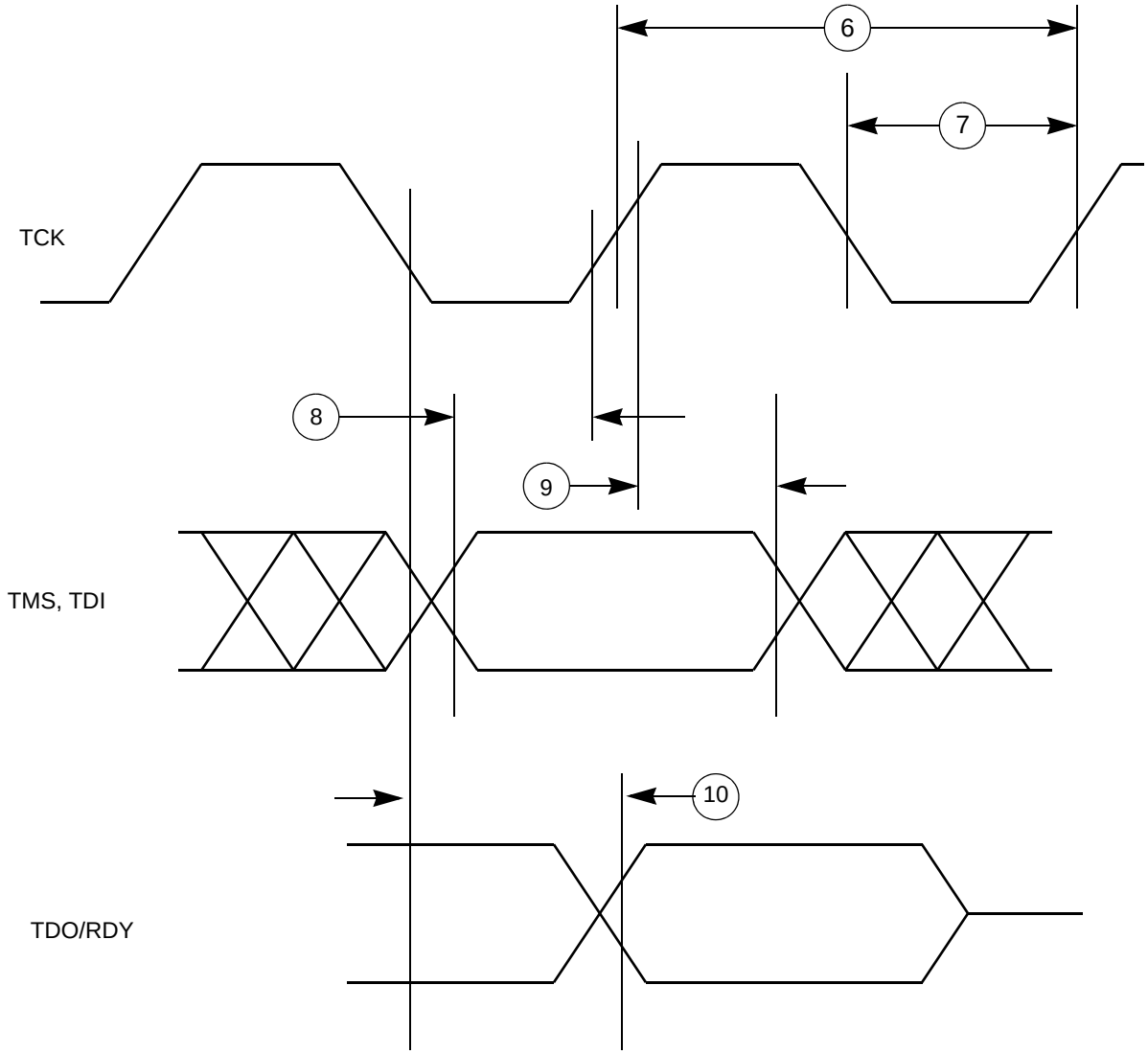


Figure 28. Nexus TDI, TMS, TDO timing

3.20.5 External interrupt timing (IRQ pin)

Table 38. External interrupt timing

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	t_{IPWL}	D	IRQ pulse width low	—	3	—	t_{CYC}
2	t_{IPWH}	D	IRQ pulse width high	—	3	—	t_{CYC}
3	t_{ICYC}	D	IRQ edge to edge time[1]	—	6	—	t_{CYC}

[1] Applies when IRQ pins are configured for rising edge or falling edge events, but not both.

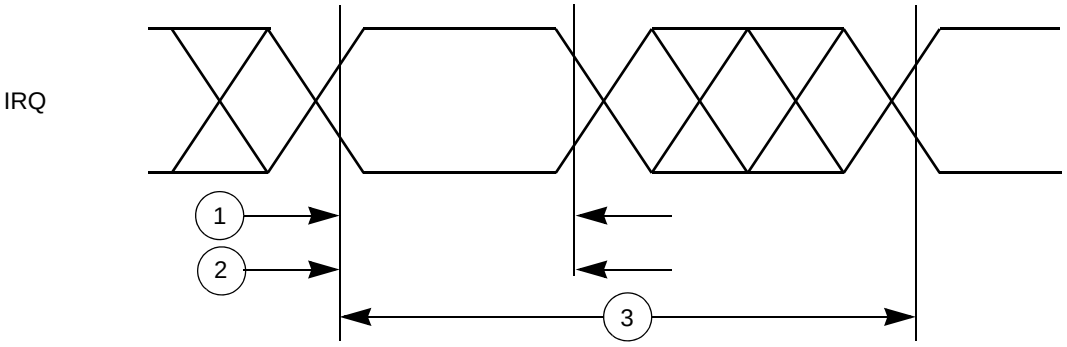
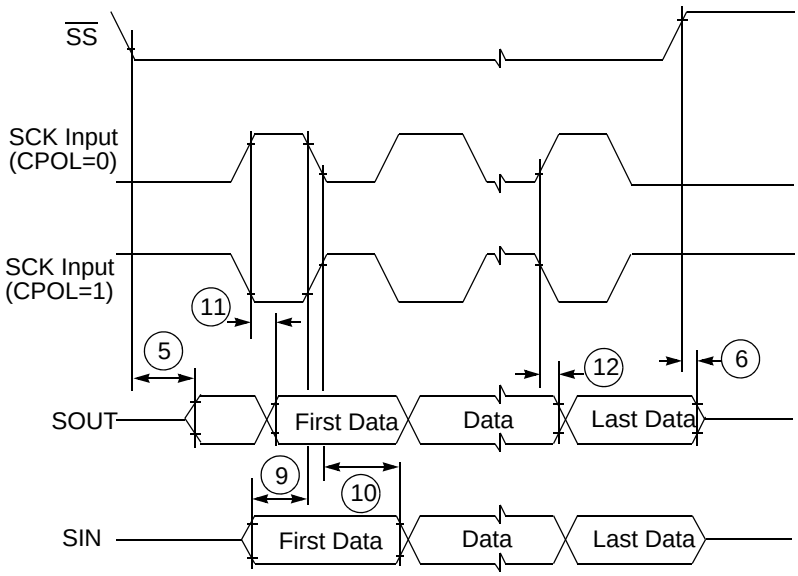


Figure 29. External interrupt timing

3.20.6 DSPI timing

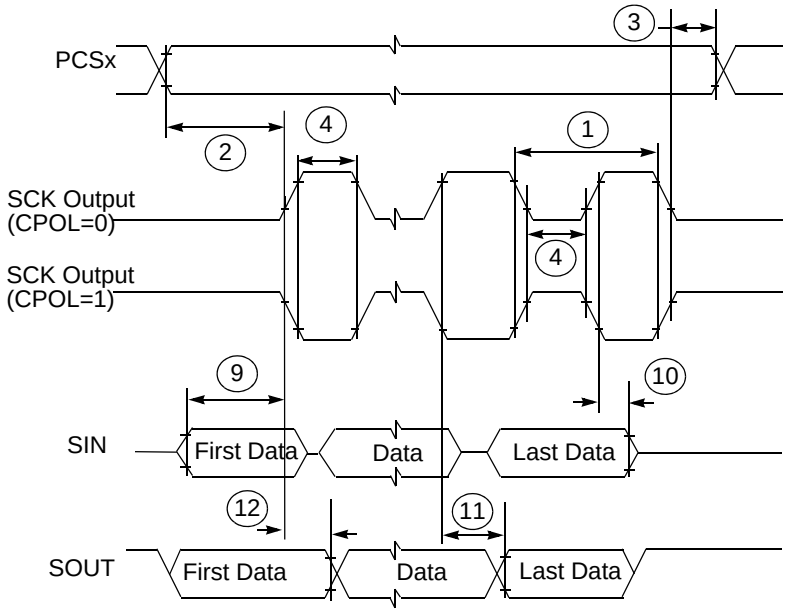
Table 39. DSPI timing

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	t_{SCK}	D	DSPI cycle time	Master (MTFE = 0)	62	—	ns
		D		Slave (MTFE = 0)	62	—	
		D		Slave Receive Only Mode[1]	16	—	
2	t_{CSC}	D	PCS to SCK delay	—	16	—	ns
3	t_{ASC}	D	After SCK delay	—	16	—	ns
4	t_{SDC}	D	SCK duty cycle	—	$t_{SCK}/2$ - 10	$t_{SCK}/2$ + 10	ns
5	t_A	D	Slave access time	$\overline{SS}$ active to SOUT valid	—	40	ns
6	t_{DIS}	D	Slave SOUT disable time	$\overline{SS}$ inactive to SOUT High-Z or invalid	—	10	ns
7	t_{PCSC}	D	PCSx to $\overline{PCSS}$ time	—	13	—	ns
8	t_{PASC}	D	$\overline{PCSS}$ to PCSx time	—	13	—	ns
9	t_{SUI}	D	Data setup time for inputs	Master (MTFE = 0)	20	—	ns
				Slave	2	—	
				Master (MTFE = 1, CPHA = 0)	5	—	
				Master (MTFE = 1, CPHA = 1)	20	—	
10	t_{HI}	D	Data hold time for inputs	Master (MTFE = 0)	–5	—	ns
				Slave	4	—	
				Master (MTFE = 1, CPHA = 0)	11	—	
				Master (MTFE = 1, CPHA = 1)	–5	—	
11	t_{SUO}	D	Data valid (after SCK edge)	Master (MTFE = 0)	—	4	ns
				Slave	—	23	
				Master (MTFE = 1, CPHA = 0)	—	12	
				Master (MTFE = 1, CPHA = 1)	—	4	



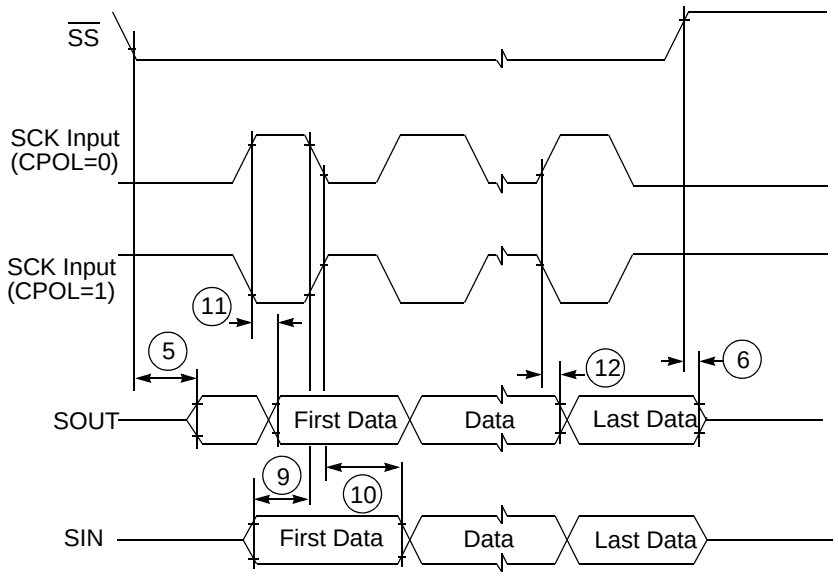
Note: The numbers shown are referenced in Table 39.

Figure 33. DSPI classic SPI timing — slave, CPHA = 1



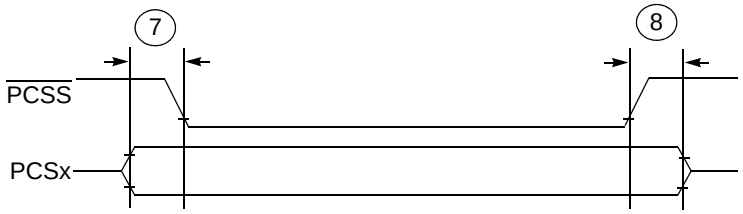
Note: The numbers shown are referenced in Table 39.

Figure 34. DSPI modified transfer format timing — master, CPHA = 0



Note: The numbers shown are referenced in Table 39.

Figure 37. DSPI modified transfer format timing — slave, CPHA = 1



Note: The numbers shown are referenced in Table 39.

Figure 38. DSPI PCS strobe ($\overline{\text{PCSS}}$) timing

4 Package characteristics

4.1 Package mechanical data

Table 40. Orderable part number summary (continued)

Part number[1]	Flash/SRAM	Package	Speed (MHz)[2]	Other features
SPC5643LF2MLQ8	1 MB/128 KB	144 LQFP (Pb free)	80	No FlexRay –40–125 °C
SPC5643LF2MMM8	1 MB/128 KB	257 MAPBGA (Pb free)	80	No FlexRay –40–125 °C
SPC5643LFF2VLQ8	1 MB/128 KB	144 LQFP (Pb free)	80	FlexRay –40–105 °C
SPC5643LFF2VMM8	1 MB/128 KB	257 MAPBGA (Pb free)	80	FlexRay –40–105 °C
SPC5643LF2VLQ8	1 MB/128 KB	144 LQFP (Pb free)	80	No FlexRay –40–105 °C
SPC5643LF2VMM8	1 MB/128 KB	257 MAPBGA (Pb free)	80	No FlexRay –40–105 °C

1 All packaged devices are SPC, rather than MPC or SPC, until product qualifications are complete. The unpackaged device prefix is PCC, rather than SCC, until product qualification is complete. Not all configurations are available in the SPC parts.

2 This speed rating does not include the ±2% for frequency modulation.

6 Document revision history

Table 41 summarizes revisions to this document.

Table 41. Revision history

Revision	Date	Description of changes
1	2 Mar 2009	Initial release.
2	5 May 2009	Updated, Advance Information. —Revised SINAD/SNR specifications. — Updated pinout and pin multiplexing information.
3	5 Oct 2009	Updated, Advance Information, Public release. — Throughout this document, added information for 257 MAPBGA package. — Updated Table 1, MPC5643L device summary. — Updated Section 1.3, Feature Details. — Updated pin-out and pin multiplexing tables. — In Section 3, Electrical characteristics, added symbols for signal characterization methods. — In Table 8, updated maximum ratings. — In Table 10 and Table 11, removed moving-air thermal characteristics. — Updated Section 3.8, Voltage regulator electrical characteristics. — Updated Section 3.14, ADC electrical characteristics. — Updated Section 3.15, Flash memory electrical characteristics. — Updated Section 3.17.1, RESET pin characteristics. — Removed External interrupt timing (IRQ pin) timing specifications. — Updated Section 3.17.6, DSPI timing. — Updated Section 5, Ordering information.

Table 41. Revision history (continued)

Revision	Date	Description of changes
		• Added Table 29 (MPC5643L SWG Specifications) • In Table 29 (MPC5643L SWG Specifications) Added table footnote for Common Mode. Changed text from “internal device pad resistance” to “internal device routing resistance”. • Added Figure 26 in Section 3.20.4, “Nexus timing”. • In Table 30 (Pad AC specifications (3.3 V , IPP_HVE = 0)), removed the row of pad “Pull Up/Downc(3.6 V max)”. • In Table 40 (Orderable part number summary) and Figure 43, updated part numbers (changed ‘PPC’ to ‘SPC’ and ‘F0’ to ‘F2’). • Replaced Figure 39, Figure 40, Figure 41, Figure 42 with the new versions. • InTable 18 (Voltage regulator electrical specifications),changed the symbol of spec external decoupling capacitor from SR to C_{ext}. In Figure 4, changed the ESR range in note text to 1 mW to 100 mW from 30 mW to 150 mW. • In Section 1.5.32, “Sine Wave Generator (SWG)” removed the following text: Frequency range from 1kHz to 50kHz. Sine wave amplitude from 0.47 V to 2.26 V. • In Table 20 (Current consumption characteristics)”,changed symbol from ‘C’ to ‘T’ , added “operating current” to the parameter and updated the maximum value for five additional RunIDD parameters. • In Table 20 (Current consumption characteristics), changed “Conditions” from ‘1.2 V supplies’ to ‘1.2 V supplies during LBIST (full LBIST configuration)’ for all the parameters. • Removed Table “SWG electrical characteristics”. • In Table 18 (Voltage regulator electrical specifications), changed the “Digital supply high voltage detector upper threshold low limit (After a destructive reset initialization phase completion)” from 1.43V to 1.38V. • Added Table 17 (Recommended operating characteristics). • Updated the IDD values in Table 20 (Current consumption characteristics). Changed conditions text from “1.2 supplies during LBIST (full LBIST configuration)” to “1.2 V supplies” for all the IDD parameters except $I_{DD\_LV\_BIST}$+$I_{DD\_LV\_PLL}$. Added footnote in “Conditions” for the DPM mode. • Removed Cut references from the whole document. • In Table 25 (ADC conversion characteristics), changed the sampling frequency value from ‘1 MHz’ to ‘983.6 KHz’.
8.1	07 May 2012	• Deleted the Footer "Preliminary-Subject to Change Without Notice" label.

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