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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Dual-Core
Speed	120MHz
Connectivity	CANbus, FlexRay, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	-
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5643lff2mlq1r

Table of Contents

1 Introduction

1.1 Document overview

This document describes the features of the family and options available within the family members, and highlights important electrical and physical characteristics of the devices.

This document provides electrical specifications, pin assignments, and package diagrams for the MPC5643L series of microcontroller units (MCUs). For functional characteristics, see the *MPC5643L Microcontroller Reference Manual*. For use of the MPC5643Lin a fail-safe system according to safety standard ISO26262, see the *Safety Application Guide for MPC5643L*.

1.2 Description

The MPC5643L series microcontrollers are system-on-chip devices that are built on Power Architecture technology and contain enhancements that improve the architecture's fit in embedded applications, include additional instruction support for digital signal processing (DSP) and integrate technologies such as an enhanced time processor unit, enhanced queued analog-to-digital converter, Controller Area Network, and an enhanced modular input-output system.

The MPC5643L family of 32-bit microcontrollers is the latest achievement in integrated automotive application controllers. It belongs to an expanding range of automotive-focused products designed to address electrical hydraulic power steering (EHPS), electric power steering (EPS) and airbag applications. The advanced and cost-efficient host processor core of the MPC5643L automotive controller family complies with the Power Architecture embedded category. It operates at speeds as high as 120 MHz and offers high-performance processing optimized for low power consumption. It capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with users' implementations.

1.3 Device comparison

Table 1. MPC5643L device summary

Feature		MPC5643L
CPU	Type	2 × e200z4 (in lock-step or decoupled operation)
	Architecture	Harvard
	Execution speed	0–120 MHz (+2% FM)
	DMIPS intrinsic performance	>240 MIPS
	SIMD (DSP + FPU)	Yes
	MMU	16 entry
	Instruction set PPC	Yes
	Instruction set VLE	Yes
	Instruction cache	4 KB, EDC
	MPU-16 regions	Yes, replicated module
	Semaphore unit (SEMA4)	Yes
Buses	Core bus	AHB, 32-bit address, 64-bit data
	Internal periphery bus	32-bit address, 32-bit data
Crossbar	Master × slave ports	Lock Step Mode: 4 × 3 Decoupled Parallel Mode: 6 × 3

  - Individual programmable filters for each mailbox
  - 8 mailboxes configurable as a 6-entry receive FIFO
  - 8 programmable acceptance filters for receive FIFO
- Programmable clock source
  - System clock
  - Direct oscillator clock to avoid FMPLL jitter

1.5.27 FlexRay

The FlexRay module provides the following features:

- Full implementation of FlexRay Protocol Specification 2.1 Rev. A
- 64 configurable message buffers can be handled
- Dual channel or single channel mode of operation, each as fast as 10 Mbit/s data rate
- Message buffers configurable as transmit or receive
- Message buffer size configurable
- Message filtering for all message buffers based on Frame ID, cycle count, and message ID
- Programmable acceptance filters for receive FIFO
- Message buffer header, status, and payload data stored in system memory (SRAM)
- Internal FlexRay memories have error detection and correction

1.5.28 Serial communication interface module (LINFlexD)

The LINFlexD module (LINFlex with DMA support) on this device features the following:

- Supports LIN Master mode, LIN Slave mode and UART mode
- LIN state machine compliant to LIN1.3, 2.0, and 2.1 specifications
- Manages LIN frame transmission and reception without CPU intervention
- LIN features
  - Autonomous LIN frame handling
  - Message buffer to store as many as 8 data bytes
  - Supports messages as long as 64 bytes
  - Detection and flagging of LIN errors (Sync field, delimiter, ID parity, bit framing, checksum and Time-out errors)
  - Classic or extended checksum calculation
  - Configurable break duration of up to 50-bit times
  - Programmable baud rate prescalers (13-bit mantissa, 4-bit fractional)
  - Diagnostic features (Loop back, LIN bus stuck dominant detection)
  - Interrupt driven operation with 16 interrupt sources
- LIN slave mode features
  - Autonomous LIN header handling
  - Autonomous LIN response handling
- UART mode
  - Full-duplex operation
  - Standard non return-to-zero (NRZ) mark/space format
  - Data buffers with 4-byte receive, 4-byte transmit
  - Configurable word length (8-bit, 9-bit, 16-bit, or 17-bit words)
  - Configurable parity scheme: none, odd, even, always 0
  - Speed as fast as 2 Mbit/s

Table 3. 144 LQFP pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
14	A[5]	SIUL	GPIO[5]	GPIO[5]
		DSPI_1	CS0	CS0
		eTimer_1	ETC[5]	ETC[5]
		DSPI_0	CS7	—
		SIUL	—	EIRQ[5]
15	C[7]	SIUL	GPIO[39]	GPIO[39]
		FlexPWM_0	A[1]	A[1]
		SSCM	DEBUG[7]	—
		DSPI_0	—	SIN
16	$V_{DD\_HV\_REG\_0}$	—		
17	$V_{SS\_LV\_COR}$	—		
18	$V_{DD\_LV\_COR}$	—		
19	F[7]	SIUL	GPIO[87]	GPIO[87]
		NPC	MCKO	—
20	F[8]	SIUL	GPIO[88]	GPIO[88]
		NPC	$\overline{\text{MSEO[1]}}$	—
21	$V_{DD\_HV\_IO}$	—		
22	$V_{SS\_HV\_IO}$	—		
23	F[9]	SIUL	GPIO[89]	GPIO[89]
		NPC	$\overline{\text{MSEO[0]}}$	—
24	F[10]	SIUL	GPIO[90]	GPIO[90]
		NPC	$\overline{\text{EVTO}}$	—
25	F[11]	SIUL	GPIO[91]	GPIO[91]
		NPC	—	$\overline{\text{EVTI}}$
26	D[9]	SIUL	GPIO[57]	GPIO[57]
		FlexPWM_0	X[0]	X[0]
		LINFlexD_1	TXD	—
27	$V_{DD\_HV\_OSC}$	—		
28	$V_{SS\_HV\_OSC}$	—		
29	XTAL	—		
30	EXTAL	—		
31	$\overline{\text{RESET}}$	—		

Table 3. 144 LQFP pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
144	A[15]	SIUL	GPIO[15]	GPIO[15]
		eTimer_1	ETC[5]	ETC[5]
		FlexCAN_1	—	RXD
		FlexCAN_0	—	RXD
		SIUL	—	EIRQ[14]

1 V_{PP_TEST} should always be tied to ground (V_{SS}) for normal operations.

Table 4. 257 MAPBGA pin function summary

Pin #	Port/function	Peripheral	Output function	Input function
A1	$V_{SS\_HV\_IO\_RING}$	—		
A2	$V_{SS\_HV\_IO\_RING}$	—		
A3	$V_{DD\_HV\_IO\_RING}$	—		
A4	H[2]	SIUL	GPIO[114]	GPIO[114]
		NPC	MDO[5]	—
A5	H[0]	SIUL	GPIO[112]	GPIO[112]
		NPC	MDO[7]	—
A6	G[14]	SIUL	GPIO[110]	GPIO[110]
		NPC	MDO[9]	—
A7	D[3]	SIUL	GPIO[51]	GPIO[51]
		FlexRay	CB_TX	—
		eTimer_1	ETC[4]	ETC[4]
		FlexPWM_0	A[3]	A[3]
A8	C[15]	SIUL	GPIO[47]	GPIO[47]
		FlexRay	CA_TR_EN	—
		eTimer_1	ETC[0]	ETC[0]
		FlexPWM_0	A[1]	A[1]
		CTU_0	—	EXT_IN
		FlexPWM_0	—	EXT_SYNC
A9	$V_{DD\_HV\_IO\_RING}$	—		
A10	A[12]	SIUL	GPIO[12]	GPIO[12]
		DSPI_2	SOUT	—
		FlexPWM_0	A[2]	A[2]
		FlexPWM_0	B[2]	B[2]
		SIUL	—	EIRQ[11]

Table 4. 257 MAPBGA pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
J12	V_{DD_LV}	—		
J14	V_{DD_LV}	—		
J15	$V_{DD\_HV\_REG\_1}$	—		
J16	$V_{SS\_HV\_FLA}$	—		
J17	H[15]	SIUL	GPIO[127]	GPIO[127]
		FlexPWM_1	B[3]	B[3]
		eTimer_2	ETC[5]	ETC[5]
K1	F[9]	SIUL	GPIO[89]	GPIO[89]
		NPC	$\overline{\text{MSEO[0]}}$	—
K2	F[8]	SIUL	GPIO[88]	GPIO[88]
		NPC	$\overline{\text{MSEO[1]}}$	—
K3	$\overline{\text{RDY}}$	NPC	$\overline{\text{RDY}}$	—
		SIUL	GPIO[132]	GPIO[132]
K4	C[7]	SIUL	GPIO[39]	GPIO[39]
		FlexPWM_0	A[1]	A[1]
		SSCM	DEBUG[7]	—
		DSPI_0	—	SIN
K6	V_{DD_LV}	—		
K7	V_{SS_LV}	—		
K8	V_{SS_LV}	—		
K9	V_{SS_LV}	—		
K10	V_{SS_LV}	—		
K11	V_{SS_LV}	—		
K12	V_{DD_LV}	—		
K14	Not connected	—		
K15	H[8]	SIUL	GPIO[120]	GPIO[120]
		FlexPWM_1	A[1]	A[1]
		DSPI_0	CS6	—
K16	H[7]	SIUL	GPIO[119]	GPIO[119]
		FlexPWM_1	X[1]	X[1]
		eTimer_2	ETC[1]	ETC[1]

Table 4. 257 MAPBGA pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
T15	D[10]	SIUL	GPIO[58]	GPIO[58]
		FlexPWM_0	A[0]	A[0]
		eTimer_0	—	ETC[0]
T16	$V_{DD\_HV\_IO\_RING}$	—		
T17	$V_{SS\_HV\_IO\_RING}$	—		
U1	$V_{SS\_HV\_IO\_RING}$	—		
U2	$V_{SS\_HV\_IO\_RING}$	—		
U3	Not connected	—		
U4	E[4]	SIUL	—	GPIO[68]
		ADC_0	—	AN[7]
U5	C[2]	SIUL	—	GPIO[34]
		ADC_0	—	AN[3]
U6	E[2]	SIUL	—	GPIO[66]
		ADC_0	—	AN[5]
U7	B[9]	SIUL	—	GPIO[25]
		ADC_0 ADC_1	—	AN[11]
U8	B[12]	SIUL	—	GPIO[28]
		ADC_0 ADC_1	—	AN[14]
U9	$V_{DD\_HV\_ADV}$	—		
U10	$V_{SS\_HV\_ADV}$	—		
U11	E[11]	SIUL	—	GPIO[75]
		ADC_1	—	AN[4]
U12	Not connected	—		
U13	Not connected	—		
U14	$V_{DD\_HV\_PMU}$	—		
U15	G[11]	SIUL	GPIO[107]	GPIO[107]
		FlexRay	DBG3	—
		FlexPWM_0	—	FAULT[3]
U16	$V_{SS\_HV\_IO\_RING}$	—		
U17	$V_{SS\_HV\_IO\_RING}$	—		

[1] V_{PP_TEST} should always be tied to ground (V_{SS}) for normal operations.

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed[1]		Pin #		
								SRC = 1	SRC = 0		144 pkg	257 pkg
A[10]	PCR[10]	SIUL	GPIO[10]	ALT0	GPIO[10]	—	—	M	S		118	A13
		DSPI_2	CS0	ALT1	CS0	PSMI[3]; PADSEL=1						
		FlexPWM_0	B[0]	ALT2	B[0]	PSMI[24]; PADSEL=0						
		FlexPWM_0	X[2]	ALT3	X[2]	PSMI[29]; PADSEL=0						
		SIUL	—	—	EIRQ[9]	—						
A[11]	PCR[11]	SIUL	GPIO[11]	ALT0	GPIO[11]	—	—	M	S		120	D11
		DSPI_2	SCK	ALT1	SCK	PSMI[1]; PADSEL=1						
		FlexPWM_0	A[0]	ALT2	A[0]	PSMI[20]; PADSEL=0						
		FlexPWM_0	A[2]	ALT3	A[2]	PSMI[22]; PADSEL=0						
		SIUL	—	—	EIRQ[10]	—						
A[12]	PCR[12]	SIUL	GPIO[12]	ALT0	GPIO[12]	—	—	M	S		122	A10
		DSPI_2	SOUT	ALT1	—	—						
		FlexPWM_0	A[2]	ALT2	A[2]	PSMI[22]; PADSEL=1						
		FlexPWM_0	B[2]	ALT3	B[2]	PSMI[26]; PADSEL=0						
		SIUL	—	—	EIRQ[11]	—						

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed[1]		Pin #		
								SRC = 1	SRC = 0		144 pkg	257 pkg
H[1]	PCR[113]	SIUL	GPIO[113]	ALT0	GPIO[113]	—	—	F	S		—	F1
		NPC	MDO[6]	ALT2	—	—						
H[2]	PCR[114]	SIUL	GPIO[114]	ALT0	GPIO[114]	—	—	F	S		—	A4
		NPC	MDO[5]	ALT2	—	—						
H[3]	PCR[115]	SIUL	GPIO[115]	ALT0	GPIO[115]	—	—	F	S		—	G1
		NPC	MDO[4]	ALT2	—	—						
H[4]	PCR[116]	SIUL	GPIO[116]	ALT0	GPIO[116]	—	—	M	S		—	L16
		FlexPWM_1	X[0]	ALT1	X[0]	—						
		eTimer_2	ETC[0]	ALT2	ETC[0]	PSMI[39]; PADSEL=0						
H[5]	PCR[117]	SIUL	GPIO[117]	ALT0	GPIO[117]	—	—	M	S		—	M17
		FlexPWM_1	A[0]	ALT1	A[0]	—						
		DSPI_0	CS4	ALT3	—	—						
H[6]	PCR[118]	SIUL	GPIO[118]	ALT0	GPIO[118]	—	—	M	S		—	H17
		FlexPWM_1	B[0]	ALT1	B[0]	—						
		DSPI_0	CS5	ALT3	—	—						
H[7]	PCR[119]	SIUL	GPIO[119]	ALT0	GPIO[119]	—	—	M	S		—	K16
		FlexPWM_1	X[1]	ALT1	X[1]	—						
		eTimer_2	ETC[1]	ALT2	ETC[1]	PSMI[40]; PADSEL=0						
H[8]	PCR[120]	SIUL	GPIO[120]	ALT0	GPIO[120]	—	—	M	S		—	K15
		FlexPWM_1	A[1]	ALT1	A[1]	—						
		DSPI_0	CS6	ALT3	—	—						
H[9]	PCR[121]	SIUL	GPIO[121]	ALT0	GPIO[121]	—	—	M	S		—	G16
		FlexPWM_1	B[1]	ALT1	B[1]	—						
		DSPI_0	CS7	ALT3	—	—						

3 Electrical characteristics

3.1 Introduction

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for this device.

This device is designed to operate at 120 MHz. The electrical specifications are preliminary and are from previous designs, design simulations, or initial evaluation. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications will be published after complete characterization and device qualifications have been completed.

The “Symbol” column of the electrical parameter and timings tables contains an additional column containing “SR”, “CC”, “P”, “C”, “T”, or “D”.

- “SR” identifies system requirements—conditions that must be provided to ensure normal device operation. An example is the input voltage of a voltage regulator.
- “CC” identifies controller characteristics—indicating the characteristics and timing of the signals that the chip provides.
- “P”, “C”, “T”, or “D” apply only to controller characteristics—specifications that define normal device operation. They specify how each characteristic is guaranteed.
  - P: parameter is guaranteed by production testing of each individual device.
  - C: parameter is guaranteed by design characterization. Measurements are taken from a statistically relevant sample size across process variations.
  - T: parameter is guaranteed by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values are shown in the typical (“typ”) column are within this category.
  - D: parameters are derived mainly from simulations.

3.2 Absolute maximum ratings

Table 8. Absolute maximum ratings[1]

Symbol		Parameter	Conditions	Min	Max	Unit
$V_{DD\_HV\_REG}$	SR	3.3 V voltage regulator supply voltage	—	–0.3	3.63[2, 3]	V
$V_{DD\_HV\_IOx}$	SR	3.3 V input/output supply voltage	—	–0.3	3.63[2, 3]	V
$V_{SS\_HV\_IOx}$	SR	Input/output ground voltage	—	–0.1	0.1	V
$V_{DD\_HV\_FLA}$	SR	3.3 V flash supply voltage	—	–0.3	3.63[2, 3]	V
$V_{SS\_HV\_FLA}$	SR	Flash memory ground	—	–0.1	0.1	V
$V_{DD\_HV\_OSC}$	SR	3.3 V crystal oscillator amplifier supply voltage	—	–0.3	3.63[2, 3]	V
$V_{SS\_HV\_OSC}$	SR	3.3 V crystal oscillator amplifier reference voltage	—	–0.1	0.1	V
$V_{DD\_HV\_ADR0}$[3,4] $V_{DD\_HV\_ADR1}$	SR	3.3 V / 5.0 V ADC_0 high reference voltage 3.3 V / 5.0 V ADC_1 high reference voltage	—	–0.3	6.0	V
$V_{SS\_HV\_ADR0}$ $V_{SS\_HV\_ADR1}$	SR	ADC_0 ground and low reference voltage ADC_1 ground and low reference voltage	—	–0.1	0.1	V
$V_{DD\_HV\_ADV}$	SR	3.3 V ADC supply voltage	—	–0.3	3.63[2, 3]	V
$V_{SS\_HV\_ADV}$	SR	3.3 V ADC supply ground	—	–0.1	0.1	V

San Jose, CA 95134 USA
(408) 943-6900

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the WEB at http://www.jedec.org.

1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
2. G. Kromann, S. Shidore, and S. Addison, “Thermal Modeling of a PBGA for Air-Cooled Applications,” Electronic Packaging and Production, pp. 53–58, March 1998.
3. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

3.5 Electromagnetic Interference (EMI) characteristics

The characteristics in Table 14 were measured using:

- Device configuration, tet conditions, and EM testing per standard IEC61967-2
- Supply voltage of 3.3 V DC
- Ambient temperature of 25 °C

The configuration information referenced in Table 14 is explained in Table 13.

Table 13. EMI configuration summary

Configuration name	Description
Configuration A	• High emission = all pads have max slew rate, LVDS pads running at 40 MHz • Oscillator frequency = 40 MHz • System bus frequency = 80 MHz • No PLL frequency modulation • IEC level I (≤ 36 dBμV)
Configuration B	• Reference emission = pads use min, mid and max slew rates, LVDS pads disabled • Oscillator frequency = 40 MHz • System bus frequency = 80 MHz • 2% PLL frequency modulation • IEC level K(≤ 30 dBμV)

Table 19. DC electrical characteristics[1] (continued)

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
V_{OH_M}	P	Medium, high level output voltage	I_{OH} = –2 mA	$V_{DD\_HV\_IOx}$ – 0.8	—	—	V
V_{OL_F}	P	Fast, high level output voltage	I_{OL} = 11 mA	—	—	0.5	V
V_{OH_F}	P	Fast, high level output voltage	I_{OH} = –11 mA	$V_{DD\_HV\_IOx}$ – 0.8	—	—	V
V_{OL_SYM}	P	Symmetric, high level output voltage	I_{OL} = 1.5 mA	—	—	0.5	V
V_{OH_SYM}	P	Symmetric, high level output voltage	I_{OH} = –1.5 mA	$V_{DD\_HV\_IOx}$ – 0.8	—	—	V
I_{INJ}	T	DC injection current per pin (all bi-directional ports)	—	–1	—	1	mA
I_{PU}	P	Equivalent pull-up current	$V_{IN} = V_{IL}$	–130	—	—	µA
			$V_{IN} = V_{IH}$	—	—	–10	
I_{PD}	P	Equivalent pull-down current	$V_{IN} = V_{IL}$	10	—	—	µA
			$V_{IN} = V_{IH}$	—	—	130	
I_{IL}	P	Input leakage current (all bidirectional ports)	T_J = –40 to +150 °C	-1	—	1	µA
		Input leakage current (all ADC input-only ports)[4]		-0.25	—	0.25	
		Input leakage current (shared ADC input-only ports)		-0.3	—	0.3	
V_{ILR}	P	$\overline{\text{RESET}}$, low level input voltage	—	–0.1[2]	—	0.35 $V_{DD\_HV\_IOx}$	V
V_{IHR}	P	$\overline{\text{RESET}}$, high level input voltage	—	0.65 $V_{DD\_HV\_IOx}$	—	$V_{DD\_HV\_IOx}$+0.1[2]	V
V_{HYSR}	D	$\overline{\text{RESET}}$, Schmitt trigger hysteresis	—	0.1 $V_{DD\_HV\_IOx}$	—	—	V
V_{OLR}	D	$\overline{\text{RESET}}$, low level output voltage	I_{OL} = 2 mA	—	—	0.5	V
I_{PD}	D	$\overline{\text{RESET}}$, equivalent pull-down current	$V_{IN} = V_{IL}$	10	—	—	µA
			$V_{IN} = V_{IH}$	—	—	130	

1 These specifications are design targets and subject to change per device characterization.

2 “SR” parameter values must not exceed the absolute maximum ratings shown in Table 8.

3 The max input voltage on the ADC pins is the ADC reference voltage VDD_HV_ADRx.

4 Measured values are applicable to all modes of the pad i.e. IBE = 0/1 and / or APC= 0/1.

3.10 Supply current characteristics

Current consumption data is given in Table 20. These specifications are design targets and are subject to change per device characterization.

A real filter can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC filter). The RC filtering may be limited according to the value of source impedance of the transducer or circuit supplying the analog signal to be measured. The filter at the input pins must be designed taking into account the dynamic characteristics of the input signal (bandwidth) and the equivalent input impedance of the ADC itself.

In fact a current sink contributor is represented by the charge sharing effects with the sampling capacitance: C_S and C_{p2} being substantially a switched capacitance, with a frequency equal to the conversion rate of the ADC, it can be seen as a resistive path to ground. For instance, assuming a conversion rate of 1 MHz, with C_{p2} + CS equal to 7.5 pF, a resistance of 133 kΩ is obtained (R_{EQ} = 1 / (fS*(C_{p2}+C_S)), where fS represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on C_s) and the sum of R_S + R_F, the external circuit must be designed to respect the Equation 4:

$$V_A \bullet \frac{R_S + R_F}{R_{EQ}} < \frac{1}{2} LSB \qquad \textit{Eqn. 4}$$

Equation 4 generates a constraint for external network design, in particular on resistive path. Internal switch resistances (R_{SW} and R_{AD}) can be neglected with respect to external resistances.

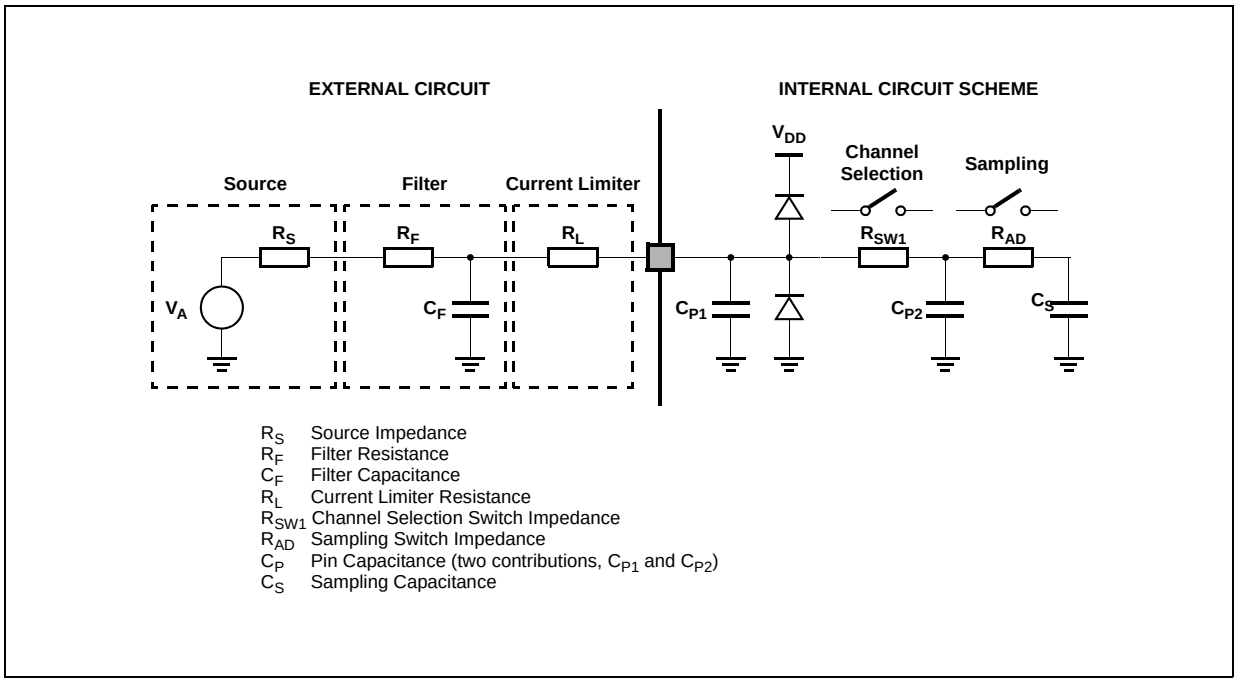


Figure 8. Input Equivalent Circuit

A second aspect involving the capacitance network shall be considered. Assuming the three capacitances C_F, C_{P1} and C_{P2} are initially charged at the source voltage V_A (refer to the equivalent circuit reported in Figure 8): A charge sharing phenomenon is installed when the sampling phase is started (A/D switch close).

Table 29. MPC5643L **SWG Specifications**

Symbol	Parameter	Value		
		Minimum	Typical	Maximum
T	SiNAD[4]	45 dB	—	—
T	Load C	25 pF	—	100 pF
T	Load I	0 μA	—	100 μA
T	ESD Pad Resistance[5]	230 Ω	—	360 Ω

1 Peak to Peak value is measured with no R or I load.

2 Peak to Peak excludes noise, SiNAD must be considered.

3 Common mode value is measured with no R or I load.

4 SiNAD is measured at Max Peak to Peak voltage.

5 Internal device routing resistance. ESD pad resistance is in series and must be considered for max Peak to Peak voltages, depending on application I load and/or R load.

3.18 AC specifications

3.18.1 Pad AC specifications

Table 30. Pad AC specifications (3.3 V , IPP_HVE = 0)[1]

No.	Pad		Tswitchon[1] (ns)			Rise/Fall[2] (ns)			Frequency (MHz)			Current slew[3] (mA/ns)			Load drive (pF)
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
1	Slow	T	3	—	40	—	—	40	—	—	4	0.01	—	2	25
			3	—	40	—	—	50	—	—	2	0.01	—	2	50
			3	—	40	—	—	75	—	—	2	0.01	—	2	100
			3	—	40	—	—	100	—	—	2	0.01	—	2	200
2	Medium	T	1	—	15	—	—	12	—	—	40	2.5	—	7	25
			1	—	15	—	—	25	—	—	20	2.5	—	7	50
			1	—	15	—	—	40	—	—	13	2.5	—	7	100
			1	—	15	—	—	70	—	—	7	2.5	—	7	200
3	Fast	T	1	—	6	—	—	4	—	—	72	3	—	40	25
			1	—	6	—	—	7	—	—	55	7	—	40	50
			1	—	6	—	—	12	—	—	40	7	—	40	100
			1	—	6	—	—	18	—	—	25	7	—	40	200
4	Symmetric	T	1	—	8	—	—	5	—	—	50	3	—	25	25

1 Propagation delay from $V_{DD\_HV\_IOx}/2$ of internal signal to Pchannel/Nchannel switch-on condition.

2 Slope at rising/falling edge.

3 Data based on characterization results, not tested in production.

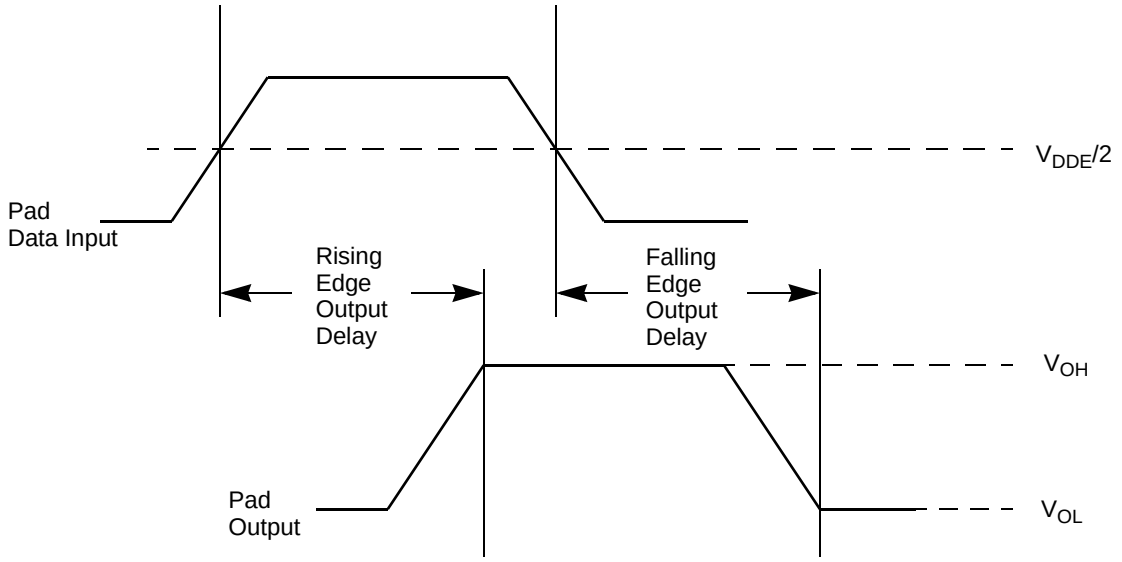


Figure 11. Pad output delay

3.19 Reset sequence

This section shows the duration for different reset sequences. It describes the different reset sequences and it specifies the start conditions and the end indication for the reset sequences.

3.19.1 Reset sequence duration

Table 31 specifies the minimum and the maximum reset sequence duration for the five different reset sequences described in Section 3.19.2, Reset sequence description.

Table 31. RESET sequences

No.	Symbol		Parameter	Conditions	T_{Reset}			Unit
					Min	Typ	Max[1]	
1	T_{DRB}	CC	Destructive Reset Sequence, BIST enabled		28	34	39	ms
2	T_{DR}	CC	Destructive Reset Sequence, BIST disabled	—	500	4200	5000	µs
3	T_{ERLB}	CC	External Reset Sequence Long, BIST enabled		28	32	37	ms
4	T_{FRL}	CC	Functional Reset Sequence Long	—	35	150	400	µs
5	T_{FRS}	CC	Functional Reset Sequence Short	—	1	4	10	µs

1 The maximum value is applicable only if the reset sequence duration is not prolonged by an extended assertion of $\overline{\text{RESET}}$ by an external reset generator.

3.19.2 Reset sequence description

The figures in this section show the internal states of the chip during the five different reset sequences. The doted lines in the figures indicate the starting point and the end point for which the duration is specified in Table 31. The start point and end point

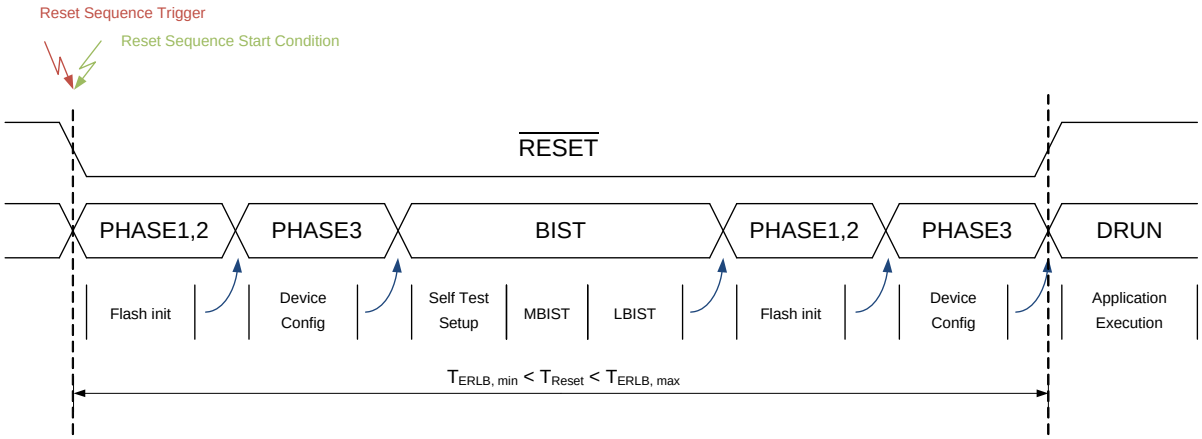


Figure 14. External Reset Sequence Long, BIST enabled

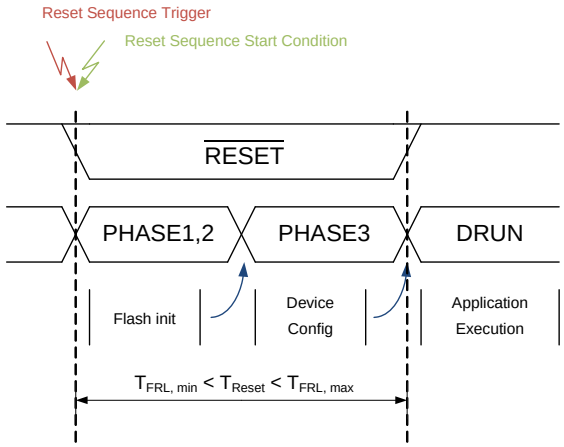


Figure 15. Functional Reset Sequence Long

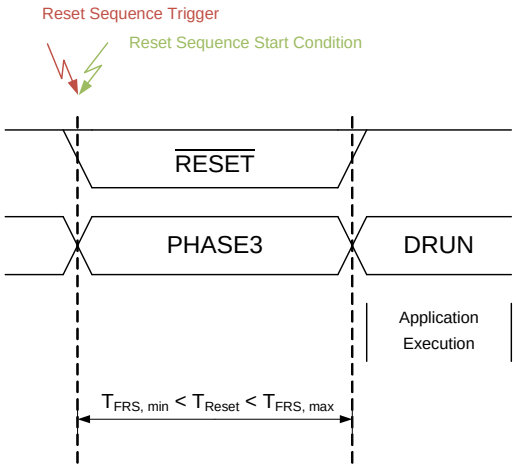


Figure 16. Functional Reset Sequence Short

Table 34. $\overline{\text{RESET}}$ electrical characteristics

No.	Symbol		Parameter	Conditions[1]	Min	Typ	Max	Unit
1	T_{tr}	D	Output transition time output pin[2]	C_L = 25pF	—	—	12	ns
				C_L = 50pF	—	—	25	
				C_L = 100pF	—	—	40	
2	W_{FRST}	P	$\overline{\text{nRESET}}$ input filtered pulse	—	—	—	40	ns
3	W_{NFRST}	P	$\overline{\text{nRESET}}$ input not filtered pulse	—	500	—	—	ns

1 V_{DD} = 3.3 V ± 10%, T_J = –40 to +150 °C, unless otherwise specified

2 C_L includes device and package capacitance (C_{PKG} < 5 pF).

3.20.2 WKUP/NMI timing

Table 35. WKUP/NMI glitch filter

No.	Symbol		Parameter	Min	Typ	Max	Unit
1	W_{FNMI}	D	NMI pulse width that is rejected	—	—	45	ns
2	W_{NFNMI}	D	NMI pulse width that is passed	205	—	—	ns

3.20.3 IEEE 1149.1 JTAG interface timing

Table 36. JTAG pin AC electrical characteristics

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	t_{JCYC}	D	TCK cycle time	—	62.5	—	ns
2	t_{JDC}	D	TCK clock pulse width (measured at V_{DDE}/2)	—	40	60	%
3	$t_{TCKRISE}$	D	TCK rise and fall times (40%–70%)	—	—	3	ns
4	t_{TMSS}, t_{TDIS}	D	TMS, TDI data setup time	—	5	—	ns
5	t_{TMSH}, t_{TDIH}	D	TMS, TDI data hold time	—	25	—	ns
6	t_{TDOV}	D	TCK low to TDO data valid	—	—	20	ns
7	t_{TDOI}	D	TCK low to TDO data invalid	—	0	—	ns
8	t_{TDOHZ}	D	TCK low to TDO high impedance	—	—	20	ns
11	t_{BSDV}	D	TCK falling edge to output valid	—	—	50	ns
12	t_{BSDVZ}	D	TCK falling edge to output valid out of high impedance	—	—	50	ns
13	t_{BSDHZ}	D	TCK falling edge to output high impedance	—	—	50	ns
14	t_{BSDST}	D	Boundary scan input valid to TCK rising edge	—	50	—	ns
15	t_{BSDHT}	D	TCK rising edge to boundary scan input invalid	—	50	—	ns

[3] The system clock frequency needs to be four times faster than the TCK frequency.

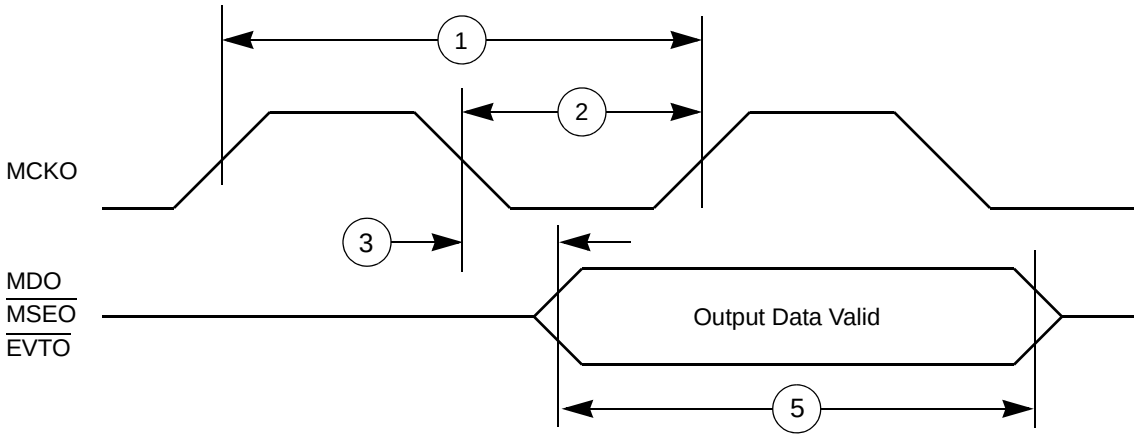


Figure 25. Nexus output timing

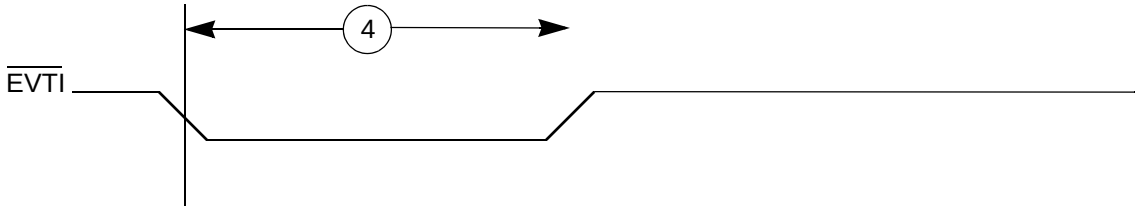
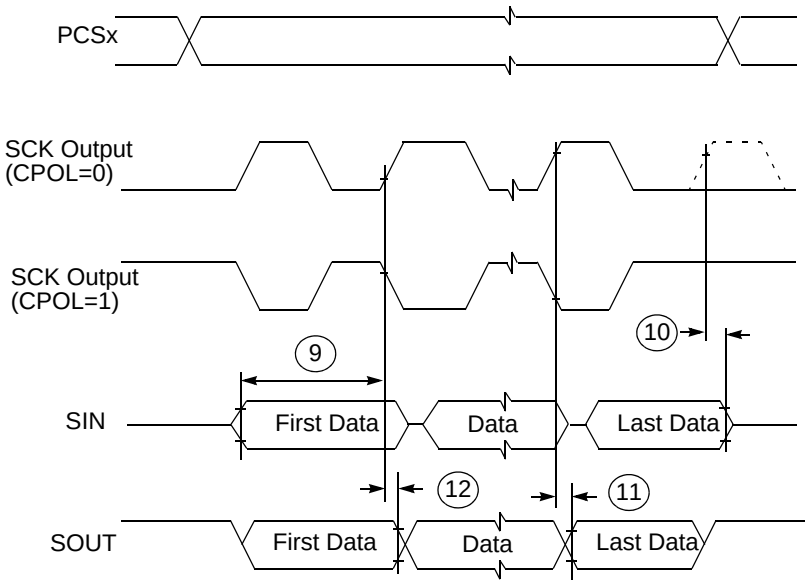
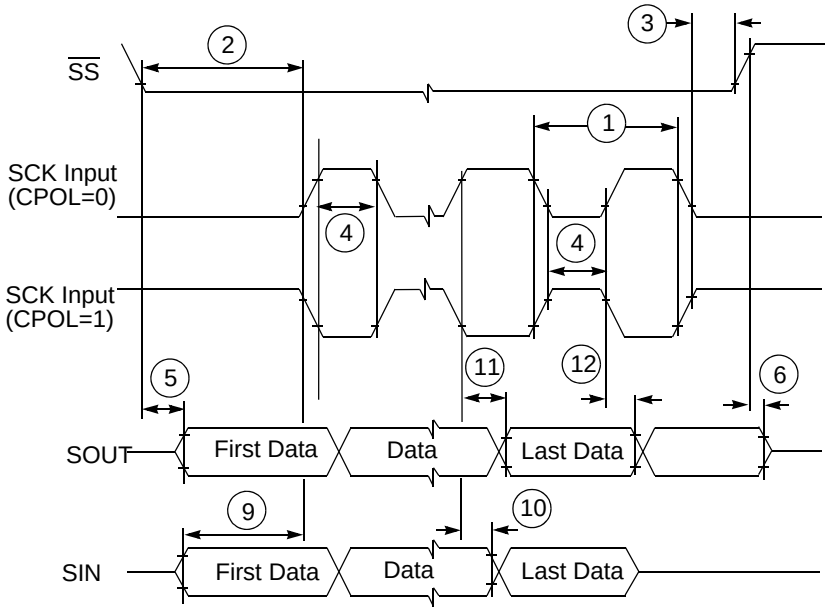


Figure 26. Nexus EVTI Input Pulse Width



Note: The numbers shown are referenced in Table 39.

Figure 35. DSPI modified transfer format timing — master, CPHA = 1



Note: The numbers shown are referenced in Table 39.

Figure 36. DSPI modified transfer format timing – slave, CPHA = 0

Table 41. Revision history (continued)

Revision	Date	Description of changes
5	31 Aug 2010	Editorial changes and improvements. Revised the Overview section. Replaced references to PowerPC with references to Power Architecture. In the feature summary, changed “As much as 128 KB on-chip SRAM” to “128 KB on-chip SRAM”. In the “Feature details” section: • In the “On-chip SRAM with ECC” section, added information about required RAM wait states. • In the PIT section, deleted “32-bit counter for real time interrupt, clocked from main external oscillator” (not supported on this device). • In the flash-memory section, changed “16 KB Test” to “16 KB test sector”, revised the wait state information, and deleted the associated Review_Q&A content. • In the SRAM section, revised the wait state information. In the 144-pin pinout diagram: • Renamed pin 58 (was VDD_HV_ADV0_ADV1, is VDD_HV_ADV). • Renamed pin 59 (was VSS_HV_ADV0_ADV1, is VSS_HV_ADV). In the “144 LQFP pin function summary” table, for pin 39, changed $V_{SS\_LV\_COR}$ to $V_{DD\_LV\_COR}$. In the “Supply pins” table: • Changed the description for $V_{DD\_LV\_COR}$ (was “Voltage regulator supply voltage”, is “Core logic supply”). • Changed the description for $V_{DD\_HV\_PMU}$ (was “Core regulator supply”, is “Voltage regulator supply”). In the “Pin muxing” table: • In the “Pad speed” column headings, changed “SRC = 0” to “SRC = 1” and “SRC = 1” to “SRC = 0” • For port B[6], changed the pad speed for SRC=0 (was M, is F). In the “Thermal characteristics” section, added meaningful values to the thermal-characteristics tables. Added the “SWG electrical specifications” section. In the “Voltage regulator electrical characteristics” section, changed the table title (was “HPREG1, HPREG2, Main LVDs, Digital HVD, and Digital LVD electrical specifications”, is “Voltage regulator electrical characteristics”) and revised the table. In the “BCP68 board schematic example” figure, removed the resistor at the base of the BCP68 transistor. In the “DC electrical characteristics” table: • Changed the guarantee parameter for I_{INJ} (was P, is T). • Added a specification for input leakage current for shared ADC input-only ports. Revised the “Flash memory module life” table. In the “FMPLL electrical characteristics” table, revised the footnote defining f_{SCM} and f_{VCO}. In the “Main oscillator electrical characteristics” table: • Changed the max specification for $g_{mXOSCHS}$ (was 11.8 mA/V, is 13.25 mA/V). • Revised the conditions for $T_{XOSCHSSU}$. In the ‘RC oscillator electrical characteristics” table, deleted the specification for $\Delta_{RCMTRIM}$. Revised the “ADC conversion characteristics” table.
5 (cont.)	31 Aug 2010 (cont.)	In the “$\overline{\text{RESET}}$ pin characteristics” section, changed “n$\overline{\text{RSTIN}}$” to “$\overline{\text{RESET}}$”. Added the “Reset sequence” section. Revised the footnotes in the “Nexus debug port timing” table. In the “Orderable part number summary” table, added a footnote about frequency modulation to the “Speed (MHz)” column heading.