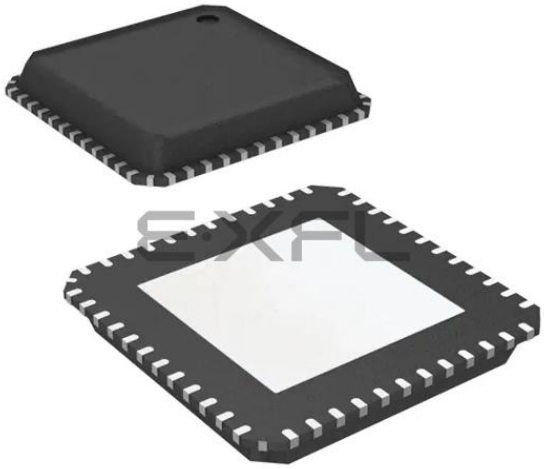

Welcome to E-XFL.COM

Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Automotive
Core Processor	XC800
Program Memory Type	FLASH (48kB)
Controller Series	-
RAM Size	3.25K x 8
Interface	LIN, SSI, UART
Number of I/O	11
Voltage - Supply	3V ~ 27V
Operating Temperature	-40°C ~ 150°C (TJ)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/tle9833qxxuma1

Edition 2012-03-08

Published by
Infineon Technologies AG
81726 Munich, Germany

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (**www.infineon.com**).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

Table of Contents

Table of Contents . . . 3

1 Summary of Features . . . 5
1.1 Device Types / Ordering Information . . . 6
1.2 Abbreviations . . . 7

2 General Device Information . . . 9
2.1 Pin Configuration . . . 9
2.2 Pin Definitions and Functions . . . 10

3 Functional Description . . . 14
3.1 Power Management Unit (PMU) . . . 19
3.1.1 Voltage Regulator 5.0V (VDDP) . . . 22
3.1.2 Voltage Regulator 1.5V (VDDC) . . . 23
3.1.3 External Voltage Regulator 5.0V (VDDEXT) . . . 24
3.2 System Control Unit . . . 25
3.2.1 System Control Unit - Power Modules . . . 25
3.2.2 System Control Unit - Digital Part . . . 26
3.3 XC800 Core . . . 26
3.4 Memory Architecture . . . 28
3.5 Flash Memory . . . 29
3.6 Watchdog Timer 1 (WDT1) . . . 29
3.7 Watchdog Timer (WDT) . . . 31
3.8 Interrupt System . . . 32
3.9 Multiplication/Division Unit . . . 38
3.10 Parallel Ports . . . 38
3.11 Timer 0 and Timer 1 . . . 41
3.12 Timer 2 and Timer 21 . . . 42
3.13 Timer 3 . . . 43
3.14 Capture/Compare Unit 6 (CCU6) . . . 44
3.15 UART . . . 46
3.16 LIN Transceiver . . . 47
3.17 High-Speed Synchronous Serial Interface . . . 47
3.18 Measurement Unit . . . 49
3.19 Measurement Core Module (incl. ADC2) . . . 51
3.20 Analog Digital Converter (ADC1) . . . 52
3.21 High Voltage Monitor Input . . . 53
3.22 High Side Switches . . . 54
3.23 Low Side Switches . . . 55
3.24 PWM Generator . . . 56
3.25 Debug System . . . 57

4 Application Information . . . 58
4.1 Electric Drive Application . . . 58
4.2 Connection of N.C. Pins . . . 59
4.3 Connection of ADCGND Pin . . . 59
4.4 Connection of Exposed Pad . . . 59
4.5 Voltage Regulators-Blocking Capacitors . . . 59
4.6 Additional External Components . . . 59
4.7 ESD Tests . . . 60

5 Electrical Characteristics . . . 61

1.1 Device Types / Ordering Information

The TLE983x product family features devices with different peripheral modules, configurations and program memory sizes to offer cost-effective solutions for different application requirements. Table 1 describes the TLE9833QX device configuration.

Table 1 Device Configuration

Device Name	Max Clock Frequency	High Side Switches	High Voltage Monitor Inputs	Flash Size	Bidirectional Parallel Port I/O´s	Operational Amplifier
TLE9833QX	40 MHz	2	5	48 kByte	11	no

2.2 Pin Definitions and Functions

After reset, all pins are configured as input (except supply and LIN pins) with one of the following settings:

- Pull-up device enabled only (PU)
- Pull-down device enabled only (PD)
- Input with both pull-up and pull-down devices disabled (I)
- Output with output stage deactivated = high impedance state (Hi-Z)

The functions and default states of the TLE9833QX external pins are provided in the following table.

Type: indicates the pin type.

- I/O: Input or output
- I: Input only
- O: Output only
- P: Power supply

Table 3 Pin Definitions and Functions

Symbol	Pin Number	Type	Reset State	Function	
P0				**Port 0** Port 0 is an 6-Bit bidirectional general purpose I/O port. Alternate functions can be assigned as follows: DAP, CCU6, Timer 0, Timer 1, Timer 2, Timer 21, UART, SSC, external interrupt input and clock output.	
P0.0	20	I/O	I/PU	T12HR_0 T2_0 DAP0 EXINT2_3 EXF21_0 RXDO	CCU6 Timer 12 hardware run input Timer 2 input Debug Access Port 0 External interrupt input 0 Timer 21 external flag output UART transmit data output (synchronous mode)
P0.1	17	I/O	I/PU	T13HR_0 RXD_1 T2EX_1 T21_0 EXINT0_3	CCU6 Timer 13 hardware run input UART receive input Timer 2 external trigger input Timer 21 input External interrupt input 0
P0.2	22	I/O	I/PU	$\overline{\text{CTRAP\_0}}$ T21EX_0 EXINT1_3 TXD_1 EXF2_0	CCU6 trap input Timer 21 external trigger input External interrupt input 1 UART transmit output Timer 2 external flag output
P0.3	23	I/O	I/PU	SCK_0 EXINT1_2 T0 CCPOS0_1 EXF21_2	SSC clock input (for slave) / output (for master) External interrupt input 1 Timer 0 input CCU6 hall input 0 Timer 21 external flag output
P0.4	24	I/O	I/PU	MTSR_0 CC60_0 T21_2 EXINT2_2 CCPOS1_1 CLKOUT_0	SSC master transmit output / slave receive input CCU6 capture/compare channel 0 input/output Timer 21 input External interrupt input 2 CCU6 hall input 1 Clock output

3.1.2 Voltage Regulator 1.5V (VDDC)

This module represents the 1.5 V voltage regulator, which serves as core supply for the 8-bit µC and other chip internal analog 1.5 V functions (e.g. 8 Bit ADC). To further reduce the current consumption of the 8-bit MCU during Stop Mode the output voltage is optionally reduced to 0.9 V.

Features

- 1.5 V low-drop voltage regulator
- Optional 0.9 V in Stop Mode
- Current limitation
- Overcurrent monitoring and shutdown with MCU signalling (interrupt)
- Overvoltage monitoring with MCU signalling (interrupt)
- Undervoltage monitoring with MCU signalling (interrupt)
- Pull-down current source at the output for Sleep Mode (100 µA)

The output capacitor C_{VDDC} is mandatory to ensure a proper regulator functionality.

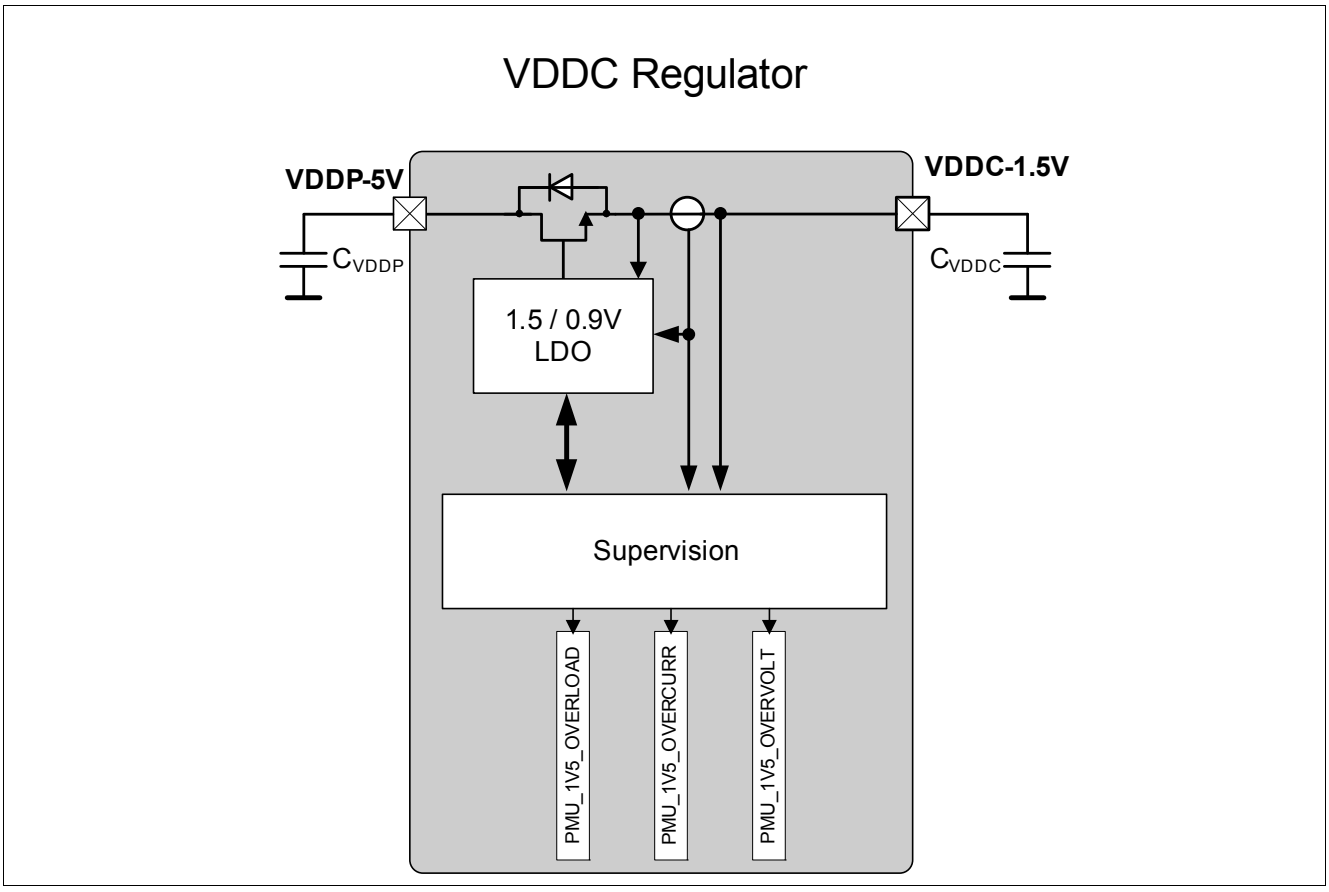

Figure 7 Module Block Diagram of VDDC Voltage Regulator

3.2 System Control Unit

3.2.1 System Control Unit - Power Modules

The System Control Unit of the power modules consists of the following sub-modules:

- Reset Control Unit (RCU): generation of all required subsystem resets
- Clock Generation Unit (CGU): providing all required clocks to the analog subsystem
- Interrupt Control Unit (ICU): all system relevant interrupt flags and status flags
- Power Control Unit (PCU): takes over control when device enters and exits Sleep Mode and Stop Mode
- System Status Unit (SSU): controls mode changes due to system failures
- External Watchdog (WDT1): independent system watchdog to monitor system activity

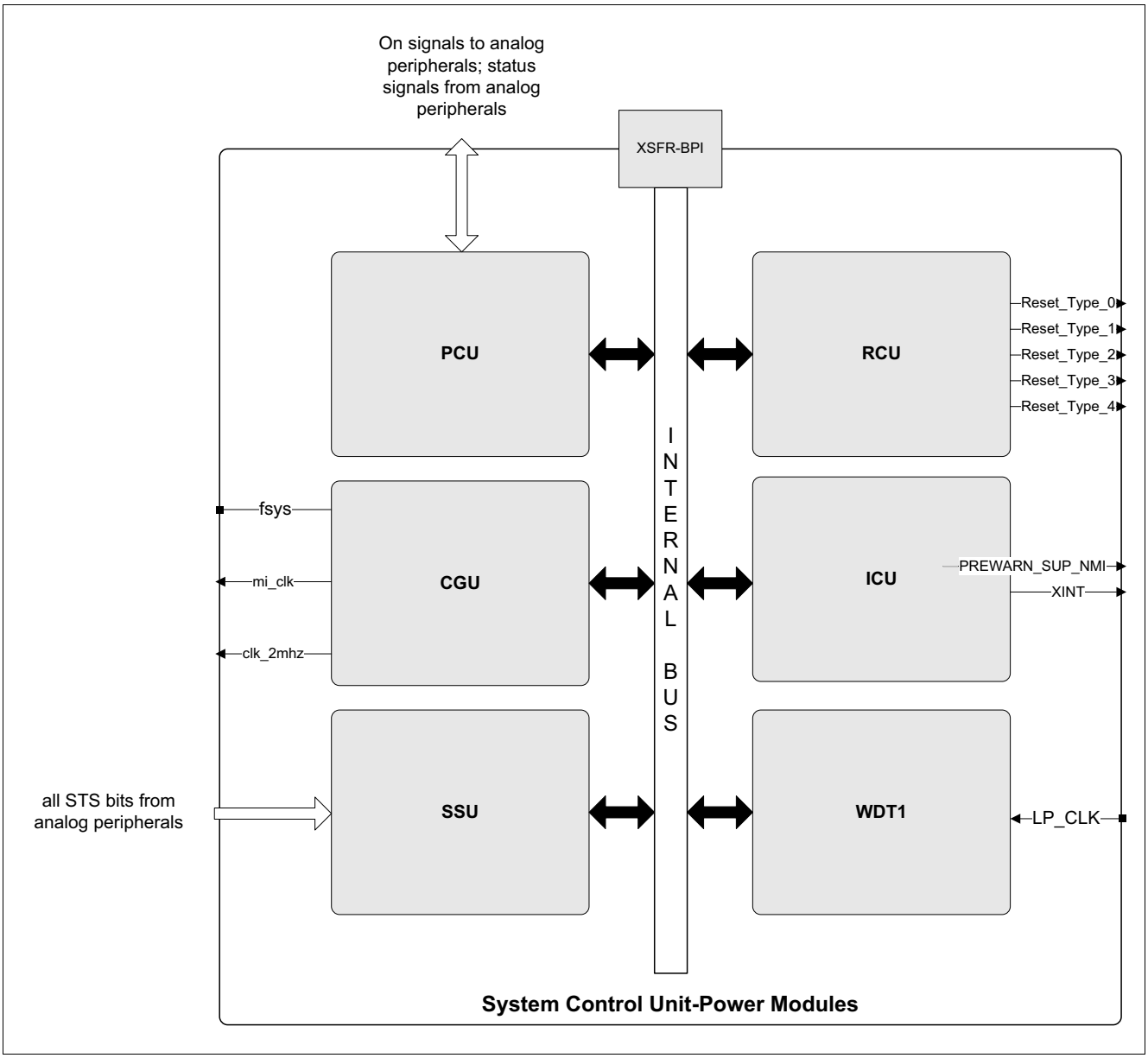

Figure 9 Block Diagram of System Control Unit - Power Modules

Figure 10 shows the functional blocks of the XC800 Core. The XC800 Core consists mainly of the instruction decoder, the arithmetic section, the program control section, the access control section, and the interrupt controller.

The instruction decoder decodes each instruction and accordingly generates the internal signals required to control the functions of the individual units within the core. These internal signals have an effect on the source and destination of data transfers and control the ALU processing.

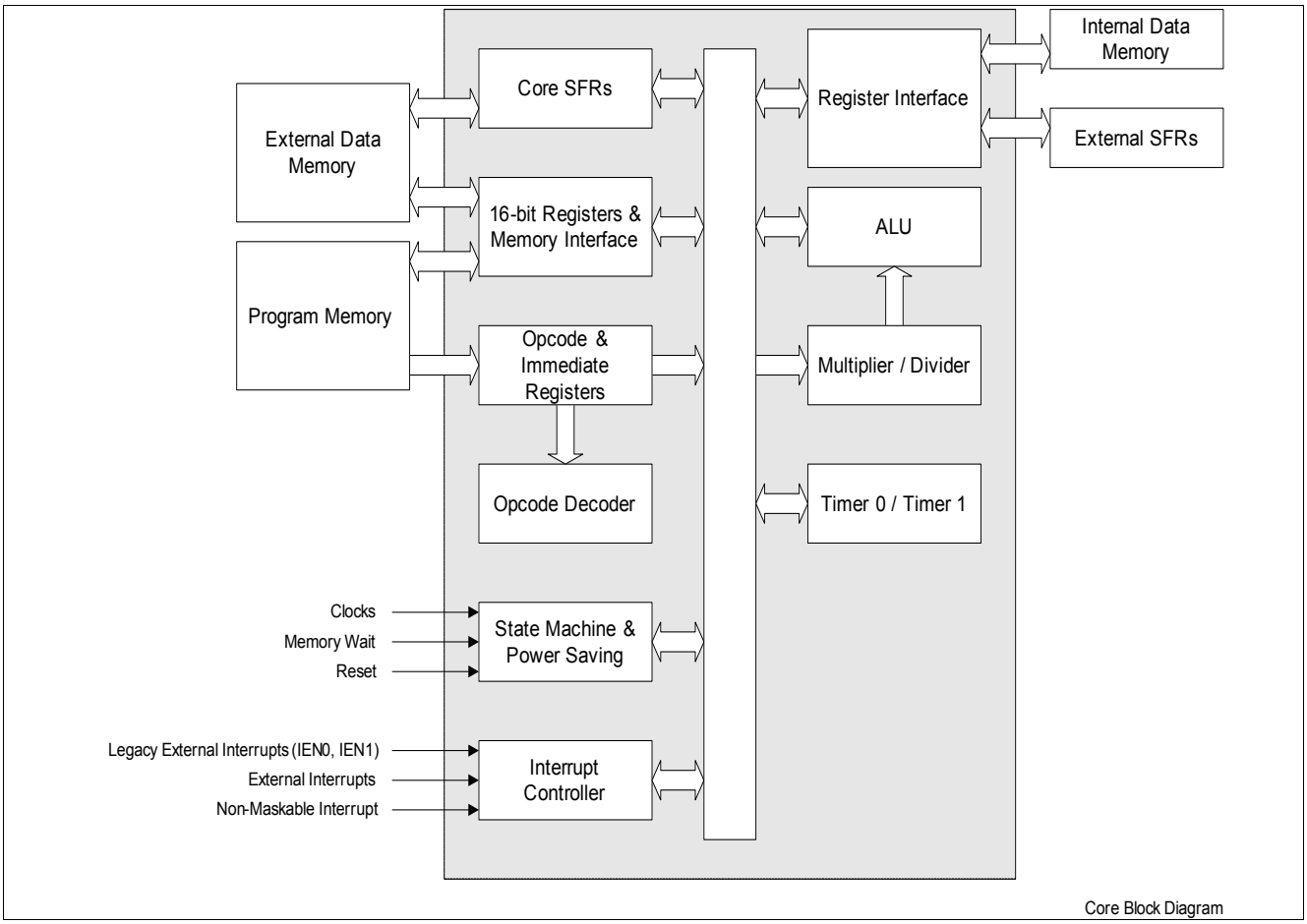

Figure 10 XC800 Core Block Diagram

The arithmetic section of the processor performs extensive data manipulation and consists of the arithmetic/logic unit (ALU), A register, B register and PSW register. The ALU accepts 8-Bit data words from one or two sources and generates an 8-Bit result under the control of the instruction decoder. The ALU performs both arithmetic and logic operations. Arithmetic operations include add, subtract, multiply, divide, increment, decrement, BCD-decimal-add-adjust and compare. Logic operations include AND, OR, Exclusive OR, complement and rotate (right, left or swap nibble (left four)). Also included is a Boolean unit performing the Bit operations as set, clear, complement, jump-if-set, jump-if-not-set, jump-if-set-and-clear and move to/from carry. The ALU can perform the Bit operations of logical AND or logical OR between any addressable Bit (or its complement) and the carry flag, and place the new result in the carry flag.

The program control section controls the sequence in which the instructions stored in program memory are executed. The 16-Bit program counter (PC) holds the address of the next instruction to be executed. The conditional branch logic enables internal and external events to the processor to cause a change in the program execution sequence.

The access control unit is responsible for the selection of the on-chip memory resources. The interrupt requests from the peripheral units are handled by the interrupt controller unit.

3.11 Timer 0 and Timer 1

Timer 0 and Timer 1 can function as both, timers or counters. When functioning as a timer, Timer 0 and Timer 1 are incremented with every machine cycle, i.e. every 2 input clocks (or 2 PCLKs). When functioning as a counter, Timer 0 and Timer 1 are incremented in response to a 1-to-0 transition (falling edge) at its respective external input pins, T0 or T1. Timer 0 and Timer 1 are fully compatible and can be configured in four different operating modes to use in a variety of applications, see **Table 6**. In modes 0, 1 and 2, the two timers operate independently, but in mode 3, their functions are specialized.

Table 6 Timer 0 and Timer 1 Modes

Mode	Operation
0	**13-Bit-timer** The timer is essentially an 8-Bit counter with a divide-by-32 prescaler. This mode is included solely for compatibility with Intel 8048 devices.
1	**16-Bit-timer** The timer registers, TLx and THx, are concatenated to form a 16-Bit counter.
2	**8-Bit timer with auto-reload** The timer register TLx is reloaded with a user-defined 8-Bit value in THx upon overflow.
3	**Timer 0 operates as two 8-Bit timers** The timer registers, TL0 and TH0, operate as two separate 8-Bit counters. Timer 1 is halted and retains its count even if enabled.

Additional Specific Functions

- Block commutation for brushless DC-drives implemented
- Position detection via hall sensor pattern
- Noise filter supported for position input signals
- Automatic rotational speed measurement and commutation control for block commutation
- Integrated error handling
- Fast emergency stop without CPU load via external signal ($\overline{\text{CTRAP}}$)
- Control modes for multi-channel AC-drives
- Output levels can be selected and adapted to the power stage

The Timer T12 can work in capture and/or compare mode for its three channels. The modes can also be combined (e.g. a channel works in compare mode, whereas another channel works in capture mode). The Timer T13 can work in compare mode only. The multi-channel control unit generates output patterns which can be modulated by T12 and/or T13. The modulation sources can be selected and combined for the signal modulation.

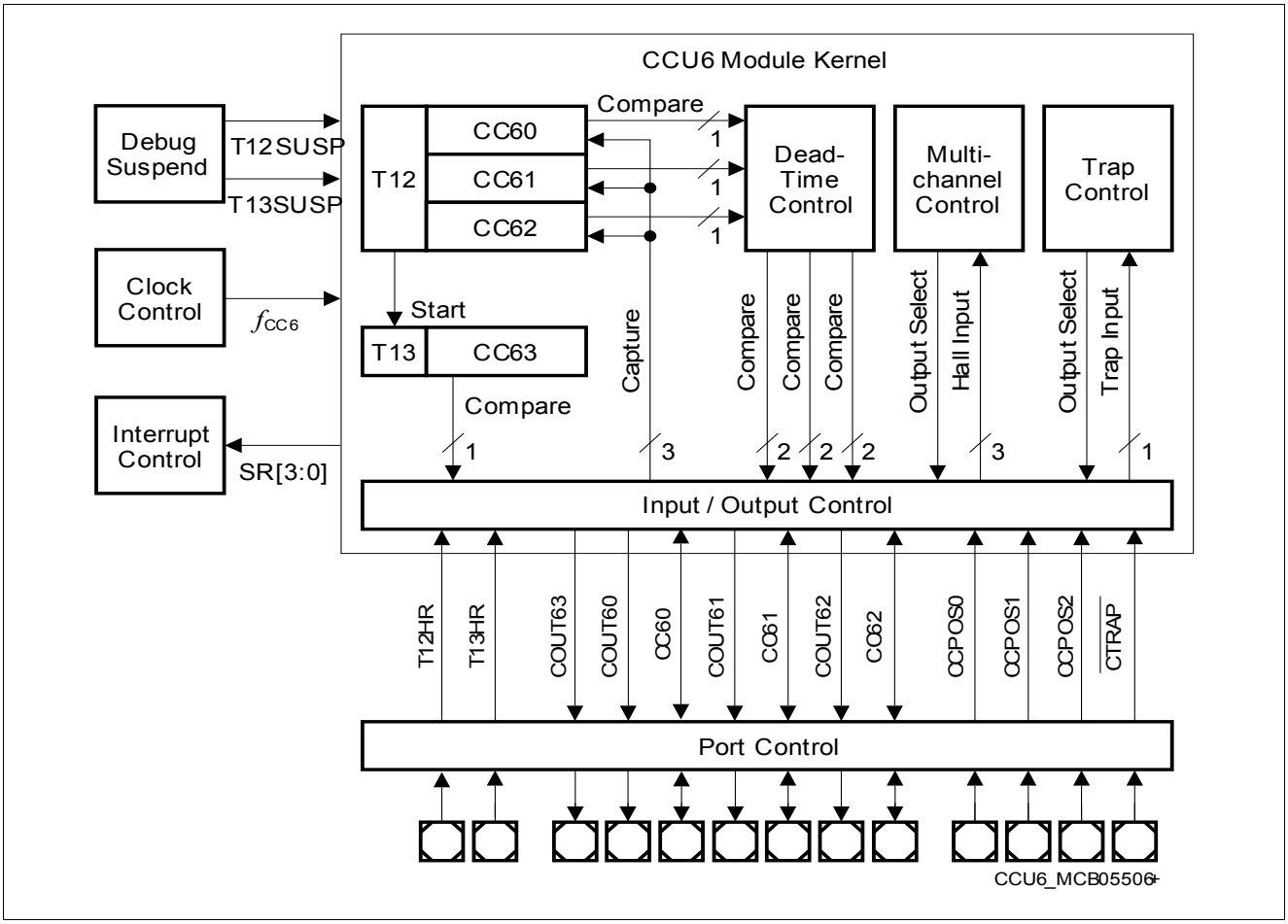

Figure 22 CCU6 Block Diagram

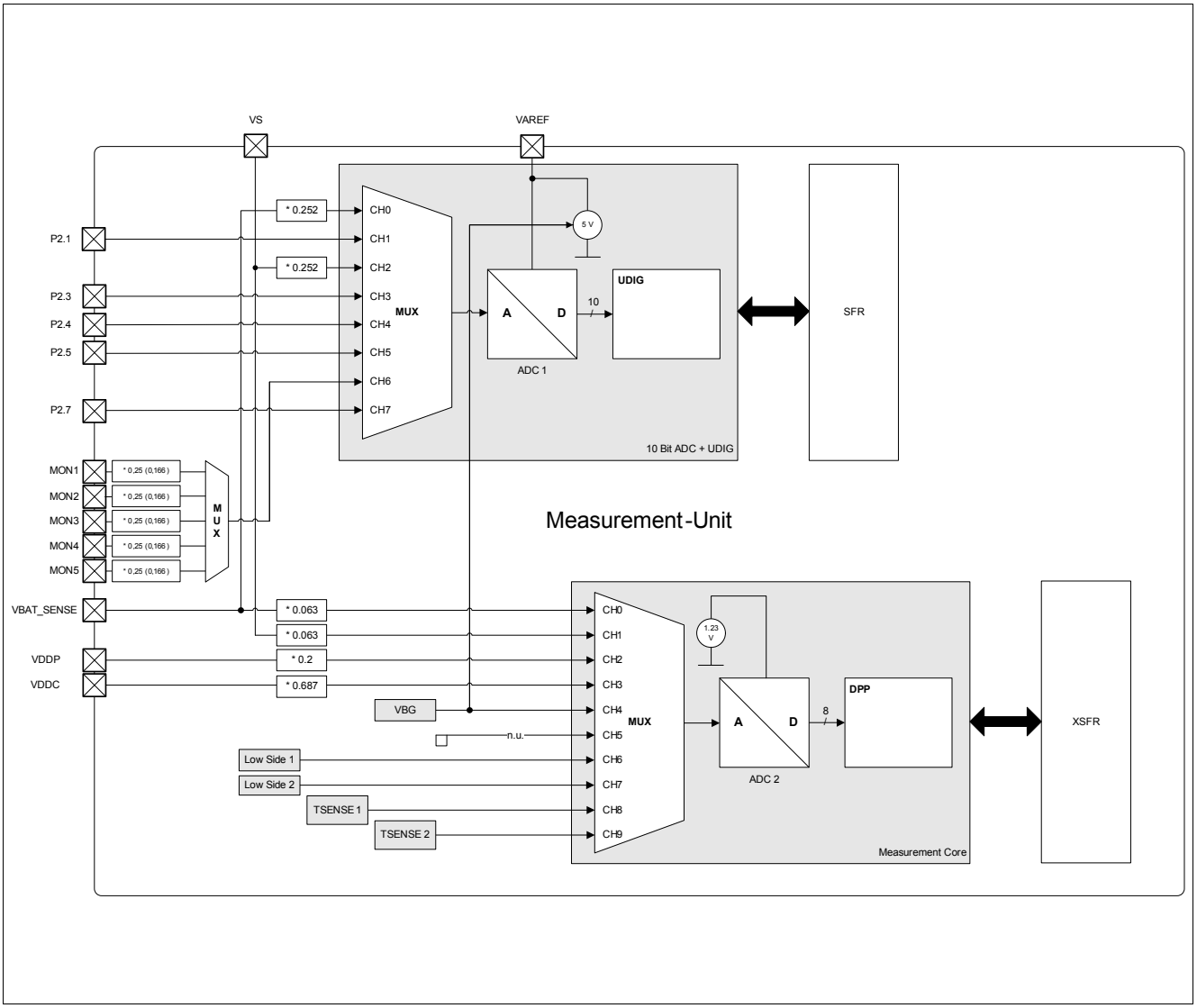

Figure 25 TLE9833QX Measurement Unit-Overview

3.21 High Voltage Monitor Input

This module is dedicated to monitor external voltage levels above or below a specified threshold or it can be used to detect a wake-up event at each high-voltage MON_IN pin in low-power mode. Each input is sensitive to an input level monitoring. It is available when the module is switched to Active Mode via the MON_int (internal signal name) output with a small filter delay of typical 2 µs.

Features

- High-voltage input with V_S/2 threshold voltage
- Edge sensitive wake capability for power saving modes
- Level sensitive wake-up feature configurable for transitions from low to high, high to low or both directions
- MON inputs can also be evaluated with ADC1 in Active Mode, using adjustable threshold values (see also **Chapter 3.20**).

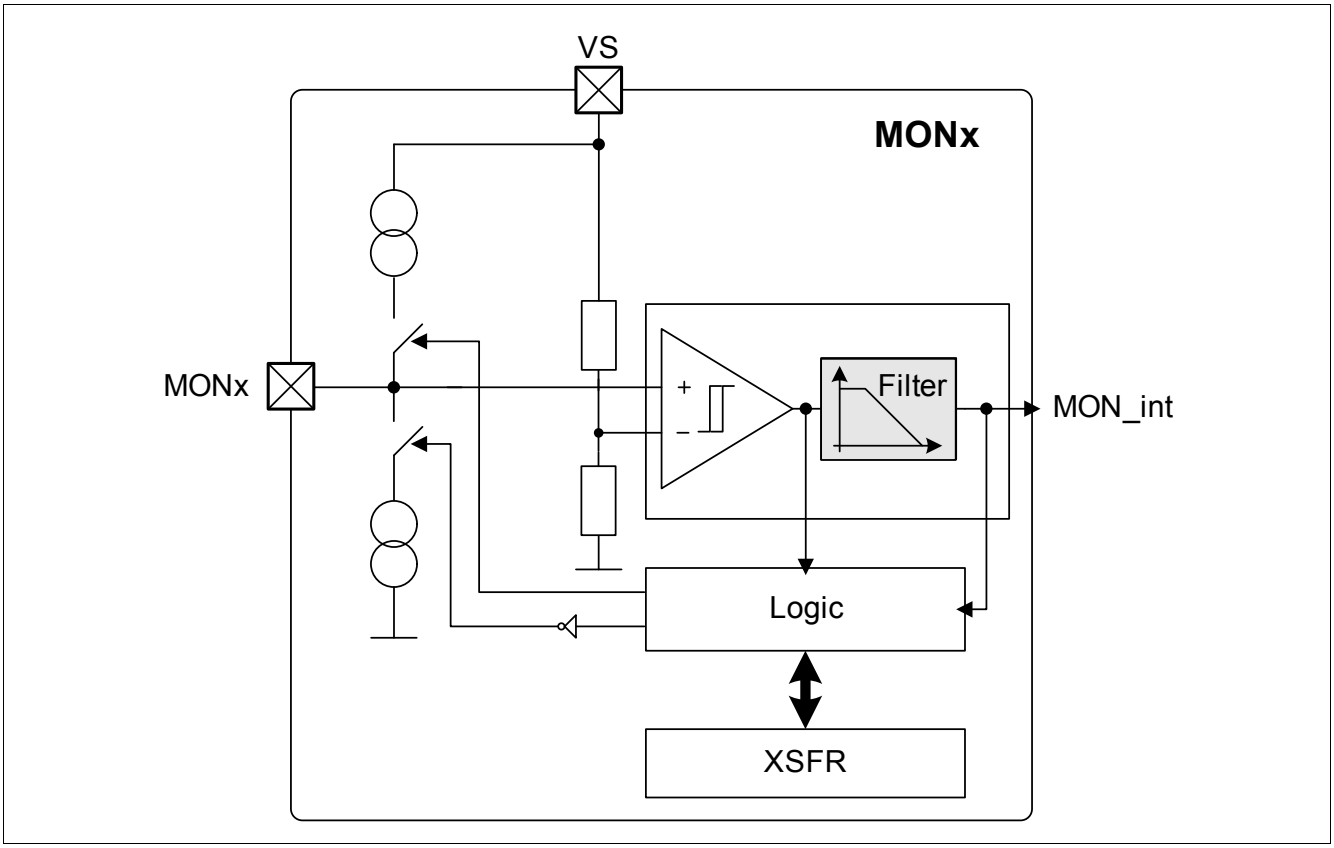

Figure 27 Monitoring Input Block Diagram

4.2 Connection of N.C. Pins

It is recommended to connect N.C. pins to GND unless otherwise specified. Since pins 10 and 46 are located next to high voltage pins (VS, MON5, LS1) these 2 N.C. pins can be also left unconnected in order to avoid huge current flow and damage of the system in case of short-circuit.

4.3 Connection of ADCGND Pin

The ADCGND pin is chip-internal connected to reference ground. In order to provide full offset compensation and achieve full accuracy of ADC1 the ADCGND pin must not be connected to board ground. ADCGND pin should be connected with a capacitor (100 nF) to VAREF only.

4.4 Connection of Exposed Pad

It is recommended to connect the exposed pad to GND.

4.5 Voltage Regulators-Blocking Capacitors

Table 11 External Component Recommendation

Symbol	Function	Comment
C_{VS}	blocking capacitor at VS pin	> 20 µF Elco + 100 nF Ceramic, ESR < 1 Ω
C_{VDDP}	blocking capacitor at VDDP pin	1 µF typ. + 100 nF Ceramic, ESR < 1 Ω
C_{VDDEXT}	blocking capacitor at VDDEXT pin	100 nF typ., ESR < 1 Ω
C_{VDDC}	blocking capacitor at VDDC pin	> 330 nF + 100 nF Ceramic, ESR < 1 Ω
C_{VAREF}	blocking capacitor at VAREF pin	> 100 nF, ESR < 1 Ω

4.6 Additional External Components

Table 12 External Component Recommendation

Symbol	Function	Comment
C_{HSx}	HF blocking capacitor at HSx pin	6.8 nF
R_{MONx}	resistor at MONx pin	1 kΩ
$R_{VBAT\_}$	resistor at VBAT_SENSE pin	1 kΩ

5.1.3 Current Consumption

Table 16 Electrical Characteristics [1)]

V_s = 5.5V to 18V, T_J = -40°C to 85°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Current Consumption @VS pin							
Current Consumption in Active Mode	I_{Active}	–	30	40	mA	fsys = 40 MHz no loads on pins, LIN in recessive state, LS1, LS2, HS1 and HS2 off	P_5.1.25
Current consumption in Stop Mode	$I_{Powerdown}$	–	85	95	µA	microcontroller in Stop Mode, LIN recessive state, MON1-5 disabled, GPIOs open (no loads)	P_5.1.26
Current consumption in Stop Mode with cyclic sense enabled	$I_{Powerdown2}$	–	–	110	µA	microcontroller in Stop Mode, LIN recessive state, GPIOs open (no loads)	P_5.1.27
Current consumption in Sleep Mode	I_{Sleep}	–	–	25	µA	system in Sleep Mode, microcontroller not powered, LIN recessive state, MON1-5 disabled and GPIOs open (no loads)	P_5.1.28

1) Not subject to production test, specified by design.

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

5.1.4 Thermal Resistance

Table 17 Thermal Resistance

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Junction to Ambient	R_{thJA}	–	23.9	–	K/W	1)	P_5.1.29

1) EIA/JESD 52_2, FR4, 76.2 x 114.3 x 1.5 mm; 35µ Cu, 5µ Sn; 300 mm^2

5.2 Power Management Unit (PMU)

This chapter includes all electrical characteristics of the Power Management Unit

5.2.1 PMU I/O Supply Parameters VDDP

Table 19 Electrical Characteristics

V_S = 5.5 V to 27 V, T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Specified Output Current	I_{VDDP}	0	–	60	mA	1)	P_5.2.1
Required Output Capacitance	C_{VDDP}	0.1	–	10	µF	1) ESR < 1Ω	P_5.2.2
Output Voltage including line regulation	V_{DDPOUT}	4.9	5.0	5.1	V	I_{load} < 90mA;Vs > 5.5V	P_5.2.3
Output Drop	$Vs_{V\ DDPout}$	–	–	+400	mV	I_{load} < 70mA; 3V < V_s < 5.5V	P_5.2.4
Dynamic Load Regulation	$V_{VDDPLOR}$	-50	–	50	mV	1) 2 ... 70mA; C=470nF; dI/dt=100mA/µs	P_5.2.5
Dynamic Line Regulation	$V_{VDDPLIR}$	-25	–	25	mV	1) V_s= 5.5 ... 20V; dV/dt=5V/µs	P_5.2.6
Power Supply Ripple Rejection	$P_{SSRVDDP}$	50	–	–	dB	1) V_s= 13.5V; f=0 ... 1KHz; Vr=2Vpp	P_5.2.7
Over Voltage Detection	V_{DDPOV}	5.05	–	5.4	V	V_s > 5.5V; Overvoltage leads to SUPPLY_NMI	P_5.2.8
Under Voltage Reset	V_{DDPUV}	2.4	–	2.7	V	V_s > 5.5V	P_5.2.9
Over Current Shutdown	I_{VDDPOC}	90	–	180	mA	–	P_5.2.10

1) Not subject to production test, specified by design

5.2.2 PMU Core Supply Parameters VDDC

Table 20 Electrical Characteristics

V_S = 5.5 V to 27 V, T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Specified Output Current	I_{VDDC}	0	–	30	mA	1) only used as internal core supply	P_5.2.11
Required Output Capacitance	C_{VDDC}	0.1	–	10	µF	2) ESR < 1Ω	P_5.2.12
Output Voltage including line regulation @ Active Mode	V_{DDCOUT}	1.44	1.5	1.56	V	I_{load} < 40mA	P_5.2.13
Output Voltage including line regulation @ Stop Mode	V_{DDCOUT}	0.89	0.95	1.15	V	I_{load} < 200µA	P_5.2.14
Dynamic Load Regulation	V_{DDCLOR}	-50	–	50	mV	2) 2 ... 30mA; C=330nF; dI/dt=100mA/µs	P_5.2.15
Dynamic Line Regulation	V_{DDCLIR}	-25	–	25	mV	2) V_{DDP}= 2.5 ... 5.5V; dV/dt=5V/µs	P_5.2.16
Over Voltage Detection	V_{DDCOV}	1.61	–	1.68	V	Overvoltage leads to SUPPLY_NMI	P_5.2.17
Under Voltage Reset	V_{DDVUV}	1.10	–	1.19	V	–	P_5.2.18
Over Current Shutdown	I_{VDDCOC}	35	–	80	mA	–	P_5.2.19

1) VDDC is not intended to be used as external voltage regulator

2) Not subject to production test, specified by design

Table 27 Current Limits for Port Output Drivers[1)]

Port Output Driver Mode	Maximum Output Current (I_{OLmax} , - I_{OHmax})		Nominal Output Current (I_{OLnom} , - I_{OHnom})		Number
	VDDP ≥ 4.5V	VDDP < 4.5V	VDDP ≥ 4.5V	VDDP < 4.5V	
Strong Driver	7.5 mA	7.5 mA	2.5 mA	2.5 mA	P_5.5.16
Medium Driver	4 mA	2.5 mA	1.0 mA	1.0 mA	P_5.5.17
Weak Driver	0.5 mA	0.5 mA	0.1 mA	0.1 mA	P_5.5.18

1) Not subject to production test, specified by design.

Note: Stresses above the values listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for an extended time may affect device reliability.
During absolute maximum rating overload conditions ($V_{IN} > V_{DDP}$ or $V_{IN} < GND$) the voltage on V_{DDP} pins with respect to ground (GND) must not exceed the values defined by the absolute maximum ratings.

Table 28 Electrical Characteristics (cont'd) **LIN Transceiver**

V_s = 5.5V - 18V, T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Duty cycle D3 (for worst case at 10,4 kBit/s)	t_{duty1}	0.417	–	–		[7] duty cycle 3 TH_{Rec}(max) = 0.778 × V_S; TH_{Dom}(max) = 0.616 × V_S; V_S = 5.5 … 18 V; t_{bit} = 96 µs; D3 = $t_{bus\_rec(min)}$/2 t_{bit}; LIN Spec 2.1 (Par. 29)	P_5.6.24
Duty cycle D4 (for worst case at 10,4 kBit/s)	t_{duty2}	–	–	0.590		duty cycle 4 TH_{Rec}(max) = 0.389 × V_S; TH_{Dom}(max) = 0.251 × V_S; V_S = 5.5 … 18 V; t_{bit} = 96 µs; D4 = $t_{bus\_rec(max)}$/2 t_{bit}; LIN Spec 2.1 (Par. 30)	P_5.6.25
AC Characteristics - Transceiver Fast Slope Mode							
Propagation delay bus dominant to RxD LOW	$t_{d(L),R}$	0.1	1	6	µs	–	P_5.6.26
Propagation delay bus recessive to RxD HIGH	$t_{d(H),R}$	0.1	1	6	µs	–	P_5.6.27
Receiver delay symmetry	$t_{sym,R}$	-1	–	1	µs	$t_{sym,R}$ = $t_{d(L),R}$ - $t_{d(H),R}$;	P_5.6.28
Duty cycle D5 (for worst case at 40 kBit/s)	t_{duty1}	0.395	–	–		[6] duty cycle 5 TH_{Rec}(max) = 0.744 × V_S; TH_{Dom}(max) = 0.581 × V_S; V_S = 5.5 … 18 V; t_{bit} = 25µs; D1 = $t_{bus\_rec(min)}$/2 t_{bit};	P_5.6.29
Duty cycle D6 (for worst case at 40 kBit/s)	t_{duty2}	–	–	0.581		[6] duty cycle 6 TH_{Rec}(max)= 0.422 × V_S; TH_{Dom}(max)= 0.284 × V_S; V_S = 5.5 … 18 V; t_{bit} = 25 µs; D2 = $t_{bus\_rec(max)}$/2 t_{bit}; LIN Spec 2.1 (Par. 28)	P_5.6.30
AC Characteristics - Flash Mode							
Propagation delay bus dominant to RxD LOW	$t_{d(L),R}$	0.1	0.5	6	µs	–	P_5.6.31

Table 39 Electrical Characteristics (cont'd)

V_S = 5.5 V to 27 V, T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Output Slew Rate (falling) with Slew Rate Control	$SR_{fall\_w\_SR}$	-10	–	-1	V/µs	90% to 10% of V_S V_S = 9 to 18V R_L =300Ω[1)]	P_5.11.9
Output Slew Rate (rising) without Slew Rate Control	SR_{raise_w/o_SR}	25	–	60	V/µs	10% to 90% of V_S V_S = 9 to 18V R_L =300Ω[1)]	P_5.11.10
Output Slew Rate (falling) without Slew Rate Control	SR_{fall_w/o_SR}	–30	–	-10	V/µs	90% to 10% of V_S V_S = 9 to 18V R_L =300Ω[1)]	P_5.11.11
Turn ON Delay time	$t_{IN\text{-}HS}$	–	–	3	µs	ON = 1 to 10% of V_S R_L =300Ω	P_5.11.12
Turn ON time	t_{ON}	1	–	15	µs	V_S =13.5V HS_ON=1 to 90% of V_S R_L =300Ω T_j =25°C	P_5.11.13
Turn OFF time	t_{OFF}	1	–	15	µs	V_S =13.5V HS_ON= 0 to 10% of V_S R_L =300Ω; T_j =25°C	P_5.11.14
Load current limitation	Ishort	-1.2	–	–	A	[1)] VS =27V, VHS=0V, max duration 200 µs	P_5.11.15
Over-current detection							
Overcurrent threshold 0	I_{octh0}	4	–	18	mA	[1)] HSx_OC_SEL =00	P_5.11.16
Overcurrent threshold 0 hysteresis	$I_{octh0,hyst}$	2	–	5	mA	[1)] HSx_OC_SEL =00	P_5.11.17
Overcurrent threshold 1	I_{octh1}	50	–	75	mA	HSx_OC_SEL =01	P_5.11.18
Overcurrent threshold 1 hysteresis	$I_{octh1,hyst}$	5	–	15	mA	[1)] HSx_OC_SEL =01	P_5.11.19
Overcurrent threshold 2	I_{octh2}	100	–	150	mA	HSx_OC_SEL =10	P_5.11.20
Overcurrent threshold 2 hysteresis	$I_{octh2,hyst}$	10	–	30	mA	[1)] HSx_OC_SEL =10	P_5.11.21
Overcurrent threshold 3	I_{octh3}	150	–	220	mA	HSx_OC_SEL =11	P_5.11.22
Overcurrent threshold 3 hysteresis	$I_{octh3,hyst}$	20	–	50	mA	[1)] HSx_OC_SEL =11	P_5.11.23
Overall over-current filter time	t_{ocft}	8	–	80	µs	[1)] VS =13.5V, R_L =100Ω, HS_ON to OC_SD (including switch-on time)	P_5.11.24
ON-state open load detection							
Open load threshold	I_{OLONth}	4	–	18	mA	[1)] OL_EN = 1; HS_ON = 1	P_5.11.25

Table 39 Electrical Characteristics (cont'd)

V_S = 5.5 V to 27 V, T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Hysteresis	$I_{OLONhys}$	1	–	4	mA	[1] OL_EN = 1; HS_ON = 1	P_5.11.26
Off-state open load detection							
Open load voltage threshold	V_{OLth1}	0.5* V_S	0.67 *V_S	0.85* V_S	V	I_{OL_test}; open load activated; OLTH_SEL = 1	P_5.11.27
Hysteresis	V_{OLhys}	0.1* V_S	–	0.3* V_S	V	IOL_SEL = 1	P_5.11.28
Open load output current	I_{OL_test}	-150	–	-25	µA	IOL_SEL = 0	P_5.11.29
Open load output current	I_{OL_test}	-1.5	–	-0.5	mA	IOL_SEL = 1	P_5.11.30
Cyclic sense mode							
ON-State Resistance	$R_{ON,static}$	–	–	40	Ω	Definition: differential resistance or resistance at 40 mA	P_5.11.31
Output Slew Rate (rising)	SR_{rise} [1]	1	–	–	V/µs	10% to 90% of V_S V_S = 9 to 18V R_L =300Ω [1]	P_5.11.32
Output Slew Rate (falling)	SR_{fall} [1]	–	–	-1	V/µs	90% to 10% of V_S V_S = 9 to 18V R_L =300Ω	P_5.11.33
Delay Time CYCLIC_ON-HS	t_{IN-CYC}	–	–	2	µs	ON =1 to 10% of V_S RL=300Ω	P_5.11.34
Turn-ON time	t_{ON}	–	–	15	µs	V_S =13.5V ON=1 to 90% R_L =300Ω	P_5.11.35
Turn-OFF time	t_{OFF}	–	–	15	µs	V_S =13.5V ON=0 to 10% of V_S R_L =300Ω; T_j=25°C	P_5.11.36

1) Not subject to production test, specified by design.

w w w . i n f i n e o n . c o m

Published by Infineon Technologies AG

Doc_Number