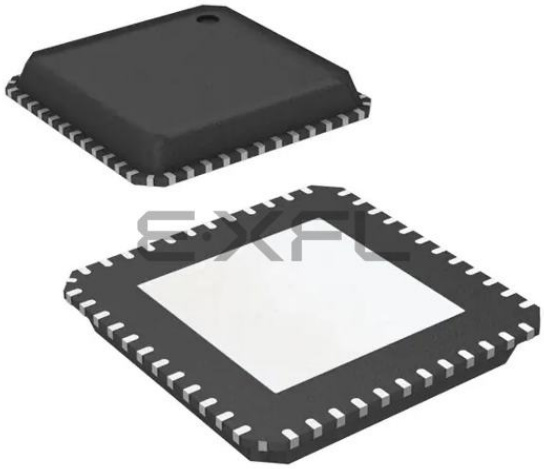

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Details	
Product Status	Obsolete
Applications	Automotive
Core Processor	XC800
Program Memory Type	FLASH (48kB)
Controller Series	-
RAM Size	3.25K x 8
Interface	LIN, SSI, UART
Number of I/O	11
Voltage - Supply	3V ~ 27V
Operating Temperature	-40°C ~ 150°C (TJ)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	PG-VQFN-48-29
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/tle9833qxxuma2

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2 General Device Information

2.1 Pin Configuration

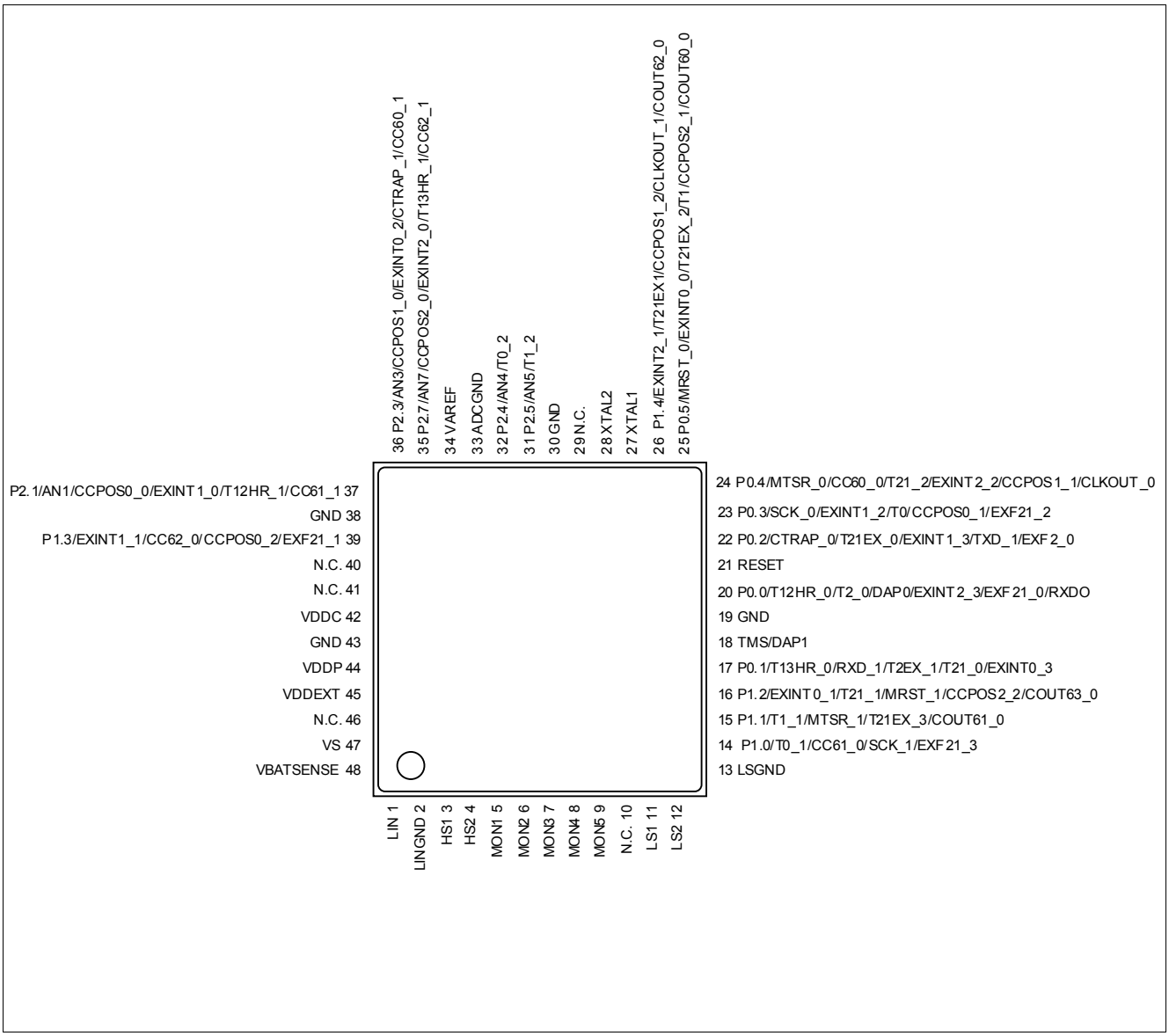


Figure 1 TLE9833QX pin configuration, VQFN-48-29 package (top view)

Table 3 Pin Definitions and Functions (cont'd)

Symbol	Pin Number	Type	Reset State	Function
Others				
VAREF	34	I/O	O	5V ADC1 reference voltage
XTAL1	27	I	I	External oscillator input
XTAL2	28	O	Hi-Z	External oscillator output
TMS	18	I	I/PD	TMS test mode select input DAP1 Debug Access Port 1
RESET	21	I/O	I/O/PU	Reset input, not available during Sleep Mode
VBAT_SENSE	48	I	I	Battery supply voltage sense input
N.C.	10, 29, 40, 41, 46	–	–	Not connected - can be connected to GND

3.1.2 Voltage Regulator 1.5V (VDDC)

This module represents the 1.5 V voltage regulator, which serves as core supply for the 8-bit µC and other chip internal analog 1.5 V functions (e.g. 8 Bit ADC). To further reduce the current consumption of the 8-bit MCU during Stop Mode the output voltage is optionally reduced to 0.9 V.

Features

- 1.5 V low-drop voltage regulator
- Optional 0.9 V in Stop Mode
- Current limitation
- Overcurrent monitoring and shutdown with MCU signalling (interrupt)
- Overvoltage monitoring with MCU signalling (interrupt)
- Undervoltage monitoring with MCU signalling (interrupt)
- Pull-down current source at the output for Sleep Mode (100 µA)

The output capacitor C_{VDDC} is mandatory to ensure a proper regulator functionality.

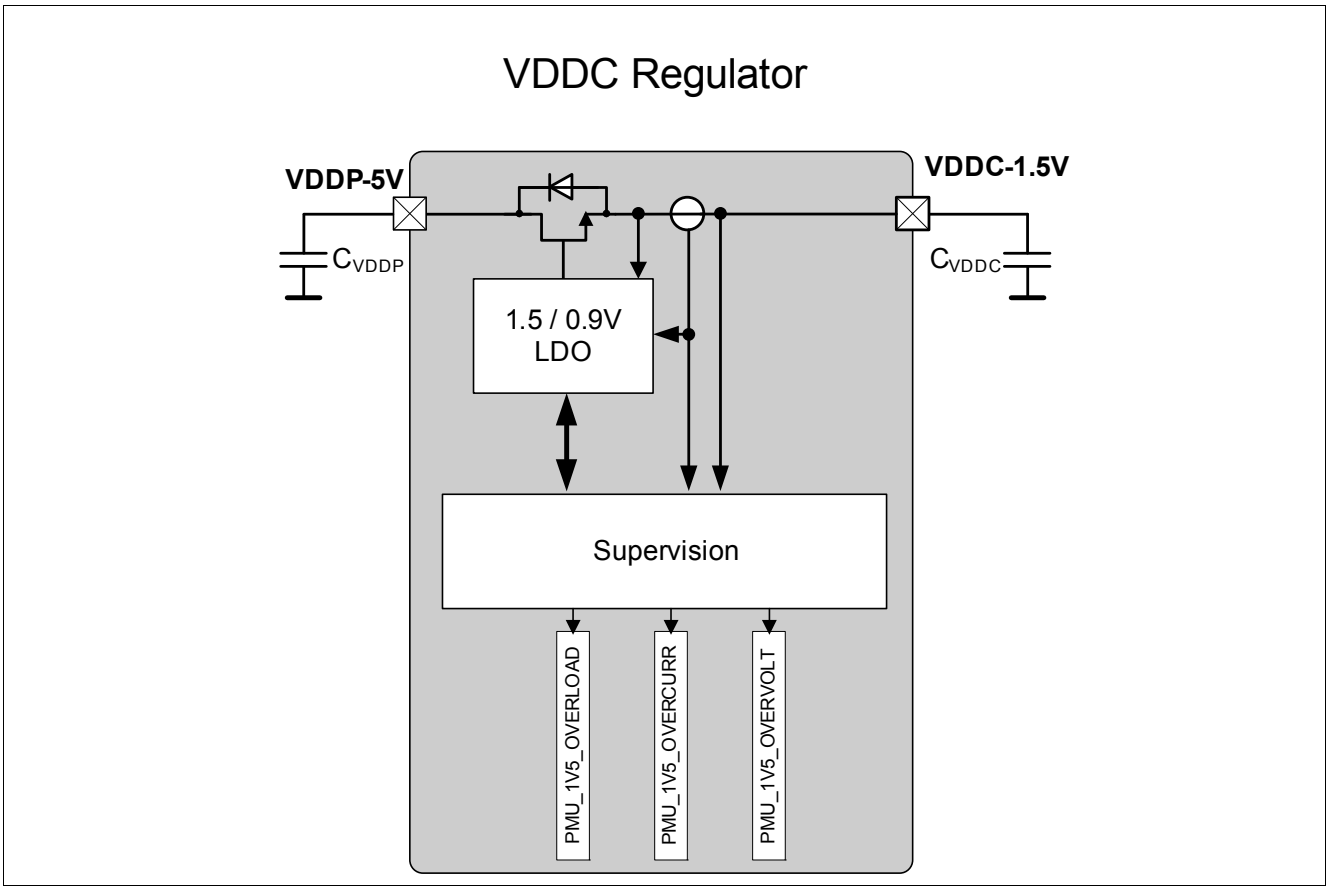


Figure 7 Module Block Diagram of VDDC Voltage Regulator

Figure 10 shows the functional blocks of the XC800 Core. The XC800 Core consists mainly of the instruction decoder, the arithmetic section, the program control section, the access control section, and the interrupt controller.

The instruction decoder decodes each instruction and accordingly generates the internal signals required to control the functions of the individual units within the core. These internal signals have an effect on the source and destination of data transfers and control the ALU processing.

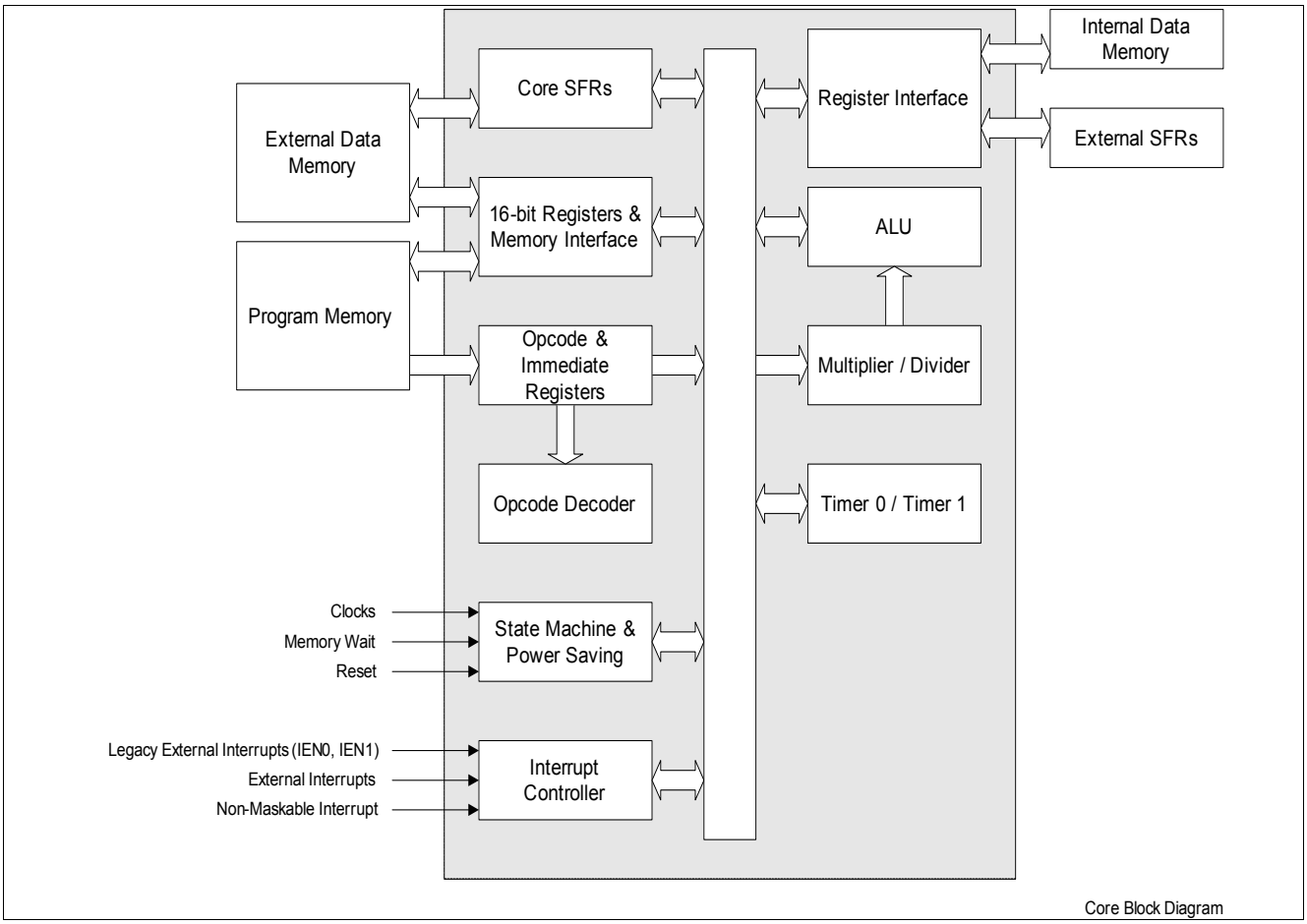


Figure 10 XC800 Core Block Diagram

The arithmetic section of the processor performs extensive data manipulation and consists of the arithmetic/logic unit (ALU), A register, B register and PSW register. The ALU accepts 8-Bit data words from one or two sources and generates an 8-Bit result under the control of the instruction decoder. The ALU performs both arithmetic and logic operations. Arithmetic operations include add, subtract, multiply, divide, increment, decrement, BCD-decimal-add-adjust and compare. Logic operations include AND, OR, Exclusive OR, complement and rotate (right, left or swap nibble (left four)). Also included is a Boolean unit performing the Bit operations as set, clear, complement, jump-if-set, jump-if-not-set, jump-if-set-and-clear and move to/from carry. The ALU can perform the Bit operations of logical AND or logical OR between any addressable Bit (or its complement) and the carry flag, and place the new result in the carry flag.

The program control section controls the sequence in which the instructions stored in program memory are executed. The 16-Bit program counter (PC) holds the address of the next instruction to be executed. The conditional branch logic enables internal and external events to the processor to cause a change in the program execution sequence.

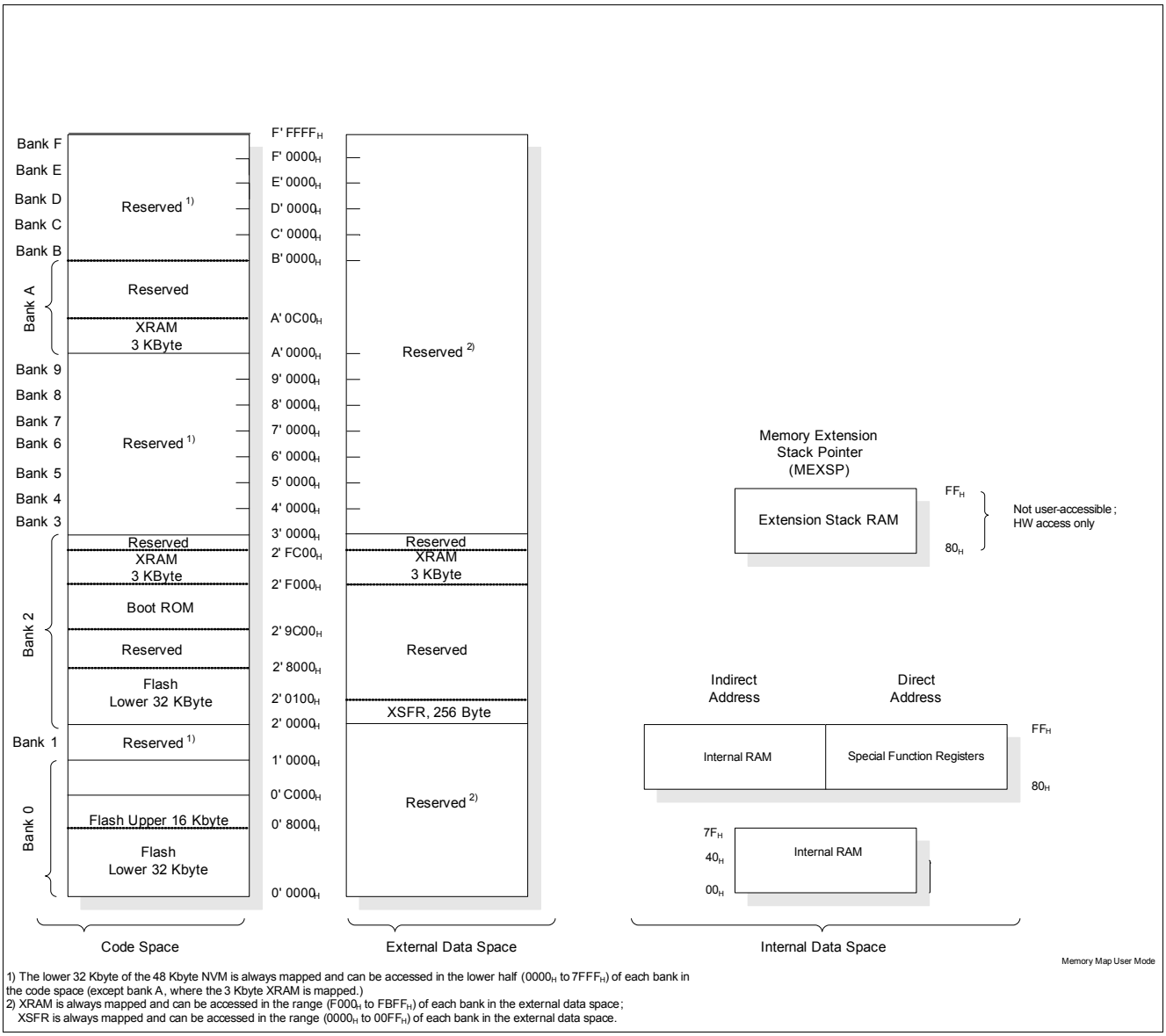
The access control unit is responsible for the selection of the on-chip memory resources. The interrupt requests from the peripheral units are handled by the interrupt controller unit.

3.4 Memory Architecture

The TLE9833QX CPU manipulates operands in the following memory spaces:

- 48 kByte of Flash memory in code space
- BootROM memory in code space
- 256 Byte of internal RAM data memory in internal data space
- 3 kByte of XRAM memory in code space and external data space (XRAM can be read/written as program memory or external data memory)
- 128 Byte of special function registers SFR in internal data space
- 256 Byte of special function registers XSFR in external data space.

Figure 11 illustrates the memory address spaces of the TLE9833QX.



1) The lower 32 Kbyte of the 48 Kbyte NVM is always mapped and can be accessed in the lower half (0000_H to $7FFF_H$) of each bank in the code space (except bank A, where the 3 Kbyte XRAM is mapped.)
2) XRAM is always mapped and can be accessed in the range ($F000_H$ to $FBFF_H$) of each bank in the external data space;
XSFR is always mapped and can be accessed in the range (0000_H to $00FF_H$) of each bank in the external data space.

Figure 11 TLE9833QX Memory Map

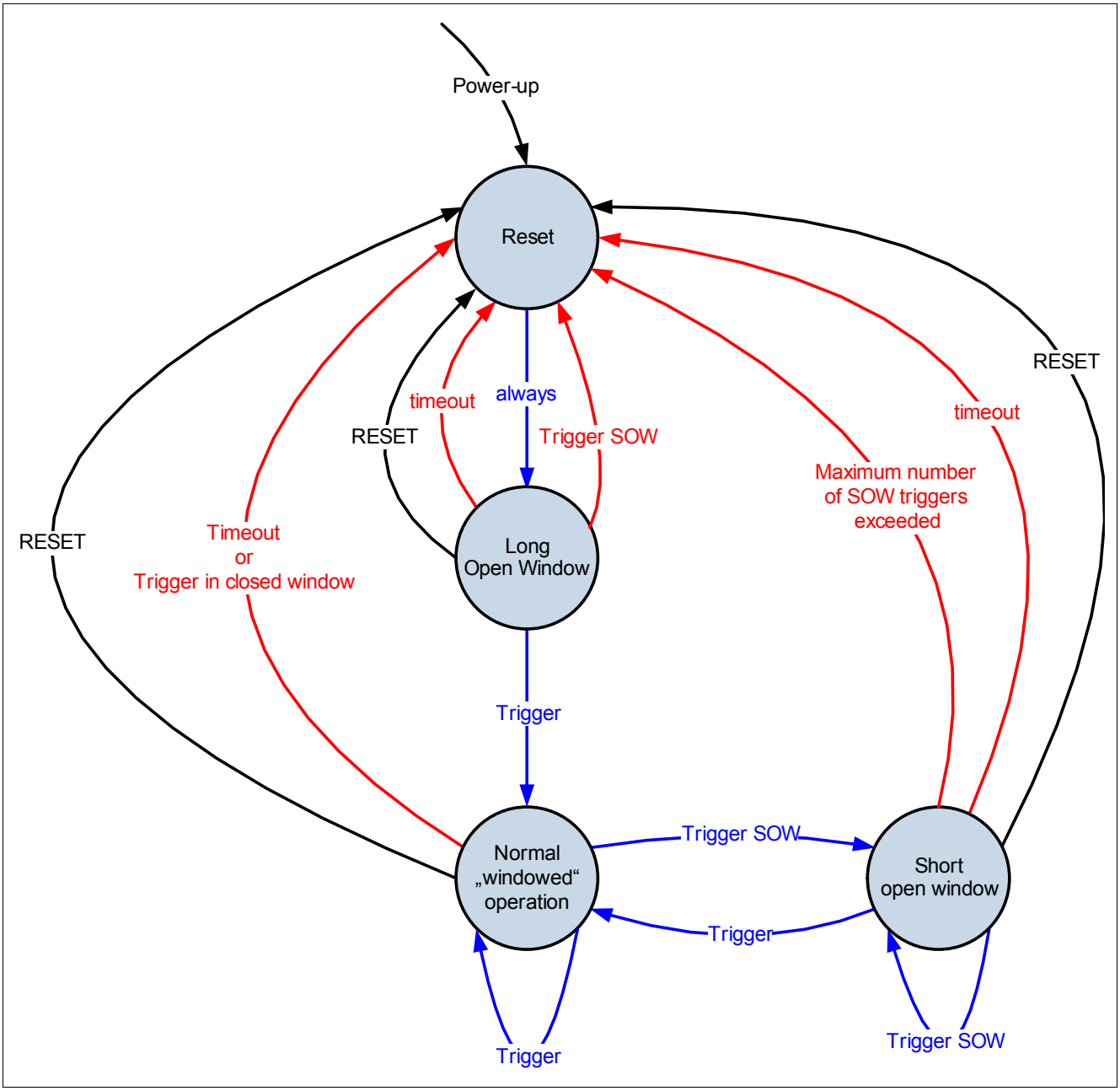


Figure 12 Watchdog Timer 1 Behavior

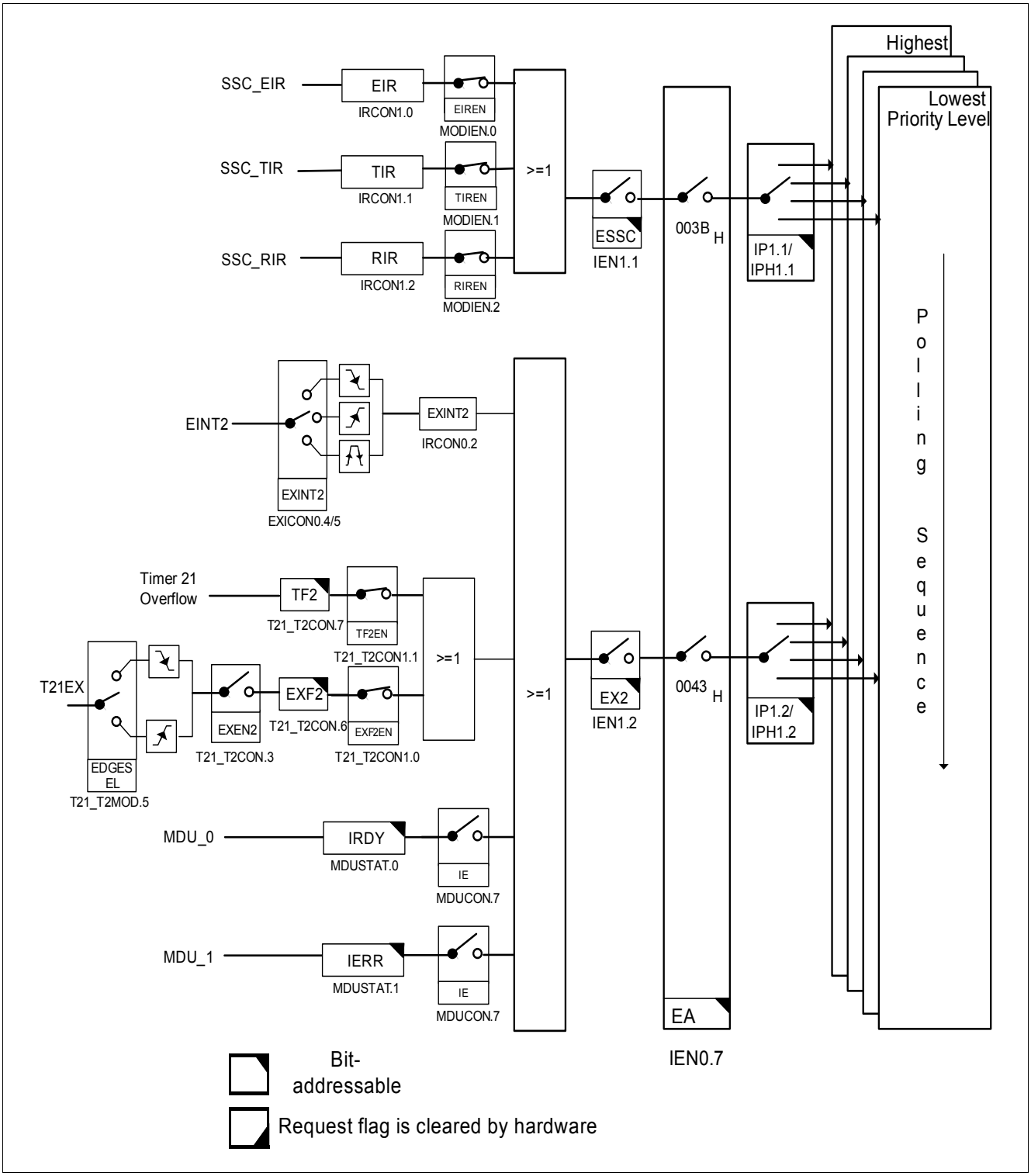


Figure 16 Interrupt Request Sources (Part 3)

3.15 UART

The UART provides a full-duplex asynchronous receiver/transmitter, i.e. it can transmit and receive simultaneously. It is also receive-buffered, i.e. it can commence reception of a second Byte before a previously received Byte has been read from the receive register. However, if the first Byte still has not been read by the time reception of the second Byte is complete, one of the Bytes will be lost. The serial port receive and transmit registers are both accessed at Special Function Register (SFR) SBUF. Writing to SBUF loads the transmit register, and reading SBUF accesses a physically separate receive register.

UART Features

- Full-duplex asynchronous modes
  - 8-Bit or 9-Bit data frames, LSB first
  - fixed or variable baud rate
- Receive buffered
- Multiprocessor communication
- Interrupt generation on the completion of a data transmission or reception
- Baud-rate generator with fractional divider for generating a wide range of baud rates
- Hardware logic for break and synch Byte detection

UART Modes

The UART can be used in four different modes. In mode 0, it operates as an 8-Bit shift register. In mode 1, it operates as an 8-Bit serial port. In modes 2 and 3, it operates as a 9-Bit serial port. The only difference between mode 2 and mode 3 is the baud rate, which is fixed in mode 2 but variable in mode 3. The variable baud rate is set by the underflow rate on the dedicated baud-rate generator.

The different modes are selected by setting Bits SM0 and SM1 to their corresponding values, as shown in **Table 9**.

Table 9 UART Modes

SM0	SM1	Operating Mode	Baud Rate
0	0	Mode 0: 8-Bit shift register	$f_{PCLK}/2$
0	1	Mode 1: 8-Bit shift UART	Variable
1	0	Mode 2: 9-Bit shift UART	$f_{PCLK}/64$
1	1	Mode 3: 9-Bit shift UART	Variable

4 Application Information

4.1 Electric Drive Application

Figure 31 shows the TLE9833QX in an electric drive application setup controlling a DC-brush motor. The two Low Side Switches are controlling a relay each. An external FET allows to control the window lift motor with a PWM signal as generated with the CCU6 module of the microcontroller.

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

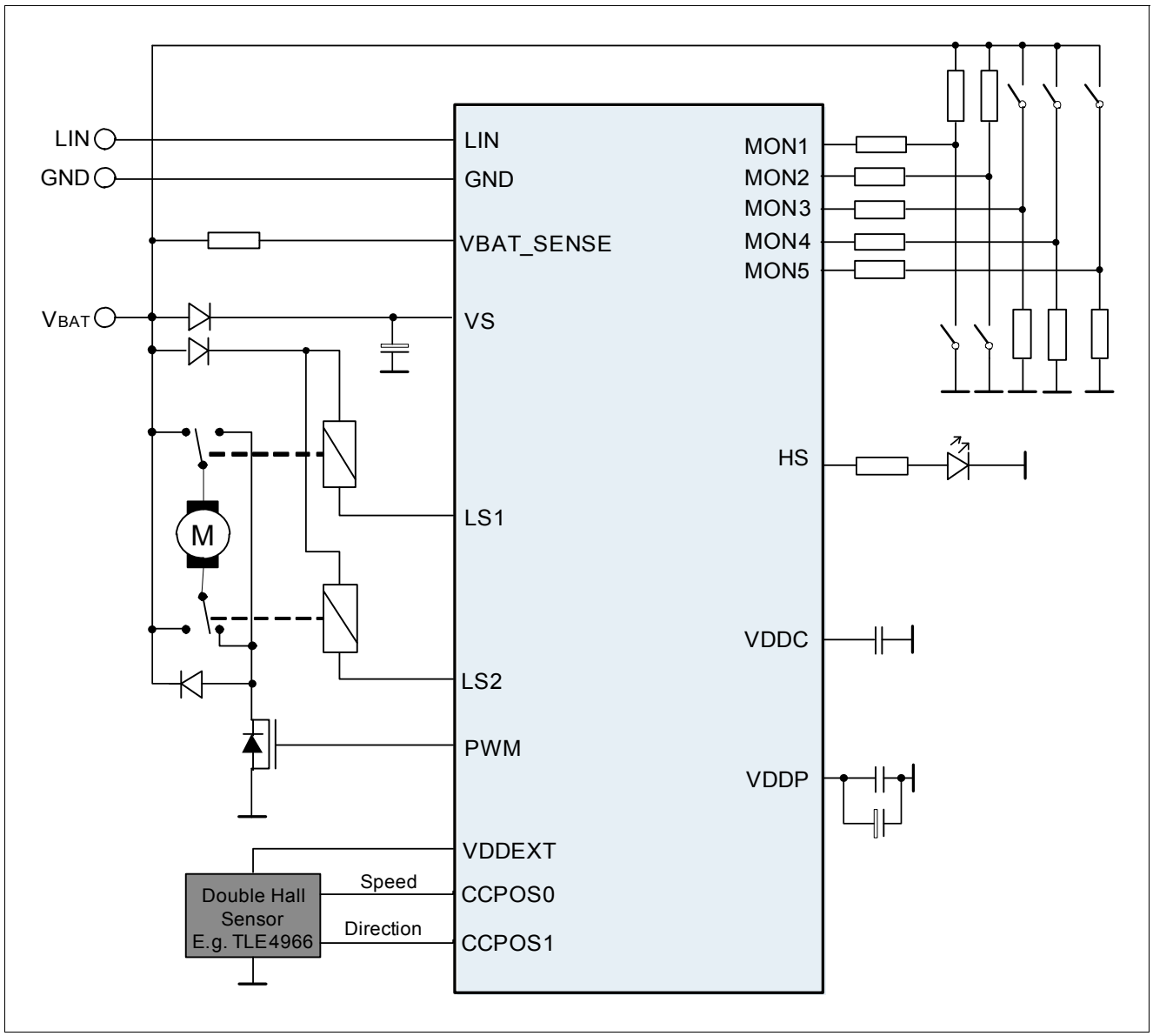


Figure 31 Simplified Application Diagram

4.2 Connection of N.C. Pins

It is recommended to connect N.C. pins to GND unless otherwise specified. Since pins 10 and 46 are located next to high voltage pins (VS, MON5, LS1) these 2 N.C. pins can be also left unconnected in order to avoid huge current flow and damage of the system in case of short-circuit.

4.3 Connection of ADCGND Pin

The ADCGND pin is chip-internal connected to reference ground. In order to provide full offset compensation and achieve full accuracy of ADC1 the ADCGND pin must not be connected to board ground. ADCGND pin should be connected with a capacitor (100 nF) to VAREF only.

4.4 Connection of Exposed Pad

It is recommended to connect the exposed pad to GND.

4.5 Voltage Regulators-Blocking Capacitors

Table 11 External Component Recommendation

Symbol	Function	Comment
C_{VS}	blocking capacitor at VS pin	> 20 µF Elco + 100 nF Ceramic, ESR < 1 Ω
C_{VDDP}	blocking capacitor at VDDP pin	1 µF typ. + 100 nF Ceramic, ESR < 1 Ω
C_{VDDEXT}	blocking capacitor at VDDEXT pin	100 nF typ., ESR < 1 Ω
C_{VDDC}	blocking capacitor at VDDC pin	> 330 nF + 100 nF Ceramic, ESR < 1 Ω
C_{VAREF}	blocking capacitor at VAREF pin	> 100 nF, ESR < 1 Ω

4.6 Additional External Components

Table 12 External Component Recommendation

Symbol	Function	Comment
C_{HSx}	HF blocking capacitor at HSx pin	6.8 nF
R_{MONx}	resistor at MONx pin	1 kΩ
$R_{VBAT\_}$	resistor at VBAT_SENSE pin	1 kΩ

5.5 Parallel Ports (GPIO)

5.5.1 Functional Range

Table 25 Functional Range

V_S = 5.5 V to 27 V, T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Output current on any pin	I_{OH} , I_{OL}	–	–	20	mA	1) 2)	P_5.5.1
Max output current for all GPIOs	I_{max}	–	–	60	mA	1) 2)	P_5.5.2

1) One of these limits must be kept.

2) Not subject to production test, specified by design

5.5.2 DC Parameters

These parameters apply to the IO voltage range, 4.5 V ≤ V_{DDP} ≤ 5.5 V.

Note: Operating Conditions apply.

Keeping signal levels within the limits specified in this table ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the overload current I_{OV}.

Table 26 DC Characteristics

V_S = 5.5 V to 27 V, T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input low voltage (all except XTAL1)	V_{IL}	-0.3	–	0.3 x V_{DDP}	V	–	P_5.5.3
Input high voltage (all except XTAL1)	V_{IH}	0.7 x V_{DDP}	–	V_{DDP} + 0.3	V	–	P_5.5.4
Input Hysteresis[1)]	HYS	0.11 x V_{DDP}	–	–	V	Series resistance = 0 Ω	P_5.5.5
Output low voltage	V_{OL}	–	–	1.0	V	2) $I_{OL} \le I_{OLmax}$	P_5.5.6
Output low voltage	V_{OL}	–	–	0.4	V	2) $I_{OL} \le$ 3) I_{OLnom}	P_5.5.7
Output high voltage[4)]	V_{OH}	V_{DDP} - 1.0	–	–	V	2) $I_{OH} \ge I_{OHmax}$	P_5.5.8
Output high voltage	V_{OH}	V_{DDP} - 0.4	–	–	V	2)3) $I_{OH} \ge I_{OHnom}$	P_5.5.9
Input leakage current (Port 2)	I_{OZ1}	-400	–	+400	nA	$T_J \le 85°C$, 0 V < V_{IN} < V_{DDP}	P_5.5.10
Input leakage current (all other)[5)]	I_{OZ2}	-5	–	+5	µA	$T_J \le 85°C$, 0.45 V < V_{IN} < V_{DDP}	P_5.5.11

Table 26 DC Characteristics

V_S = 5.5 V to 27 V, T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input leakage current (all other)	I_{OZ2}	-15	–	+15	µA	T_J ≤ 150°C, 0.45 V < V_{IN} < V_{DDP}	P_5.5.12
Pull level keep current	I_{PLK}	-240	–	+240	µA	6) V_{PIN} ≥ V_{IH} (up) V_{PIN} ≤ V_{IL} (dn)	P_5.5.13
Pull level force current	I_{PLF}	-1.5	–	+1.5	mA	6) V_{PIN} ≤ V_{IL} (up) V_{PIN} ≥ V_{IH} (dn)	P_5.5.14
Pin capacitance (digital inputs/outputs)	C_{IO}	–	–	10	pF	–	P_5.5.15

1) Not subject to production test, specified by design.

2) The maximum deliverable output current of a port driver depends on the selected output driver mode. The limit for pin groups must be respected.

3) As a rule, with decreasing output current the output levels approach the respective supply level (V_{OL}→GND, V_{OH}→V_{DDP}). However, only the levels for nominal output currents are verified.

4) This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage is determined by the external circuit.

5) The given values are worst-case values. In production test, this leakage current is only tested at 125°C; other values are ensured by correlation. For derating, please refer to the following descriptions:
Leakage derating depending on temperature (T_J = junction temperature [°C]):
I_{OZ} = 0.05 × $e^{(1.5 + 0.028 \times TJ)}$ [µA]. For example, at a temperature of 95°C the resulting leakage current is 3.2 µA.
Leakage derating depending on voltage level (ΔV = V_{DDP} - V_{PIN} [V]):
I_{OZ} = $I_{OZtempmax}$ - (1.6 × ΔV) [µA]
This voltage derating formula is an approximation which applies for maximum temperature.

6) Keep current: Limit the current through this pin to the indicated value so that the enabled pull device can keep the default pin level: V_{PIN} ≥ V_{IH} for a pull-up; V_{PIN} ≤ V_{IL} for a pull-down.
Force current: Drive the indicated minimum current through this pin to change the default pin level driven by the enabled pull device: V_{PIN} ≤ V_{IL} for a pull-up; V_{PIN}≥ V_{IH} for a pull-down.
These values apply to the fixed pull-devices in dedicated pins and to the user-selectable pull-devices in general purpose IO pins.

5.6 LIN Transceiver

5.6.1 Electrical Characteristics

Table 28 Electrical Characteristics LIN Transceiver

V_s = 5.5V - 18V, T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Bus Receiver Interface							
Receiver threshold voltage, recessive to dominant edge	V_{th_dom}	0.4 × V_S	0.45 × V_S	0.53 x V_S	V	SAE J2602	P_5.6.1
Receiver dominant state	V_{BUSdom}	-27	–	0.4 × V_S	V	LIN Spec 2.1 (Par. 17)	P_5.6.2
Receiver threshold voltage, dominant to recessive edge	V_{th_rec}	0.47 x V_S	0.55 × V_S	0.6 × V_S	V	SAE J2602	P_5.6.3
Receiver recessive state	V_{BUSrec}	0.6 × V_S	–	1.15 × V_S	V	[1] LIN Spec 2.1 (Par. 18)	P_5.6.4
Receiver center voltage	V_{BUS_CNT}	0.475 × V_S	0.5 × V_S	0.525 × V_S	V	[2] LIN Spec 2.1 (Par. 19)	P_5.6.5
Receiver hysteresis	V_{HYS}	0.07 V_S	0.12 × V_S	0.175 × V_S	V	[3] LIN Spec 2.1 (Par. 20)	P_5.6.6
Wake-up threshold voltage	$V_{BUS,wk}$	0.4 × V_S	0.5 × V_S	0.6 × V_S	V	–	P_5.6.7
Dominant time for bus wake-up	$t_{WK,bus}$	3	–	15	µs	To achieve the required wake-up time from 30 µs to 150 µs according to LIN spec., an additional digital filter is added (see PMU chapter)	P_5.6.8
Bus Transmitter Interface							
Bus recessive output voltage	$V_{BUS,ro}$	0.8 × V_S	–	V_S	V	V_{TxD} = high Level	P_5.6.9
Bus short circuit current	$I_{BUS,sc}$	40	100	150	mA	V_{BUS} = 13.5 V	P_5.6.10
Leakage current	$I_{BUS\_NO\_GND}$	-1000	-70	–	µA	V_S = 0 V; V_{BUS} = -12 V; LIN Spec 2.1 (Par. 15)	P_5.6.11
Leakage current	$I_{BUS\_NO\_BAT}$	–	10	20	µA	V_S = 0 V; V_{BUS} = 18 V; LIN Spec 2.1 (Par. 16)	P_5.6.12
Leakage current	$I_{BUS\_PAS\_dom}$	-1	–	–	mA	V_S = 18 V; V_{BUS} = 0 V; LIN Spec 2.1 (Par. 13)	P_5.6.13
Leakage current	$I_{BUS\_PAS\_rec}$	–	–	20	µA	V_S = 8 V; V_{BUS} = 18 V; LIN Spec 2.1 (Par. 14)	P_5.6.14
Bus pull-up resistance	R_{BUS}	20	30	47	kΩ	Normal mode LIN Spec 2.1 (Param. 26)	P_5.6.15
LIN input capacity	C_{LIN_IN}	–	15	30	pF	[4]	P_5.6.80

5.7 High-Speed Synchronous Serial Interface

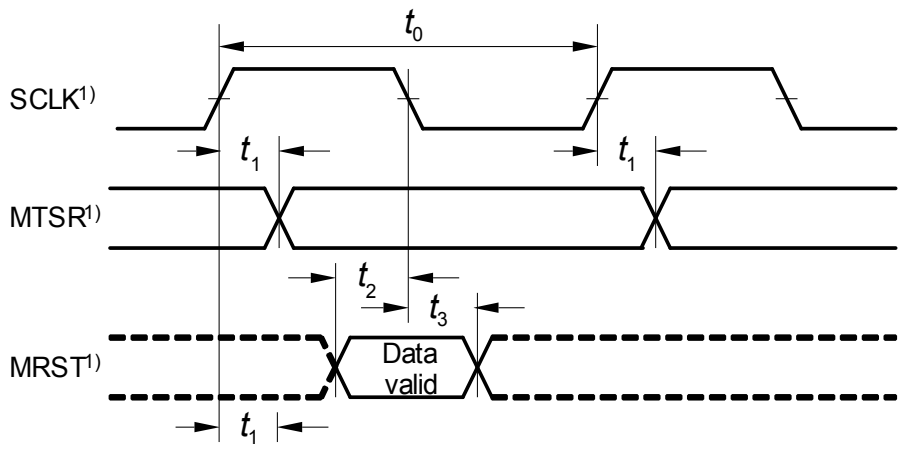
The table below provides the SSC timing in the TLE9833QX.

Table 29 SSC Master Mode Timing (Operating Conditions apply; CL = 50 pF)

V_S = 5.5 V to 27 V, T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
SCLK clock period	t_0	1) 2 * T_{SSC}	–	–		–	P_5.7.1
MTSR delay from SCLK	t_1	10	–	–	ns	–	P_5.7.2
MRST setup to SCLK	t_2	10	–	–	ns	–	P_5.7.3
MRST hold from SCLK	t_3	15	–	–	ns	–	P_5.7.4

1) $T_{SSCmin} = T_{CPU} = 1/f_{CPU}$. When f_{CPU} = 24 MHz, t_0 = 83.3 ns. T_{CPU} is the CPU clock period.



1) This timing is based on the following setup: CON.PH = CON.PO = 0.

SSC_Tmg1

Figure 32 SSC Master Mode Timing

Table 31 Supply voltage signal conditioning

V_S = 5.5 V to 27 V, T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
V_{DD5_SENSE}	ΔV_{DDP_SENSE}	-150	–	150	mV	–	P_5.8.15
V_{DD1V5_SENSE}	ΔV_{DDC_SENSE}	-45	–	45	mV	–	P_5.8.16

1) This parameter is not subject to production test

2) The device is calibrated based on an external 1kΩ resistor

5.8.3 Measurement Functions Monitoring Input Voltage Attenuator

Table 32 Monitoring input voltage attenuation

V_S = 5.5 V to 27 V, T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Power Supply							
Input resistance[1)]	R_{IN}	300	400	500	kΩ	PD_N=1 (on-state) V_{MON_X}=0 to 18V if VMON_SEN_SEL_INRANGE = 0	P_5.8.17
Input resistance	R_{IN}	250	–	–	kΩ	V_{MON_X} =0 to 28V if VMON_SEN_SEL_INRANGE = 1 >200 kΩ under all other conditions	P_5.8.18
Timing Characteristics							
Analog Multiplexer Settling Time	$T_{MUXsettle}$	–	–	30	µs	This time frame is valid from writing the corresponding selection register to proper settling of the voltage at channel 7 of the 10-Bit ADC	P_5.8.19
Overall (calibrated) measurement accuracy after A/D-conversion							
V_{MONx} 10-bit ADC	$\Delta V_{MONxADC10B}$	-200	–	200	mV	V_s=5.5V to 18V, T_j = 40..85°C	P_5.8.20

1) Not subject to production test, specified by design.

5.10 High-Voltage Monitor Input

Table 37 Electrical Characteristics

V_S = 5.5 V to 27 V, T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input Pin characteristics							
Wake-up/monitoring threshold voltage	V_{MONth}	0.4*V_s	0.5*V_s	0.6*V_s	V	without external serial resistor R_s (with R_s: $\Delta V = I_{PD/PU} * R_s$);	P_5.10.1
Threshold hysteresis	$V_{MONth,hys}$	0.02*V_s	0.06*V_s	0.12*V_s	V	in all modes; without external serial resistor R_s (with R_s: $\Delta V = I_{PD/PU} * R_s$);	P_5.10.2
Pull-up current MONx_CTRL_STS.MONx_PU = high MONx_CTRL_STS.MONx_PD = low	$I_{PU, MONx}$	-20	-10	-1	µA	0 V < V_{MON_IN} < V_s - 2 V	P_5.10.3
Pull-up current MONx_CTRL_STS.MONx_PU = high MONx_CTRL_STS.MONx_PD = high	$I_{PU, MONx}$	-20	-10	-1	µA	0.6*V_s < V_{MON_IN} < V_s - 2 V	P_5.10.4
Pull-down current MONx_CTRL_STS.MONx_PU = low MONx_CTRL_STS.MONx_PD = high	$I_{PD, MONx}$	4	10	18	µA	2 V < V_{MON_IN} < V_s	P_5.10.5
Pull-down current MONx_CTRL_STS.MONx_PU = high MONx_CTRL_STS.MONx_PD = high	$I_{PD, MONx}$	4	10	18	µA	2 V < V_{MON_IN} < 0.4*V_s	P_5.10.6
Input leakage current MONx_CTRL_STS.MONx_PU = low MONx_CTRL_STS.MONx_PD = low	$I_{LK,I}$	-2	–	2	µA	0 V < V_{MON_IN} < 28 V	P_5.10.7

The Parameters of the analog measurement are listed in the chapter Measurement Interface.

6 Package Outlines

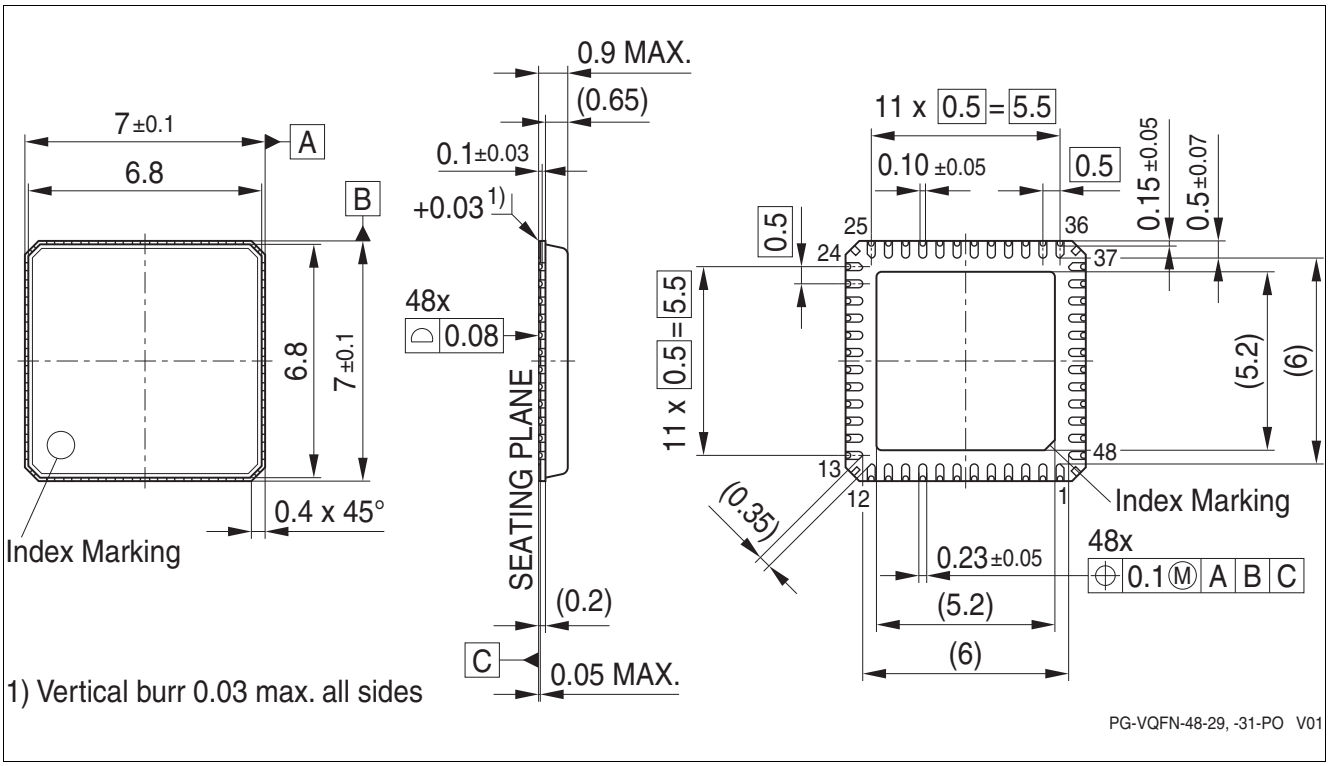


Figure 33 Package outline VQFN-48-29

Notes

1. *You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/products**.*
2. *Dimensions in mm.*

7 Revision History

Revision	Date	Changes
1.1	2012-03-08	Editorial Changes
1.1	2012-03-08	Added full package name (VQFN-48-29)
1.1	2012-03-08	**Table 4**: VDD1V5P: Power Mode configurations: added comment: "Power Down Supply"
1.1	2012-03-08	**Table 5**: Description of PMU Submodules: PMU-CYCMU description added and PMU-CMU changed from “cyclic” to “clock” management
1.1	2012-03-08	**Table 30**: Changed Value Max. from parameter “Common input voltage in differential mode” from V_{DD} to V_{DDP}
1.1	2012-03-08	**Table 23**: Changed Value Min. from parameter “Input voltage (amplitude) on XTAL1” from $0.3xV_{DDI}$ to $0.3xV_{DDP}$
1.1	2012-03-08	**Table 41**: for “Turn ON..., Turn OFF...” Parameters changed Test condition from R_L =1kΩ to R_L =270Ω
1.1	2012-03-08	**Table 14**: - Removed “max” from the symbol suffixes - Corrected Symbol of Parameter “Input voltage at LIN” from V_{MONx} to V_{LIN}
1.1	2012-03-08	**Table 41**: Parameter “Overcurrent Limitation”: - Renamed Parameter from “Typical on-state current” to “Overcurrent Limitation”. - Added min. (175mA) and max (325mA) values - Removed Parameter “Overcurrent threshold accuracy”. This information is added in the “Note/Test” Condition of the Parameter ”Overcurrent Limitation”
1.1	2012-03-08	**Table 19**: - Renamed Parameter “Output Current” to “Specified Output Current” - Renamed Parameter “Output Capacitance” to “Required Output Capacitance”
1.1	2012-03-08	**Table 20**: - Renamed Parameter “Output Current” to “Specified Output Current” - Renamed Parameter “Output Capacitance” to “Required Output Capacitance” - Parameter “Dynamic Line Regulation”: Correct typo in “Note/Test Condition” from V_{DDC} to V_{DDP} - Parameter “Output Voltage including line regulation @ Stop Mode”: Value Max. changed from 1.01 to 1.15
1.1	2012-03-08	**Figure 31**: Application Diagram updated
1.1	2012-03-08	**Figure 29**: Module Block Diagram updated (replaced 500mA by 250mA)
1.1	2012-03-08	**Table 27**: Changed “Maximum Output Current” to “Nominal Output Current” in third row
1.1	2012-03-08	**Table 14**: Added “Output voltage VDDP” for t < 100ms, in Stop Mode only
1.1	2012-03-08	**Chapter 4.1**: Added disclaimer note
1.1	2012-03-08	**Table 11**: Changed value C_{VDDEXT} of blocking capacitor at VDDEXT pin to100nF (from 10nF)
1.1	2012-03-08	**Table 11** and **Table 12**: Changed headline from “External Component Requirements” to “External Component Recommendation”