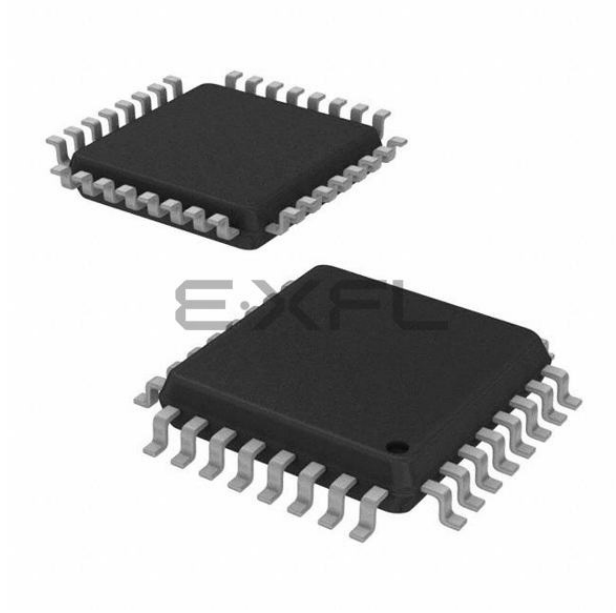

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST7
Core Size	8-Bit
Speed	8MHz
Connectivity	SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384 x 8
Voltage - Supply (Vcc/Vdd)	3.8V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st72f324bk2t3

2 Pin description

Figure 2. 44-pin LQFP package pinout

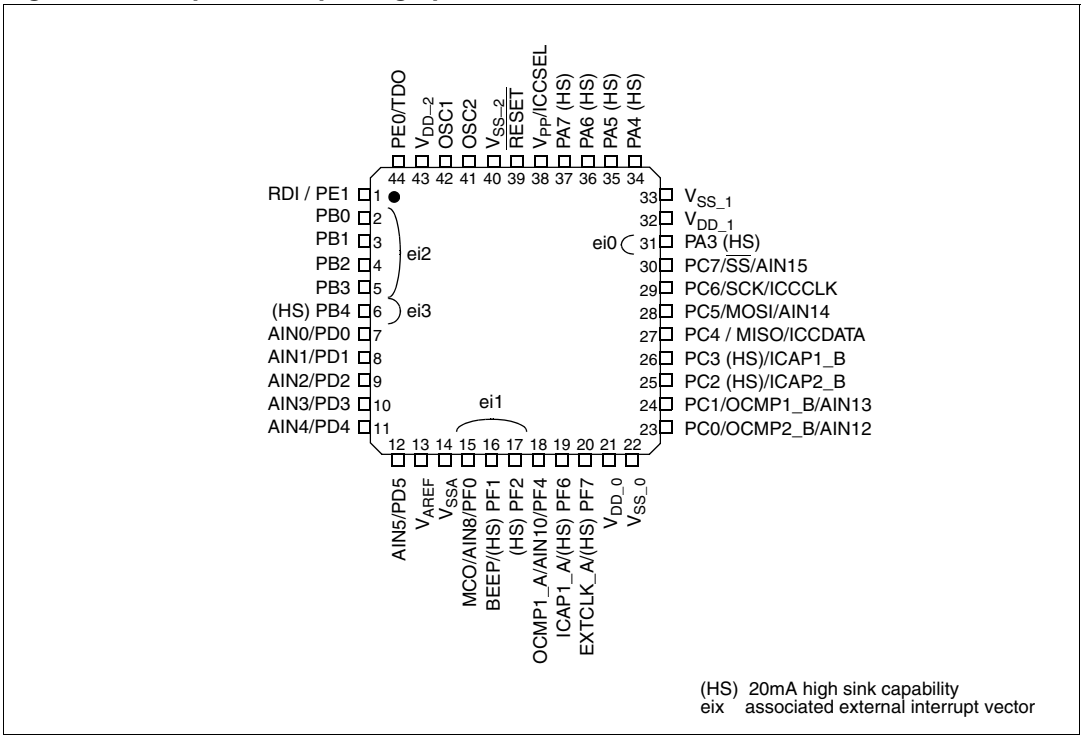
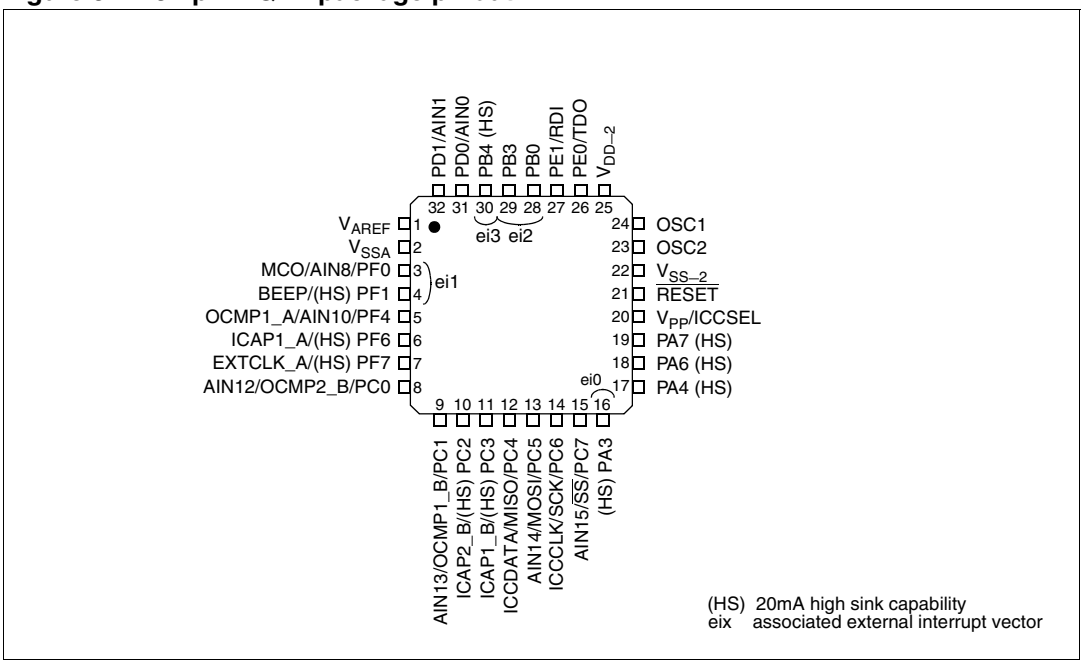


Figure 3. 32-pin LQFP package pinout



See *Section 12: Electrical characteristics on page 145* for external pin connection guidelines.

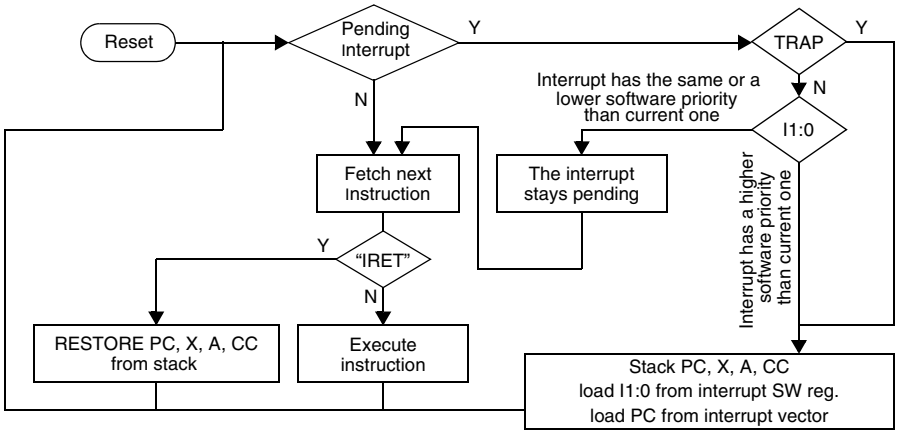
Table 2. Device pin description (continued)

Pin			Type	Level		Port						Main function (after reset)	Alternate function	
No.		Name				Input				Output				
LQFP44	LQFP32			Input	Output	float	wpu	int	ana	OD	PP			
26	11	PC3 (HS)/ICAP1_B	I/O	C_T	HS	**X**	X			X	X	Port C3	Timer B input capture 1	
27	12	PC4/MISO/ICCDATA	I/O	C_T		**X**	X			X	X	Port C4	SPI master in/slave out data	ICC data input
28	13	PC5/MOSI /AIN14	I/O	C_T		**X**	X		X	X	X	Port C5	SPI master out/slave in data	ADC analog input 14
29	14	PC6/SCK /ICCCLK	I/O	C_T		**X**	X			X	X	Port C6	SPI serial clock	ICC clock output
30	15	PC7/$\overline{SS}$/AIN15	I/O	C_T		**X**	X		X	X	X	Port C7	SPI slave select (active low)	ADC analog input 15
31	16	PA3 (HS)	I/O	C_T	HS	**X**		ei0		X	X	Port A3		
32	-	V_{DD_1}(1)	S									Digital main supply voltage		
33	-	V_{SS_1}(1)	S									Digital ground voltage		
34	17	PA4 (HS)	I/O	C_T	HS	**X**	X			X	X	Port A4		
35	-	PA5 (HS)	I/O	C_T	HS	**X**	X			X	X	Port A5		
36	18	PA6 (HS)	I/O	C_T	HS	**X**				T		Port A6(2)		
37	19	PA7 (HS)	I/O	C_T	HS	**X**				T		Port A7(2)		
38	20	V_{PP} /ICCSEL	I									Must be tied low. In the Flash programming mode, this pin acts as the programming voltage input V_{PP}. See *Section 12.10.2* for more details. High voltage must not be applied to ROM devices.		
39	21	$\overline{RESET}$	I/O	C_T								Top priority non-maskable interrupt		
40	22	V_{SS_2}(1)	S									Digital ground voltage		
41	23	OSC2(3)	O									Resonator oscillator inverter output		
42	24	OSC1(3)	I									External clock input or resonator oscillator inverter input		
43	25	V_{DD_2}(1)	S									Digital main supply voltage		
44	26	PE0/TDO	I/O	C_T		**X**	X			X	X	Port E0	SCI transmit data out	
1	27	PE1/RDI	I/O	C_T		**X**	X			X	X	Port E1	SCI receive data in	

Table 14. Interrupt software priority levels

Interrupt software priority	Level	I1	I0
Level 0 (main)	Low	1	0
Level 1	↓	0	1
Level 2	↓	0	0
Level 3 (= interrupt disable)	High	1	1

Figure 16. Interrupt processing flowchart



7.2.1 Servicing pending interrupts

As several interrupts can be pending at the same time, the interrupt to be taken into account is determined by the following two-step process:

- the highest software priority interrupt is serviced,
- if several interrupts have the same software priority then the interrupt with the highest hardware priority is serviced first.

Figure 17 describes this decision process.

Figure 17. Priority decision process flowchart

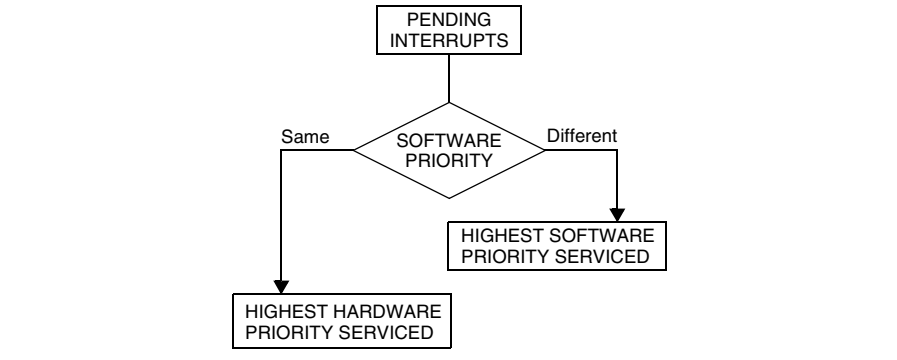
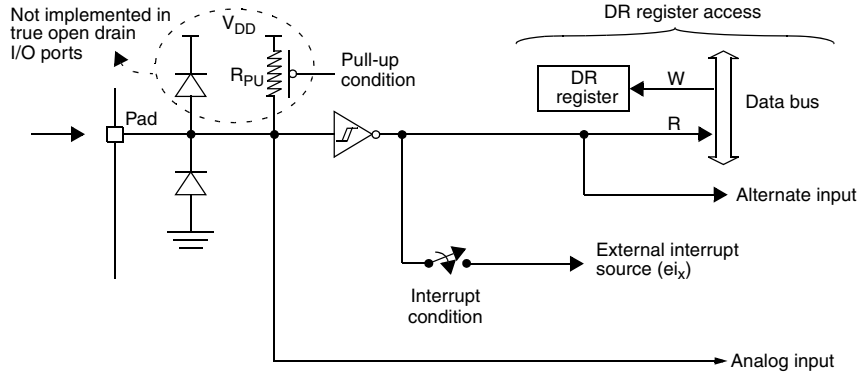
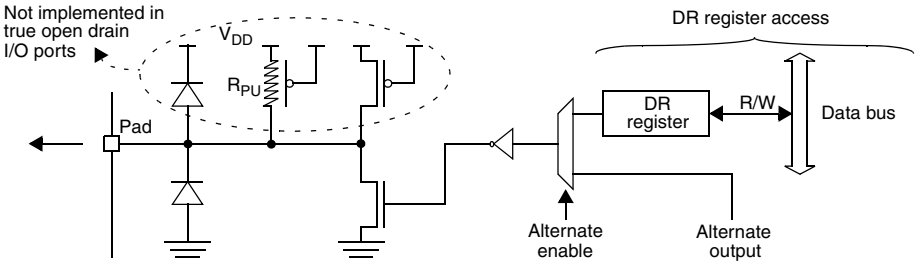
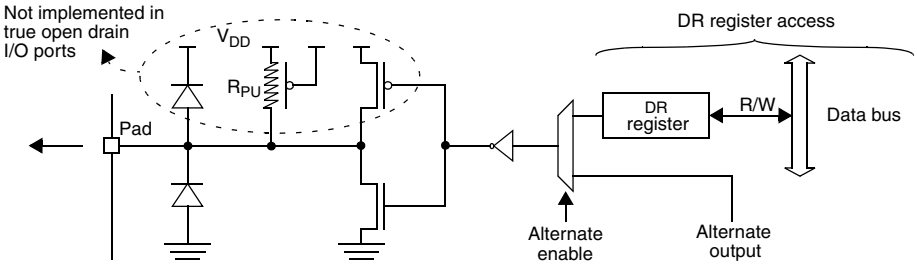


Table 29. I/O port configurations

	Hardware configuration
Input(1)	
Open-drain output(2)	
PUSH-pull output(2)	

1. When the I/O port is in input configuration and the associated alternate function is enabled as an output, reading the DR register will read the alternate function output status.
2. When the I/O port is in output configuration and the associated alternate function is enabled as an input, the alternate function reads the pin status given by the DR register content.

Caution: The alternate function must not be activated as long as the pin is configured as input with interrupt, in order to avoid generating spurious interrupts.

External clock

The external clock (where available) is selected if CC0 = 1 and CC1 = 1 in the CR2 register.

The status of the EXEDG bit in the CR2 register determines the type of level transition on the external clock pin EXTCLK that will trigger the free running counter.

The counter is synchronized with the falling edge of the internal CPU clock.

A minimum of four falling edges of the CPU clock must occur between two consecutive active edges of the external clock; thus the external clock frequency must be less than a quarter of the CPU clock frequency.

Figure 36. Counter timing diagram, internal clock divided by 2

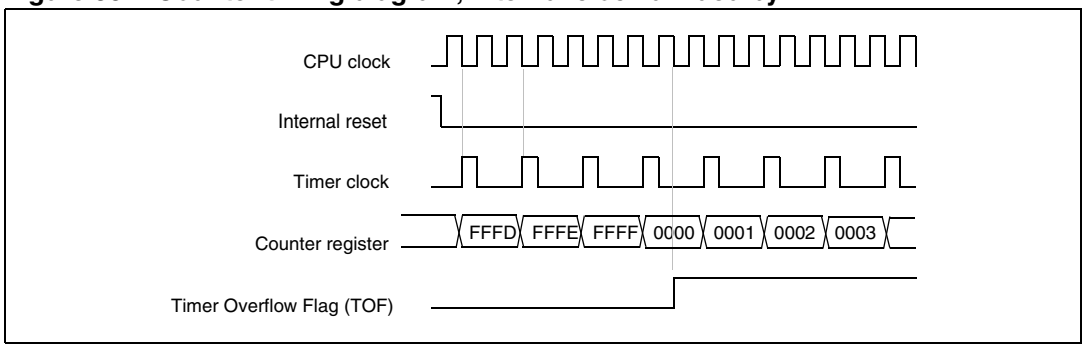


Figure 37. Counter timing diagram, internal clock divided by 4

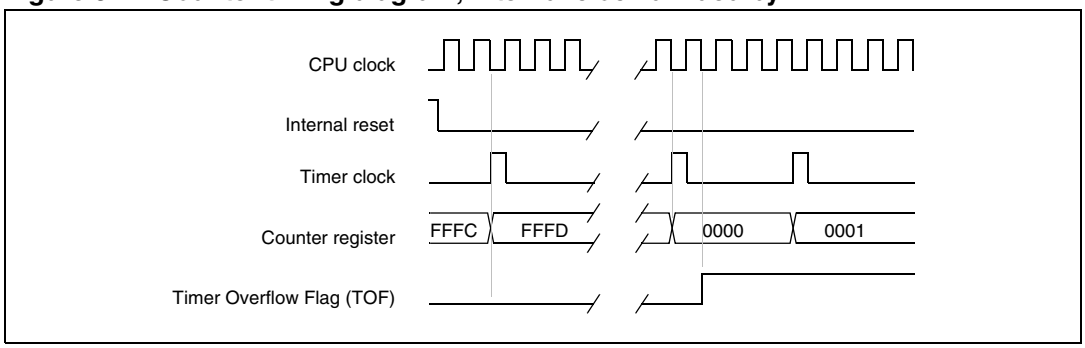
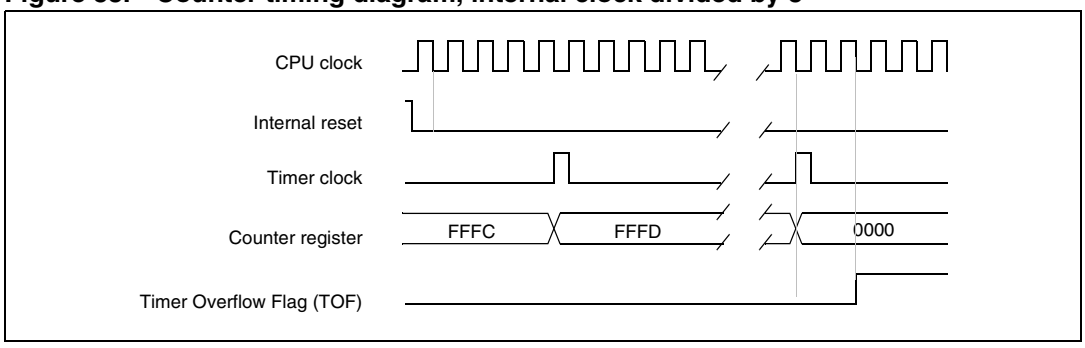


Figure 38. Counter timing diagram, internal clock divided by 8



Note: The MCU is in reset state when the internal reset signal is high, when it is low the MCU is running.

Input capture

In this section, the index, *i*, may be 1 or 2 because there are two input capture functions in the 16-bit timer.

The two 16-bit input capture registers (IC1R/IC2R) are used to latch the value of the free running counter after a transition is detected on the ICAP*i* pin (see *Figure 40*).

Table 44. Input capture byte distribution

Register	MS byte	LS byte
ICiR	IC*i*HR	IC*i*LR

The ICiR registers are read-only registers.

The active transition is software programmable through the IEDG*i* bit of Control Registers (CR*i*).

Timing resolution is one count of the free running counter: (f_{CPU}/CC[1:0]).

Procedure

To use the input capture function select the following in the CR2 register:

- Select the timer clock (CC[1:0]) (see *Table 50*).
- Select the edge of the active transition on the ICAP2 pin with the IEDG2 bit (the ICAP2 pin must be configured as floating input or input with pull-up without interrupt if this configuration is available).

Select the following in the CR1 register:

- Set the ICIE bit to generate an interrupt after an input capture coming from either the ICAP1 pin or the ICAP2 pin
- Select the edge of the active transition on the ICAP1 pin with the IEDG1 bit (the ICAP1pin must be configured as floating input or input with pull-up without interrupt if this configuration is available).

When an input capture occurs:

- ICF*i* bit is set.
- The IC*i*R register contains the value of the free running counter on the active transition on the ICAP*i* pin (see *Figure 40*).
- A timer interrupt is generated if the ICIE bit is set and the I bit is cleared in the CC register. Otherwise, the interrupt remains pending until both conditions become true.

Clearing the Input Capture interrupt request (that is, clearing the ICF*i* bit) is done in two steps:

1. Reading the SR register while the ICF*i* bit is set
2. An access (read or write) to the IC*i*LR register

Control/Status Register (CSR)

CSR Reset value: xxxx x0xx (xxh)

7	6	5	4	3	2	1	0
ICF1	OCF1	TOF	ICF2	OCF2	TIMD	Reserved	
RO	RO	RO	RO	RO	R/W	-	

Table 51. CSR register description

Bit	Name	Function
7	ICF1	Input Capture Flag 1 0: No Input Capture (reset value). 1: An Input Capture has occurred on the ICAP1 pin or the counter has reached the OC2R value in PWM mode. To clear this bit, first read the SR register, then read or write the low byte of the IC1R (IC1LR) register.
6	OCF1	Output Compare Flag 1 0: No match (reset value). 1: The content of the free running counter has matched the content of the OC1R register. To clear this bit, first read the SR register, then read or write the low byte of the OC1R (OC1LR) register.
5	TOF	Timer Overflow Flag 0: No timer overflow (reset value). 1: The free running counter rolled over from FFFFh to 0000h. To clear this bit, first read the SR register, then read or write the low byte of the CR (CLR) register. *Note: Reading or writing the ACLR register does not clear TOF.*
4	ICF2	Input Capture Flag 2 0: No input capture (reset value). 1: An Input Capture has occurred on the ICAP2 pin. To clear this bit, first read the SR register, then read or write the low byte of the IC2R (IC2LR) register.
3	OCF2	Output Compare Flag 2 0: No match (reset value). 1: The content of the free running counter has matched the content of the OC2R register. To clear this bit, first read the SR register, then read or write the low byte of the OC2R (OC2LR) register.
2	TIMD	Timer Disable This bit is set and cleared by software. When set, it freezes the timer prescaler and counter and disabled the output functions (OCMP1 and OCMP2 pins) to reduce power consumption. Access to the timer registers is still available, allowing the timer configuration to be changed, or the counter reset, while it is disabled. 0: Timer enabled. 1: Timer prescaler, counter and outputs disabled.
1:0	-	Reserved, must be kept cleared.

10.4.6 Low power modes

Table 53. Effect of low power modes on SPI

Mode	Description
Wait	No effect on SPI. SPI interrupt events cause the device to exit from Wait mode.
Halt	SPI registers are frozen. In Halt mode, the SPI is inactive. SPI operation resumes when the MCU is woken up by an interrupt with Exit from Halt mode capability. The data received is subsequently read from the SPIDR register when the software is running (interrupt vector fetching). If several data are received before the wake-up event, then an overrun error is generated. This error can be detected after the fetch of the interrupt routine that woke up the device.

Using the SPI to wake up the MCU from Halt mode

In slave configuration, the SPI is able to wake up the ST7 device from Halt mode through a SPIF interrupt. The data received is subsequently read from the SPIDR register when the software is running (interrupt vector fetch). If multiple data transfers have been performed before software clears the SPIF bit, then the OVR bit is set by hardware.

Note: When waking up from Halt mode, if the SPI remains in Slave mode, it is recommended to perform an extra communications cycle to bring the SPI from Halt mode state to normal state. If the SPI exits from Slave mode, it returns to normal state immediately.

Caution: The SPI can wake up the ST7 from Halt mode only if the Slave Select signal (external $\overline{SS}$ pin or the SSI bit in the SPICSR register) is low when the ST7 enters Halt mode. Therefore, if Slave selection is configured as external (see *Slave Select management on page 99*), make sure the master drives a low level on the $\overline{SS}$ pin when the slave enters Halt mode.

10.4.7 Interrupts

Table 54. SPI interrupt control/wake-up capability(1)

Interrupt event	Event flag	Enable control bit	Exit from WAIT	Exit from HALT
SPI end of transfer event	SPIF	SPIE	Yes	Yes
Master mode fault event	MODF			No
Overrun error	OVR			

1. The SPI interrupt events are connected to the same interrupt vector (see *Section 7: Interrupts*). They generate an interrupt if the corresponding Enable Control Bit is set and the interrupt mask in the CC register is reset (RIM instruction).

Receiver muting and wake-up feature

In multiprocessor configurations it is often desirable that only the intended message recipient should actively receive the full message contents, thus reducing redundant SCI service overhead for all non-addressed receivers.

The non-addressed devices may be placed in sleep mode by means of the muting function.

Setting the RWU bit by software puts the SCI in sleep mode:

All the reception status bits cannot be set.

All the receive interrupts are inhibited.

A muted receiver may be awakened by one of the following two ways:

- by Idle Line detection if the Wake bit is reset,
- by Address Mark detection if the Wake bit is set.

A receiver wakes up by Idle Line detection when the Receive line has recognized an Idle Frame. Then the RWU bit is reset by hardware but the Idle bit is not set.

A receiver wakes up by Address Mark detection when it received a ‘1’ as the most significant bit of a word, thus indicating that the message is an address. The reception of this particular word wakes up the receiver, resets the RWU bit and sets the RDRF bit, which allows the receiver to receive this word normally and to use it as an address word.

Caution: In Mute mode, do not write to the SCICR2 register. If the SCI is in Mute mode during the read operation (RWU = 1) and an address mark wake-up event occurs (RWU is reset) before the write operation, the RWU bit will be set again by this write operation. Consequently the address byte is lost and the SCI is not woken up from Mute mode.

Parity control

Parity control (generation of parity bit in transmission and parity checking in reception) can be enabled by setting the PCE bit in the SCICR1 register. Depending on the frame length defined by the M bit, the possible SCI frame formats are as listed in *Table 59*.

Table 59. Frame formats(1)(2)

M bit	PCE bit	SCI frame
0	0	| SB | 8 bit data | STB |
0	1	| SB | 7-bit data | PB | STB |
1	0	| SB | 9-bit data | STB |
1	1	| SB | 8-bit data PB | STB |

1. SB = Start bit, STB = Stop bit, and PB = Parity bit.
2. In case of wake-up by an address mark, the MSB bit of the data is taken into account and not the Parity bit.

10.5.5 Low power modes

Table 60. Effect of low power modes on SCI

Mode	Description
Wait	No effect on SCI. SCI interrupts cause the device to exit from Wait mode.
Halt	SCI registers are frozen. In Halt mode, the SCI stops transmitting/receiving until Halt mode is exited.

10.5.6 Interrupts

The SCI interrupt events are connected to the same interrupt vector.

These events generate an interrupt if the corresponding Enable Control bit is set and the interrupt mask in the CC register is reset (RIM instruction).

Table 61. SCI interrupt control/wake-up capability

Interrupt event	Event flag	Enable control bit	Exit from WAIT	Exit from HALT
Transmit data register empty	TDRE	TIE	Yes	No
Transmission complete	TC	TCIE	Yes	No
Received data ready to be read	RDRF	RIE	Yes	No
Overrun error detected	OR		Yes	No
Idle line detected	IDLE	ILIE	Yes	No
Parity error	PE	PIE	Yes	No

10.5.7 SCI registers

SCI Status Register (SCISR)

SCISR Reset value: 1100 0000 (C0h)

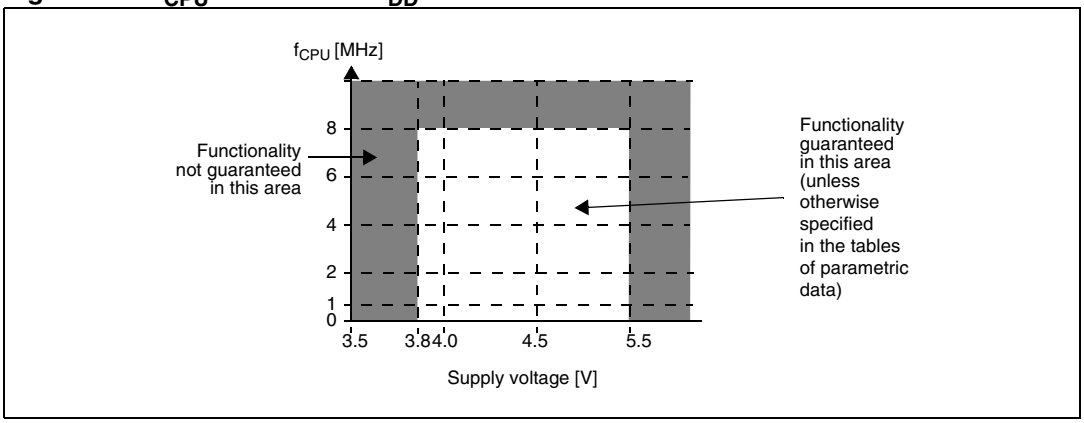
7	6	5	4	3	2	1	0
TDRE	TC	RDRF	IDLE	OR	NF	FE	PE
RO	RO	RO	RO	RO	RO	RO	RO

12.3 Operating conditions

Table 86. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CPU}	Internal clock frequency		0	8	MHz
V_{DD}	Operating voltage (except Flash Write/Erase)		3.8	5.5	V
	Operating Voltage for Flash Write/Erase	V_{PP} = 11.4 to 12.6V	4.5	5.5	
T_A	Ambient temperature range	A-suffix versions	-40	85	°C
		B-suffix versions		105	
		C-suffix version		125	
		D-suffix version		150	

Figure 62. f_{CPU} max versus V_{DD}



Note: Some temperature ranges are only available with a specific package and memory size. Refer to Section 14: Device configuration and ordering information.

Warning: Do not connect 12V to V_{PP} before V_{DD} is powered on, as this may damage the device.

12.5.3 Supply and clock managers

The previous current consumption specified for the ST7 functional operating modes over temperature range does not take into account the clock source current consumption. To obtain the total device consumption, the two current values must be added (except for Halt mode).

Table 91. Oscillators, PLL and LVD current consumption

Symbol	Parameter	Conditions	Typ	Max	Unit
$I_{DD(RCINT)}$	Supply current of internal RC oscillator		625		µA
$I_{DD(RES)}$	Supply current of resonator oscillator(1)(2)		see Section 12.6.3 on page 154		
$I_{DD(PLL)}$	PLL supply current	V_{DD} = 5V	360		
$I_{DD(LVD)}$	LVD supply current		150	300	

1. Data based on characterization results done with the external components specified in Section 12.6.3, not tested in production.
2. As the oscillator is based on a current source, the consumption does not depend on the voltage.

12.5.4 On-chip peripherals

Table 92. On-chip peripherals current consumption

Symbol	Parameter	Conditions	Typ	Unit
$I_{DD(TIM)}$	16-bit timer supply current(1)	T_A = 25°C, f_{CPU} = 4 MHz, V_{DD} = 5.0V	50	µA
$I_{DD(SPI)}$	SPI supply current(2)		400	
$I_{DD(SCI)}$	SCI supply current(3)			
$I_{DD(ADC)}$	ADC supply current when converting(4)			

1. Data based on a differential I_{DD} measurement between reset configuration (timer counter running at $f_{CPU}/4$) and timer counter stopped (only TIMD bit set). Data valid for one timer.
2. Data based on a differential I_{DD} measurement between reset configuration (SPI disabled) and a permanent SPI master communication at maximum speed (data sent equal to 55h). This measurement includes the pad toggling consumption.
3. Data based on a differential I_{DD} measurement between SCI low power state (SCID = 1) and a permanent SCI data transmit sequence.
4. Data based on a differential I_{DD} measurement between reset configuration and continuous A/D conversions.

2. Not tested in production.

12.8.3 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU and DLU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). Two models can be simulated for standard microcontrollers: Human Body Model and Charged Device Model. These tests conform to standards JESD22-A114 and JESD22-C101. There is an additional model for automotive microcontrollers: Machine Model, JESD22-A115.

Table 103. Absolute maximum ratings

Symbol	Ratings	Conditions	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25°C	2000	V
$V_{ESD(MM)}$	Electrostatic discharge voltage (machine model)		200	
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charged device model)		750	

1. Data based on characterization results, not tested in production.

Static and dynamic Latch-Up

- **LU**: 3 complementary static tests are required on 10 parts to assess the latch-up performance. A supply overvoltage (applied to each power supply pin) and a current injection (applied to each input, output and configurable I/O pin) are performed on each sample. This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.
- **DLU**: Electrostatic discharges (one positive then one negative test) are applied to each pin of three samples when the micro is running to assess the latch-up performance in dynamic mode. Power supplies are set to the typical values, the oscillator is connected as near as possible to the pins of the micro and the component is put in reset mode. This test conforms to the IEC1000-4-2 and SAEJ1752/3 standards. For more details, refer to the application note AN1181.

12.13.1 Analog power supply and reference pins

Depending on the MCU pin count, the package may feature separate V_{AREF} and V_{SSA} analog power supply pins. These pins supply power to the A/D converter cell and function as the high and low reference voltages for the conversion. In some packages, V_{AREF} and V_{SSA} pins are not available (refer to *Section 2 on page 15*). In this case the analog supply and reference pads are internally bonded to the V_{DD} and V_{SS} pins.

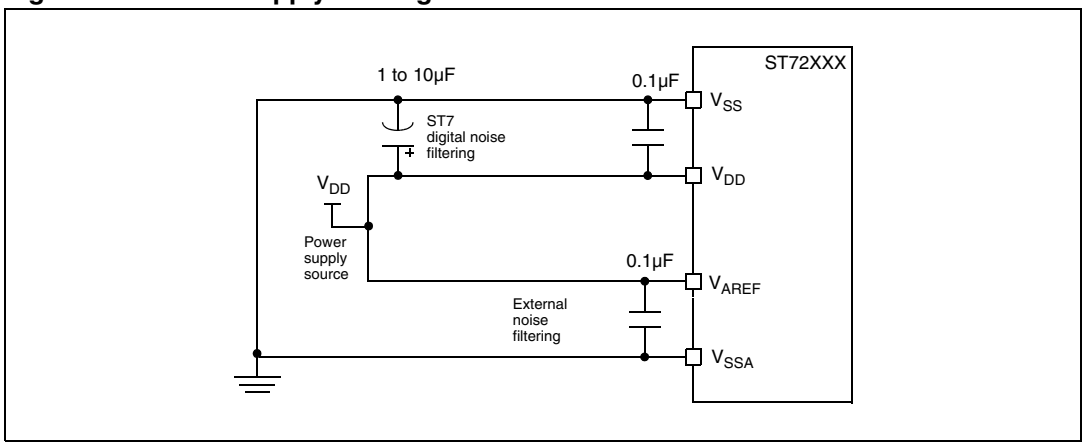
Separation of the digital and analog power pins allow board designers to improve A/D performance. Conversion accuracy can be impacted by voltage drops and noise in the event of heavily loaded or badly decoupled power supply lines (see *Section 12.13.2: General PCB design guidelines*).

12.13.2 General PCB design guidelines

To obtain best results, some general design and layout rules should be followed when designing the application PCB to shield the noise-sensitive, analog physical interface from noise-generating CMOS logic signals.

- Use separate digital and analog planes. The analog ground plane should be connected to the digital ground plane via a single point on the PCB.
- Filter power to the analog power planes. It is recommended to connect capacitors, with good high frequency characteristics, between the power and ground lines, placing 0.1µF and optionally, if needed 10pF capacitors as close as possible to the ST7 power supply pins and a 1 to 10µF capacitor close to the power source (see *Figure 85*).
- The analog and digital power supplies should be connected in a star network. Do not use a resistor, as V_{AREF} is used as a reference voltage by the A/D converter and any resistance would cause a voltage drop and a loss of accuracy.
- Properly place components and route the signal traces on the PCB to shield the analog inputs. Analog signals paths should run over the analog ground plane and be as short as possible. Isolate analog signals from digital signals that may switch while the analog inputs are being sampled by the A/D converter. Do not toggle digital outputs on the same I/O port as the A/D input being converted.

Figure 85. Power supply filtering



13.3 Thermal characteristics

Table 115. Thermal characteristics

Symbol	Ratings	Value	Unit
R_{thJA}	Package thermal resistance (junction to ambient): LQFP44 10x10 LQFP32 7x7	 52 70	°C/W
P_D	Power dissipation(1)	500	mW
T_{Jmax}	Maximum junction temperature(2)	150	°C

1. The maximum power dissipation is obtained from the formula $P_D = (T_J - T_A) / R_{thJA}$. The power dissipation of an application can be defined by the user with the formula: $P_D = P_{INT} + P_{PORT}$ where P_{INT} is the chip internal power (I_{DD} x V_{DD}) and P_{PORT} is the port power dissipation depending on the ports used in the application.
2. The maximum chip-junction temperature is based on technology characteristics.

13.4 Ecopack information

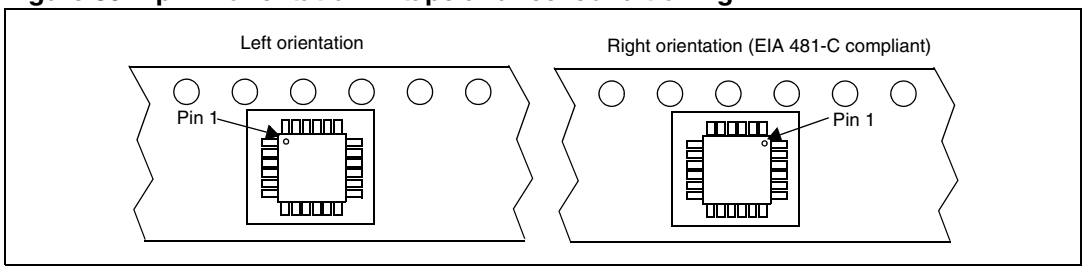
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

13.5 Packaging for automatic handling

The devices can be supplied in trays or with tape and reel conditioning.

Tape and reel conditioning can be ordered with pin 1 left-oriented or right-oriented when facing the tape sprocket holes as shown in *Figure 89*.

Figure 89. pin 1 orientation in tape and reel conditioning



See also *Figure 90: ST72F324Bxx-Auto Flash commercial product structure on page 182* and *Figure 91: ST72P324Bxx-Auto FastROM commercial product structure on page 184*.

14.2 ROM device ordering information and transfer of customer code

Customer code is made up of the ROM/FASTROM contents and the list of the selected options (if any). The ROM/FASTROM contents are to be sent with the S19 hexadecimal file generated by the development tool. All unused bytes must be set to FFh. Complete the appended ST72324B-Auto Microcontroller FASTROM/ROM Option List on page 185 to communicate the selected options to STMicroelectronics.

Refer to application note AN1635 for information on the counter listing returned by ST after code has been transferred.

The following *Figure 91: ST72P324Bxx-Auto FastROM commercial product structure* and *Figure 92: ST72324Bxx-Auto ROM commercial product structure* serve as guides for ordering. The STMicroelectronics Sales Organization will be pleased to provide detailed information on contractual points.

Caution: The readout protection binary value is inverted between ROM and Flash products. The option byte checksum differs between ROM and Flash.

ST72324B-Auto Microcontroller FASTROM/ROM Option List

(Last update: July 2007)

Customer: . . . . . .
Address: . . . . . .
. . . . . .
Contact: . . . . . .
Phone No: . . . . . .
Reference: . . . . . .

The FASTROM/ROM code name is assigned by STMicroelectronics.
FASTROM/ROM code must be sent in .S19 format. .Hex extension cannot be processed.

Device Type/Memory Size/Package (check only one option):

FASTROM DEVICE:	32K	16K	8K
LQFP44 10x10:	[ ] ST72P324B(J6)T	[ ] ST72P324B(J4)T	[ ] ST72P324B(J2)T
LQFP32 7x17:	[ ] ST72P324B(K6)T	[ ] ST72P324B(K4)T	[ ] ST72P324B(K2)T

ROM DEVICE:	32K	16K	8K
LQFP44 10x10:	[ ] ST72324B(J6)T	[ ] ST72324B(J4)T	[ ] ST72324B(J2)T
LQFP32 7x7:	[ ] ST72324B(K6)T	[ ] ST72324B(K4)T	[ ] ST72324B(K2)T

Conditioning for LQFP package (check only one option):

[ ] Tape and Reel [ ] Tray

Temperature range :
[ ] A (-40°C to +85°C)
[ ] B (-40°C to +105°C)
[ ] C (-40°C to +125°C)
[ ] D (-40°C to +150°C)

Special Marking: [ ] No [ ] Yes "_ _ _ _ _ _ _ _ _ _"
LQFP32: 7 characters max. Other packages: 10 characters max.
Authorized characters are letters, digits, '.', '-', '/' and spaces only.

Clock Source Selection: [ ] Resonator:
[ ] LP: Low power resonator (1 to 2 MHz)
[ ] MP: Medium power resonator (2 to 4 MHz)
[ ] MS: Medium speed resonator (4 to 8 MHz)
[ ] HS: High speed resonator (8 to 16 MHz)
[ ] Internal RC
[ ] External clock (sets MP medium power resonator in option byte)

PLL (1)(2) [ ] Disabled [ ] Enabled

LVD reset [ ] Disabled [ ] High threshold
[ ] Medium threshold [ ] Low threshold

Reset delay [ ] 256 cycles [ ] 4096 cycles

Watchdog selection [ ] Software activation [ ] Hardware activation

Halt when Watchdog on [ ] Reset [ ] No reset

Readout protection [ ] Disabled [ ] Enabled

Date . . . . . Signature . . . . . .

1. PLL must be disabled if internal RC network is selected.
2. The PLL can be enabled only if the resonator is configured to “Medium power: 2~4 MHz”.

CAUTION: The readout protection binary value is inverted between ROM and Flash products. The option byte checksum will differ between ROM and Flash.

Table 123. Document revision history (continued)

Date	Revision	Changes
12-Jul-2010	4	Added *Section 13.5 on page 178* Updated *Figure 90: ST72F324Bxx-Auto Flash commercial product structure on page 182*, *Figure 91: ST72P324Bxx-Auto FastROM commercial product structure on page 184* and *Figure 92: ST72324Bxx-Auto ROM commercial product structure on page 185*