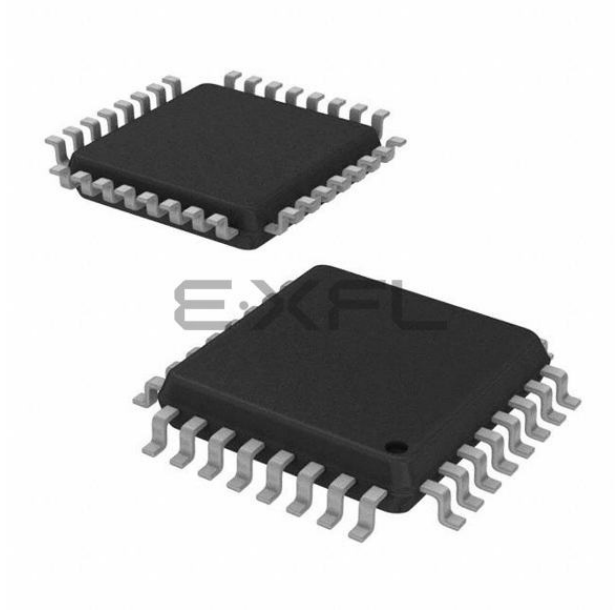

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST7
Core Size	8-Bit
Speed	8MHz
Connectivity	SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	3.8V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st72f324bk4t3tr

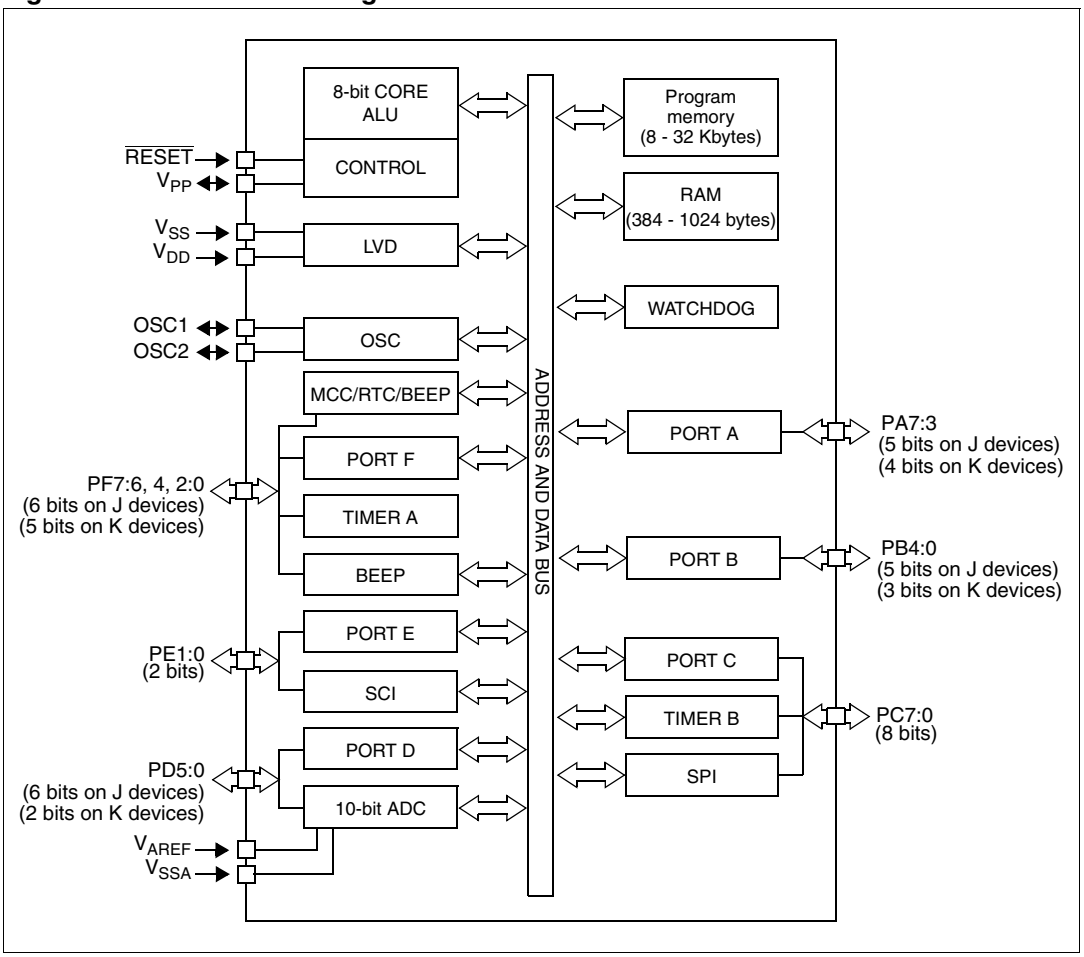
1 Description

The ST72324B-Auto devices are members of the ST7 microcontroller family designed for mid-range automotive applications running from 3.8 to 5.5V. Different package options offer up to 32 I/O pins.

All devices are based on a common industry-standard 8-bit core, featuring an enhanced instruction set and are available with Flash or ROM program memory. The ST7 family architecture offers both power and flexibility to software developers, enabling the design of highly efficient and compact application code.

The on-chip peripherals include an A/D converter, two general purpose timers, an SPI interface and an SCI interface. For power economy, the microcontroller can switch dynamically into, Slow, Wait, Active Halt or Halt mode when the application is in idle or stand-by state.

Figure 1. Device block diagram



Typical applications include

- all types of car body applications such as window lift, DC motor control, rain sensors
- safety microcontroller in airbag and engine management applications
- auxiliary functions in car radios

Table 2. Device pin description (continued)

Pin			Type	Level		Port						Main function (after reset)	Alternate function
No.		Name		Input	Output	Input				Output			
LQFP44	LQFP32					float	wpu	int	ana	OD	PP		
2	28	PB0	I/O	C_T		**X**	ei2			X	X	Port B0	**Caution:** Negative current injection not allowed on this pin on 8/16 Kbyte Flash devices.(4)
3	-	PB1	I/O	C_T		**X**	ei2			X	X	Port B1	
4	-	PB2	I/O	C_T		**X**	ei2			X	X	Port B2	
5	29	PB3	I/O	C_T		**X**		ei2		X	X	Port B3	

1. It is mandatory to connect all available V_{DD} and V_{REF} pins to the supply voltage and all V_{SS} and V_{SSA} pins to ground.
2. On the chip, each I/O port has eight pads. Pads that are not bonded to external pins are in input pull-up configuration after reset. The configuration of these pads must be kept at reset state to avoid added current consumption..
3. OSC1 and OSC2 pins connect a crystal/ceramic resonator, or an external source to the on-chip oscillator; see *Section 1: Description* and *Section 12.6: Clock and timing characteristics* or more details.
4. For details refer to *Section 12.9.1 on page 162*

Legend / Abbreviations for *Table 2:*

Type:I = input, O = output, S = supply

Input level: A = Dedicated analog input

In/Output level: C = CMOS $0.3V_{DD}/0.7_{DD}$
C_T = CMOS $0.3V_{DD}/0.7_{DD}$ with input trigger

Output level: HS = 20mA high sink (on N-buffer only)

Port and control configuration:

Input:float = floating, wpu = weak pull-up, int = interrupt(a), ana = analog ports

Output:OD = open drain(b), PP = push-pull

a. In the interrupt input column, “eiX” defines the associated external interrupt vector. If the weak pull-up column (wpu) is merged with the interrupt column (int), then the I/O configuration is pull-up interrupt input, else the configuration is floating interrupt input.

b. In the open drain output column, ‘T’ *defines a true open drain I/O (P-Buffer and protection diode to V_{DD} are not implemented). See Section 9: I/O ports and Section 12.9: I/O port pin characteristics for more details.*

4.3.1 Readout protection

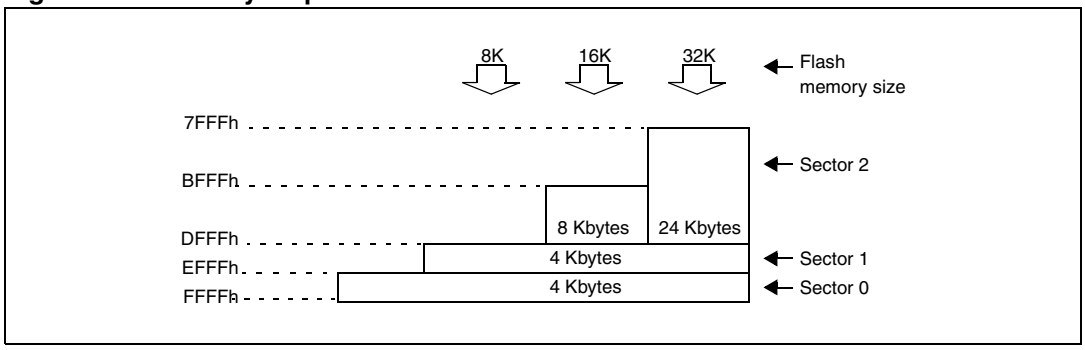
Readout protection, when selected, provides a protection against program memory content extraction and against write access to Flash memory. Even if no protection can be considered as totally unbreakable, the feature provides a very high level of protection for a general purpose microcontroller.

In Flash devices, this protection is removed by reprogramming the option. In this case, the entire program memory is first automatically erased.

Readout protection selection depends on the device type:

- In Flash devices it is enabled and removed through the FMP_R bit in the option byte.
- In ROM devices it is enabled by mask option specified in the option list.

Figure 5. Memory map and sector address



4.4 ICC interface

ICC needs a minimum of 4 and up to 6 pins to be connected to the programming tool (see *Figure 6*). These pins are:

- $\overline{\text{RESET}}$: device reset
- V_{SS}: device power supply ground
- ICCCLK: ICC output serial clock pin
- ICCDATA: ICC input/output serial data pin
- ICCSEL/V_{PP}: programming voltage
- OSC1 (or OSCIN): main clock input for external source (optional)
- V_{DD}: application board power supply (optional, see *Figure 6*, Note 3).

4.6 IAP (in-application programming)

This mode uses a BootLoader program previously stored in Sector 0 by the user (in ICP mode or by plugging the device in a programming tool).

This mode is fully controlled by user software. This allows it to be adapted to the user application, (such as user-defined strategy for entering programming mode, choice of communications protocol used to fetch the data to be stored). For example, it is possible to download code from the SPI, SCI, USB or CAN interface and program it in the Flash. IAP mode can be used to program any of the Flash sectors except Sector 0, which is write/erase protected to allow recovery in case errors occur during the programming operation.

4.7 Related documentation

For details on Flash programming and ICC protocol, refer to the *ST7 Flash Programming Reference Manual* and to the *ST7 ICC Protocol Reference Manual*.

4.7.1 Flash Control/Status Register (FCSR)

This register is reserved for use by programming tool software. It controls the Flash programming and erasing operations.

FCSR Reset value:0000 0000 (00h)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 5. Flash control/status register address and reset value

Address (Hex)	Register label	7	6	5	4	3	2	1	0
0029h	FCSR reset value	0	0	0	0	0	0	0	0

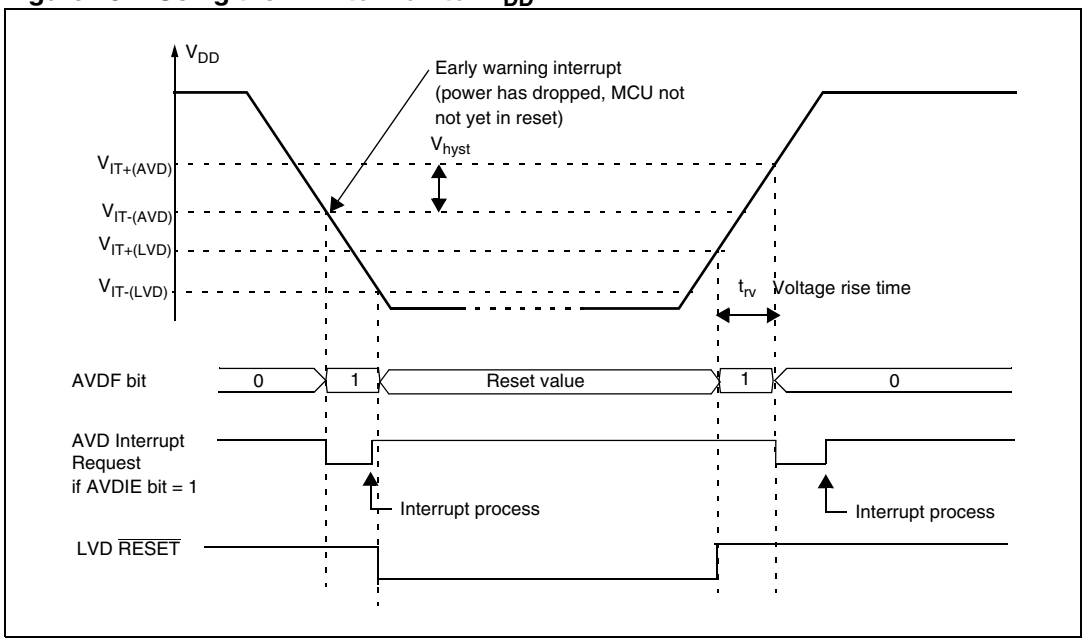
The interrupt on the rising edge is used to inform the application that the V_{DD} warning state is over.

If the voltage rise time t_{rv} is less than 256 or 4096 CPU cycles (depending on the reset delay selected by option byte), no AVD interrupt will be generated when $V_{IT+(AVD)}$ is reached.

If t_{rv} is greater than 256 or 4096 cycles then:

- If the AVD interrupt is enabled before the $V_{IT+(AVD)}$ threshold is reached, then 2 AVD interrupts will be received: the first when the AVDIE bit is set, and the second when the threshold is reached.
- If the AVD interrupt is enabled after the $V_{IT+(AVD)}$ threshold is reached then only one AVD interrupt will occur.

Figure 15. Using the AVD to monitor V_{DD}



6.5.3 Low power modes

Table 10. Effect of low power modes on SI

Mode	Description
Wait	No effect on SI. AVD interrupt causes the device to exit from Wait mode.
Halt	The CRSR register is frozen.

6.5.4 Interrupts

The AVD interrupt event generates an interrupt if the AVDIE bit is set and the interrupt mask in the CC register is reset (RIM instruction).

Table 11. AVD interrupt control/wake-up capability

Interrupt event	Event flag	Enable Control bit	Exit from WAIT	Exit from HALT
AVD event	AVDF	AVDIE	Yes	No

They can be also set/cleared by software with the RIM, SIM, HALT, WFI, IRET and PUSH/POP instructions (see *Table 18: Dedicated interrupt instruction set*).

7.5.2 Interrupt software priority registers (ISPRx)

ISPRx Reset value: 1111 1111 (FFh)

	7	6	5	4	3	2	1	0
ISPR0	I1_3	I0_3	I1_2	I0_2	I1_1	I0_1	I1_0	I0_0
ISPR1	I1_7	I0_7	I1_6	I0_6	I1_5	I0_5	I1_4	I0_4
ISPR2	I1_11	I0_11	I1_10	I0_10	I1_9	I0_9	I1_8	I0_8
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ISPR3	1	1	1	1	I1_13	I0_13	I1_12	I0_12
	RO	RO	RO	RO	R/W	R/W	R/W	R/W

These four registers contain the interrupt software priority of each interrupt vector.

- Each interrupt vector (except reset and TRAP) has corresponding bits in these registers where its own software priority is stored. This correspondence is shown in the following *Table 17*.

Table 17. ISPRx interrupt vector correspondence

Vector address	ISPRx bits
FFFBh-FFFAh	I1_0 and I0_0 bits
FFF9h-FFF8h	I1_1 and I0_1 bits
...	...
FFE1h-FFE0h	I1_13 and I0_13 bits

- Each I1_x and I0_x bit value in the ISPRx registers has the same meaning as the I1 and I0 bits in the CC register.
- Level 0 cannot be written (I1_x = 1, I0_x = 0). In this case, the previously stored value is kept (for example, previous value = CFh, write = 64h, result = 44h).

The reset, and TRAP vectors have no software priorities. When one is serviced, the I1 and I0 bits of the CC register are both set.

Caution: If the I1_x and I0_x bits are modified while the interrupt x is executed the following behavior has to be considered: If the interrupt x is still pending (new interrupt or flag not cleared) and the new software priority is higher than the previous one, the interrupt x is re-entered. Otherwise, the software priority stays unchanged up to the next interrupt request (after the IRET of the interrupt x).

Table 18. Dedicated interrupt instruction set(1)

Instruction	New description	Function/example	I1	H	I0	N	Z	C
HALT	Entering HALT mode		1		0			

Figure 26. HALT timing overview

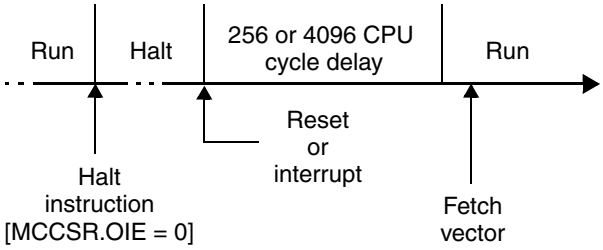
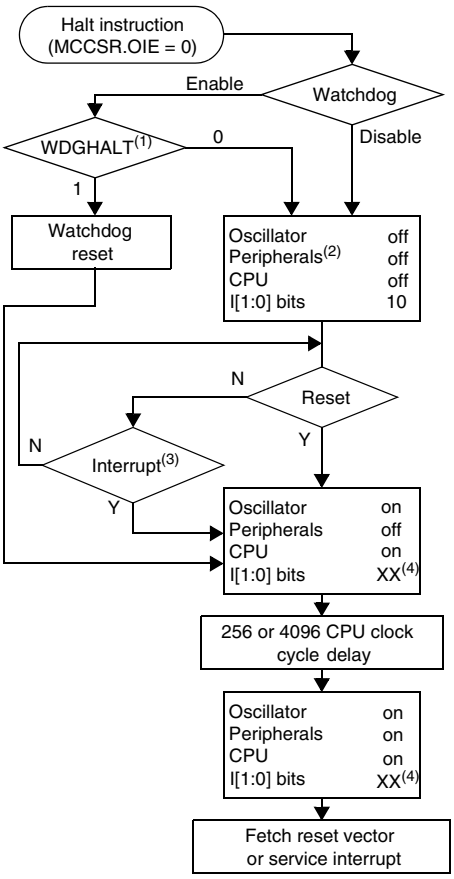


Figure 27. Halt mode flowchart



1. WDGHALT is an option bit. See *Section 14.1 on page 179* for more details.
2. Peripheral clocked with an external clock source can still be active.
3. Only some specific interrupts can exit the MCU from Halt mode (such as external interrupt). Refer to *Table 25: Interrupt mapping*for more details.
4. Before servicing an interrupt, the CC register is pushed on the stack. The I[1:0] bits of the CC register are set to the current software priority level of the interrupt routine and recovered when the CC register is popped.

10.2.2 Clock-out capability

The clock-out capability is an alternate function of an I/O port pin that outputs the f_{CPU} clock to drive external devices. It is controlled by the MCO bit in the MCCSR register.

Caution: When selected, the clock out pin suspends the clock during Active Halt mode.

10.2.3 Real-time clock (RTC) timer

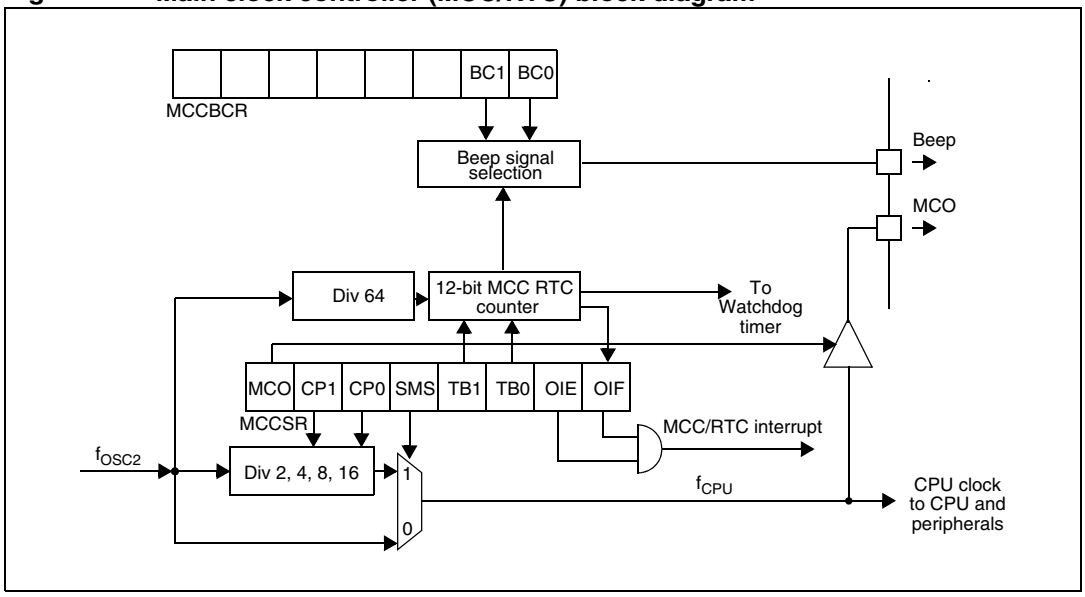
The counter of the real-time clock timer allows an interrupt to be generated based on an accurate real-time clock. Four different time bases depending directly on f_{OSC2} are available. The whole functionality is controlled by four bits of the MCCSR register: TB[1:0], OIE and OIF.

When the RTC interrupt is enabled (OIE bit set), the ST7 enters Active Halt mode when the HALT instruction is executed. See *Section 8.4: Active Halt and Halt modes on page 54*for more details.

10.2.4 Beeper

The beep function is controlled by the MCCBCR register. It can output three selectable frequencies on the Beep pin (I/O port alternate function).

Figure 33. Main clock controller (MCC/RTC) block diagram



Input Capture 1 High Register (IC1HR)

This is an 8-bit register that contains the high part of the counter value (transferred by the input capture 1 event).

IC1HR Reset value: undefined

7	6	5	4	3	2	1	0
MSB							LSB
RO	RO	RO	RO	RO	RO	RO	RO

Input Capture 1 Low Register (IC1LR)

This is an 8-bit register that contains the low part of the counter value (transferred by the input capture 1 event).

IC1LR — Reset value: undefined

7	6	5	4	3	2	1	0
MSB							LSB
RO	RO	RO	RO	RO	RO	RO	RO

Output Compare 1 High Register (OC1HR)

This is an 8-bit register that contains the high part of the value to be compared to the CHR register.

OC1HR — Reset value: 1000 0000 (80h)

7	6	5	4	3	2	1	0
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Output Compare 1 Low Register (OC1LR)

This is an 8-bit register that contains the low part of the value to be compared to the CLR register.

OC1LR — Reset value: 0000 0000 (00h)

7	6	5	4	3	2	1	0
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Output Compare 2 High Register (OC2HR)

This is an 8-bit register that contains the high part of the value to be compared to the CHR register.

OC2HR — Reset value: 1000 0000 (80h)

7	6	5	4	3	2	1	0
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

10.5.3 General description

The interface is externally connected to another device by two pins (see *Figure 56*):

- TDO: Transmit Data Output. When the transmitter and the receiver are disabled, the output pin returns to its I/O port configuration. When the transmitter and/or the receiver are enabled and nothing is to be transmitted, the TDO pin is at high level.
- RDI: Receive Data Input is the serial data input. Oversampling techniques are used for data recovery by discriminating between valid incoming data and noise.

Through these pins, serial data is transmitted and received as frames comprising:

- an Idle Line prior to transmission or reception
- a start bit
- a data word (8 or 9 bits) least significant bit first
- a Stop bit indicating that the frame is complete

This interface uses two types of baud rate generator:

- a conventional type for commonly-used baud rates
- an extended type with a prescaler offering a very wide range of baud rates even with non-standard oscillator frequencies

Break characters

Setting the SBK bit loads the shift register with a break character. The break frame length depends on the M bit (see *Figure 56*).

As long as the SBK bit is set, the SCI send break frames to the TDO pin. After clearing this bit by software the SCI insert a logic 1 bit at the end of the last break frame to guarantee the recognition of the start bit of the next frame.

Idle characters

Setting the TE bit drives the SCI to send an idle frame before the first data frame.

Clearing and then setting the TE bit during a transmission sends an idle frame after the current word.

Note: Resetting and setting the TE bit causes the data in the TDR register to be lost. Therefore, the best time to toggle the TE bit is when the TDRE bit is set, that is, before writing the next byte in the SCIDR.

Receiver

The SCI can receive data words of either 8 or 9 bits. When the M bit is set, word length is 9 bits and the MSB is stored in the R8 bit in the SCICR1 register.

Character reception

During a SCI reception, data shifts in least significant bit first through the RDI pin. In this mode, the SCIDR register consists or a buffer (RDR) between the internal bus and the received shift register (see *Figure 55*).

Procedure

1. Select the M bit to define the word length.
2. Select the desired baud rate using the SCIBRR and the SCIERPR registers.
3. Set the RE bit, this enables the receiver which begins searching for a start bit.

When a character is received:

- The RDRF bit is set. It indicates that the content of the shift register is transferred to the RDR.
- An interrupt is generated if the RIE bit is set and the I bit is cleared in the CCR register.
- The error flags can be set if a frame error, noise or an overrun error has been detected during reception.

Clearing the RDRF bit is performed by the following software sequence done by:

1. An access to the SCISR register

2. A read to the SCIDR register.

The RDRF bit must be cleared before the end of the reception of the next character to avoid an overrun error.

Break character

When a break character is received, the SCI handles it as a framing error.

Idle character

When a idle frame is detected, there is the same procedure as a data received character plus an interrupt if the ILIE bit is set and the I bit is cleared in the CCR register.

Table 63. SCICR1 register description (continued)

Bit	Name	Function
3	WAKE	Wake-Up method This bit determines the SCI Wake-Up method, it is set or cleared by software. 0: Idle line 1: Address mark
2	PCE	Parity Control Enable This bit selects the hardware parity control (generation and detection). When the parity control is enabled, the computed parity is inserted at the MSB position (9th bit if M = 1; 8th bit if M = 0) and parity is checked on the received data. This bit is set and cleared by software. Once it is set, PCE is active after the current byte (in reception and in transmission). 0: Parity control disabled 1: Parity control enabled
1	PS	Parity Selection This bit selects the odd or even parity when the parity generation/detection is enabled (PCE bit set). It is set and cleared by software. The parity will be selected after the current byte. 0: Even parity 1: Odd parity
0	PIE	Parity Interrupt Enable This bit enables the interrupt capability of the hardware parity control when a parity error is detected (PE bit set). It is set and cleared by software. 0: Parity error interrupt disabled 1: Parity error interrupt enabled

SCI Control Register 2 (SCICR2)

SCICR2 Reset value: 0000 0000 (00h)

7	6	5	4	3	2	1	0
TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 64. SCICR2 register description

Bit	Name	Function
7	TIE	Transmitter Interrupt Enable This bit is set and cleared by software. 0: Interrupt is inhibited 1: An SCI interrupt is generated whenever TDRE = 1 in the SCISR register.
6	TCIE	Transmission Complete Interrupt Enable This bit is set and cleared by software. 0: Interrupt is inhibited 1: An SCI interrupt is generated whenever TC = 1 in the SCISR register.

14 Device configuration and ordering information

Each device is available for production in user programmable versions (Flash) as well as in factory coded versions (ROM/FASTROM).

ST72324B-Auto devices are ROM versions. ST72P324B-Auto devices are Factory Advanced Service Technique ROM (FASTROM) versions: They are factory-programmed HDFlash devices. Flash devices are shipped to customers with a default content (FFh), while ROM factory coded parts contain the code supplied by the customer. This implies that Flash devices have to be configured by the customer using the Option bytes while the ROM devices are factory-configured.

14.1 Flash devices

14.1.1 Flash configuration

Table 116. Flash option bytes

	Static option byte 0								Static option byte 1							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	WDG		Res	VD		Reserved		FMP_R	PKG1	RSTC	OSCTYPE		OSCRANGE			PLLOFF
	HALT	SW		1	0						1	0	2	1	0	
Default	1	1	1	0	0	1	1	1	See note 1	1	1	0	0	1	1	1

1. Depends on device type as defined in *Table 119: Package selection (OPT7) on page 181*

The option bytes allow the hardware configuration of the microcontroller to be selected. They have no address in the memory map and can be accessed only in programming mode (for example using a standard ST7 programming tool). The default content of the Flash is fixed to FFh. To program directly the Flash devices using ICP, Flash devices are shipped to customers with the internal RC clock source. In masked ROM devices, the option bytes are fixed in hardware by the ROM code (see option list).

Table 117. Option byte 0 bit description

Bit	Name	Function
OPT7	WDG HALT	Watchdog reset on HALT This option bit determines if a reset is generated when entering Halt mode while the Watchdog is active. 0: No reset generation when entering Halt mode 1: Reset generation when entering Halt mode
OPT6	WDG SW	Hardware or software Watchdog This option bit selects the Watchdog type. 0: Hardware (Watchdog always enabled) 1: Software (Watchdog to be enabled by software)

Table 117. Option byte 0 bit description (continued)

Bit	Name	Function
OPT5	-	Reserved, must be kept at default value.
OPT4:3	VD[1:0]	Voltage detection These option bits enable the voltage detection block (LVD and AVD) with a selected threshold for the LVD and AVD. 00: Selected LVD = Highest threshold (V_{DD}~4V). 01: Selected LVD = Medium threshold (V_{DD}~3.5V). 10: Selected LVD = Lowest threshold (V_{DD}~3V). 11: LVD and AVD off **Caution:** If the medium or low thresholds are selected, the detection may occur outside the specified operating voltage range. Below 3.8V, device operation is not guaranteed. For details on the AVD and LVD threshold levels refer to *Section 12.4.1 on page 149*.
OPT2:1	-	Reserved, must be kept at default value
OPT0	FMP_R	Flash memory readout protection Readout protection, when selected, provides a protection against program memory content extraction and against write access to Flash memory. Erasing the option bytes when the FMP_R option is selected causes the whole user memory to be erased first, afterwhich the device can be reprogrammed. Refer to *Section 4.3.1 on page 23* and the *ST7 Flash Programming Reference Manual* for more details. 0: Readout protection enabled 1: Readout protection disabled

Table 118. Option byte 1 bit description

Bit	Name	Function
OPT7	PKG1	Pin package selection bit This option bit selects the package (see *Table 119*). *Note: On the chip, each I/O port has eight pads. Pads that are not bonded to external pins are in input pull-up configuration after reset. The configuration of these pads must be kept at reset state to avoid added current consumption.*
OPT6	RSTC	Reset clock cycle selection This option bit selects the number of CPU cycles applied during the reset phase and when exiting Halt mode. For resonator oscillators, it is advised to select 4096 due to the long crystal stabilization time. 0: Reset phase with 4096 CPU cycles 1: Reset phase with 256 CPU cycles
OPT5:4	OSCTYPE[1:0]	Oscillator type These option bits select the ST7 main clock source type. 00: Clock source = Resonator oscillator 01: Reserved 10: Clock source = Internal RC oscillator 11: Clock source = External source

Table 118. Option byte 1 bit description (continued)

Bit	Name	Function
OPT3:1	OSCRANGE[2:0]	Oscillator range When the resonator oscillator type is selected, these option bits select the resonator oscillator current source corresponding to the frequency range of the used resonator. When the external clock source is selected, these bits are set to medium power (2 ~ 4 MHz). 000: Typ. frequency range (LP) = 1 ~ 2 MHz 001: Typ. frequency range (MP) = 2 ~ 4 MHz 010: Typ. frequency range (MS) = 4 ~ 8 MHz 011: Typ. frequency range (HS) = 8 ~ 16 MHz
OPT0	PLL OFF	PLL activation This option bit activates the PLL which allows multiplication by two of the main input clock frequency. The PLL must not be used with the internal RC oscillator. The PLL is guaranteed only with an input frequency between 2 and 4 MHz. 0: PLL x2 enabled 1: PLL x2 disabled **Caution**: The PLL can be enabled only if the “OSCRANGE” (OPT3:1) bits are configured to “MP - 2~4 MHz”. Otherwise, the device functionality is not guaranteed.

Table 119. Package selection (OPT7)

Version	Selected package	PKG1
J	LQFP44	1
K	LQFP32	0

ST72324B-Auto Microcontroller FASTROM/ROM Option List

(Last update: July 2007)

Customer: . . . . . .
Address: . . . . . .
. . . . . .
Contact: . . . . . .
Phone No: . . . . . .
Reference: . . . . . .

The FASTROM/ROM code name is assigned by STMicroelectronics.
FASTROM/ROM code must be sent in .S19 format. .Hex extension cannot be processed.

Device Type/Memory Size/Package (check only one option):

FASTROM DEVICE:	32K	16K	8K
LQFP44 10x10:	[ ] ST72P324B(J6)T	[ ] ST72P324B(J4)T	[ ] ST72P324B(J2)T
LQFP32 7x17:	[ ] ST72P324B(K6)T	[ ] ST72P324B(K4)T	[ ] ST72P324B(K2)T

ROM DEVICE:	32K	16K	8K
LQFP44 10x10:	[ ] ST72324B(J6)T	[ ] ST72324B(J4)T	[ ] ST72324B(J2)T
LQFP32 7x7:	[ ] ST72324B(K6)T	[ ] ST72324B(K4)T	[ ] ST72324B(K2)T

Conditioning for LQFP package (check only one option):

[ ] Tape and Reel [ ] Tray

Temperature range :
[ ] A (-40°C to +85°C)
[ ] B (-40°C to +105°C)
[ ] C (-40°C to +125°C)
[ ] D (-40°C to +150°C)

Special Marking: [ ] No [ ] Yes "_ _ _ _ _ _ _ _ _ _"
LQFP32: 7 characters max. Other packages: 10 characters max.
Authorized characters are letters, digits, '.', '-', '/' and spaces only.

Clock Source Selection: [ ] Resonator:
[ ] LP: Low power resonator (1 to 2 MHz)
[ ] MP: Medium power resonator (2 to 4 MHz)
[ ] MS: Medium speed resonator (4 to 8 MHz)
[ ] HS: High speed resonator (8 to 16 MHz)
[ ] Internal RC
[ ] External clock (sets MP medium power resonator in option byte)

PLL (1)(2) [ ] Disabled [ ] Enabled

LVD reset [ ] Disabled [ ] High threshold
[ ] Medium threshold [ ] Low threshold

Reset delay [ ] 256 cycles [ ] 4096 cycles

Watchdog selection [ ] Software activation [ ] Hardware activation

Halt when Watchdog on [ ] Reset [ ] No reset

Readout protection [ ] Disabled [ ] Enabled

Date . . . . . Signature . . . . . .

1. PLL must be disabled if internal RC network is selected.
2. The PLL can be enabled only if the resonator is configured to “Medium power: 2~4 MHz”.

CAUTION: The readout protection binary value is inverted between ROM and Flash products. The option byte checksum will differ between ROM and Flash.

Table 123. Document revision history (continued)

Date	Revision	Changes
23-Jul-2007	2 (cont'd)	*Table 121: Flash user programmable device types on page 189*: - added footnote to order code column - modified order codes - replaced R with TR for tape and reel in order codes *Figure 89: Flash commercial product code structure on page 183*: - replaced R with TR for tape and reel - changed presentation of temperature ranges *Section 14.2: ROM device ordering information and transfer of customer code on page 184*: Added links to option list, to *Table 122* and to *Table 123* *Table 122: FASTROM factory coded device types on page 191*: - added footnote to order code column - modified order codes *Figure 90: FASTROM commercial product code structure on page 184*: Changed presentation of temperature ranges *Table 123: ROM factory coded device types on page 192*: - added footnote to order code column - modified order codes *Figure 91: ROM commercial product code structure on page 184*: s - changed title - changed presentation of temperature range *ST72324B-Auto Microcontroller FASTROM/ROM Option List on page 185*: - replaced ST72324B with ST72324B-Auto in title - grouped device code characters defining pinout and memory size in parentheses - modified special marking max characters allowed
10-Jun-2010	3	Removed section covering differences between automotive and standard devices. *Table 86: Operating conditions on page 148*: -added D temperature range *Section 12.8.3: Absolute maximum ratings (electrical sensitivity) on page 160* - standard microcontrollers: HB and CDM models specified only - automotive microcontrollers: plus an additional test of MM *Figure 90: ST72F324Bxx-Auto Flash commercial product structure on page 182* and *Figure 91: ST72P324Bxx-Auto FastROM commercial product structure on page 184*: - modified figure to reflect leadfree package in Catania (from E to S). - modified tape and reel symbol from R to X or TX. -Table 121.Flash user programmable device removed. -Table 122.FASTROM factory coded device removed. *Figure 92: ST72324Bxx-Auto ROM commercial product structure on page 185*: - modified figure to reflect leadfree package in Catania (from E to S). - modified tape and reel symbol from R to X or TX. - added D temperature range. -Table 123.ROM factory coded device removed. Option List ordering sheet: added D temperature range