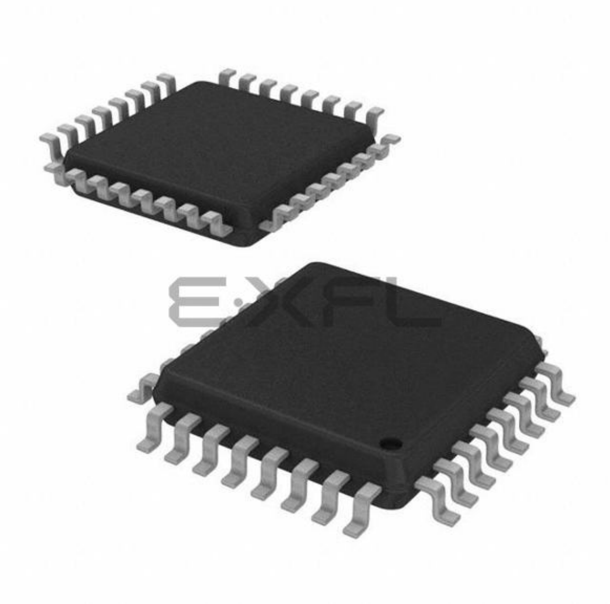

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST7
Core Size	8-Bit
Speed	8MHz
Connectivity	SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	3.8V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st72f324bk4tae

5 Central processing unit (CPU)

5.1 Introduction

This CPU has a full 8-bit architecture and contains six internal registers allowing efficient 8-bit data manipulation.

5.2 Main features

- Enable executing 63 basic instructions
- Fast 8-bit by 8-bit multiply
- 17 main addressing modes (with indirect addressing mode)
- Two 8-bit index registers
- 16-bit stack pointer
- Low power Halt and Wait modes
- Priority maskable hardware interrupts
- Non-maskable software/hardware interrupts

5.3 CPU registers

The six CPU registers shown in *Figure 7* are not present in the memory mapping and are accessed by specific instructions.

Figure 7. CPU registers

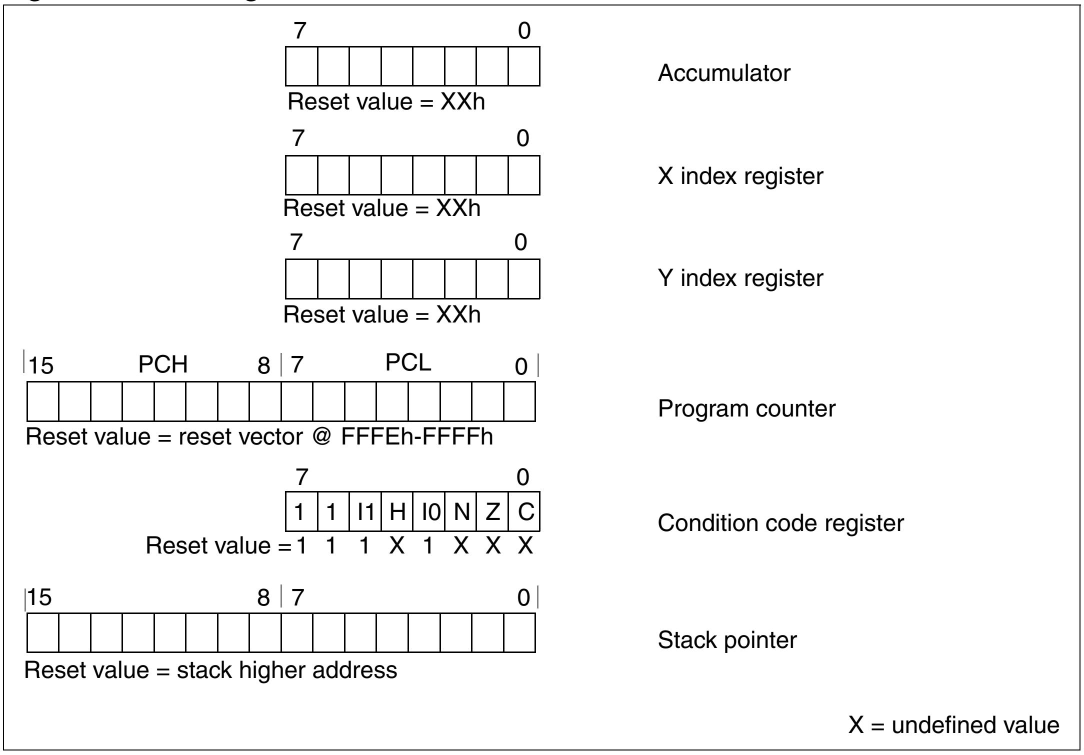
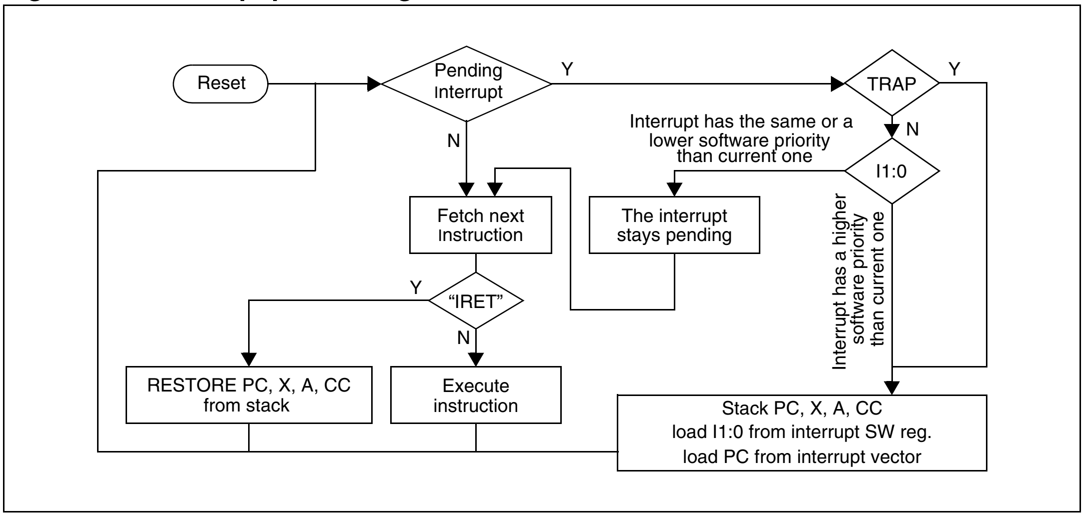


Table 14. Interrupt software priority levels

Interrupt software priority	Level	I1	I0
Level 0 (main)	Low	1	0
Level 1	↓	0	1
Level 2		0	0
Level 3 (= interrupt disable)	High	1	1

Figure 16. Interrupt processing flowchart



7.2.1 Servicing pending interrupts

As several interrupts can be pending at the same time, the interrupt to be taken into account is determined by the following two-step process:

- the highest software priority interrupt is serviced,
- if several interrupts have the same software priority then the interrupt with the highest hardware priority is serviced first.

Figure 17 describes this decision process.

Figure 17. Priority decision process flowchart

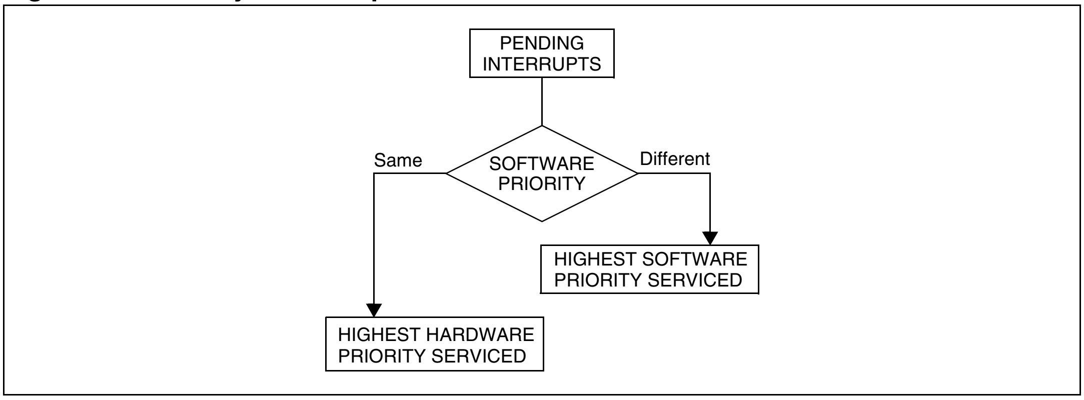


Table 21. Interrupt sensitivity - ei3

IS11	IS10	External interrupt sensitivity
0	0	Falling edge and low level
0	1	Rising edge only
1	0	Falling edge only
1	1	Rising and falling edge

Table 22. Interrupt sensitivity - ei0

IS21	IS20	External interrupt sensitivity	
		IPA bit = 0	IPA bit = 1
0	0	Falling edge and low level	Rising edge and high level
0	1	Rising edge only	Falling edge only
1	0	Falling edge only	Rising edge only
1	1	Rising and falling edge	

Table 23. Interrupt sensitivity - ei1

IS21	IS20	External interrupt sensitivity
0	0	Falling edge and low level
0	1	Rising edge only
1	0	Falling edge only
1	1	Rising and falling edge

Table 24. Nested interrupts register map and reset values

Address (Hex.)	Register label	7	6	5	4	3	2	1	0
0024h	ISPR0 reset value	ei1		ei0		MCC + SI			
		I1_3 1	I0_3 1	I1_2 1	I0_2 1	I1_1 1	I0_1 1	1	1
0025h	ISPR1 reset value	SPI				ei3		ei2	
		I1_7 1	I0_7 1	I1_6 1	I0_6 1	I1_5 1	I0_5 1	I1_4 1	I0_4 1
0026h	ISPR2 reset value	AVD		SCI		Timer B		Timer A	
		I1_11 1	I0_11 1	I1_10 1	I0_10 1	I1_9 1	I0_9 1	I1_8 1	I0_8 1
0027h	ISPR3 reset value	1	1	1	1	I1_13 1	I0_13 1	I1_12 1	I0_12 1
0028h	EICR reset value	IS11 0	IS10 0	IPB 0	IS21 0	IS20 0	IPA 0	0	0

Figure 28. I/O port general block diagram

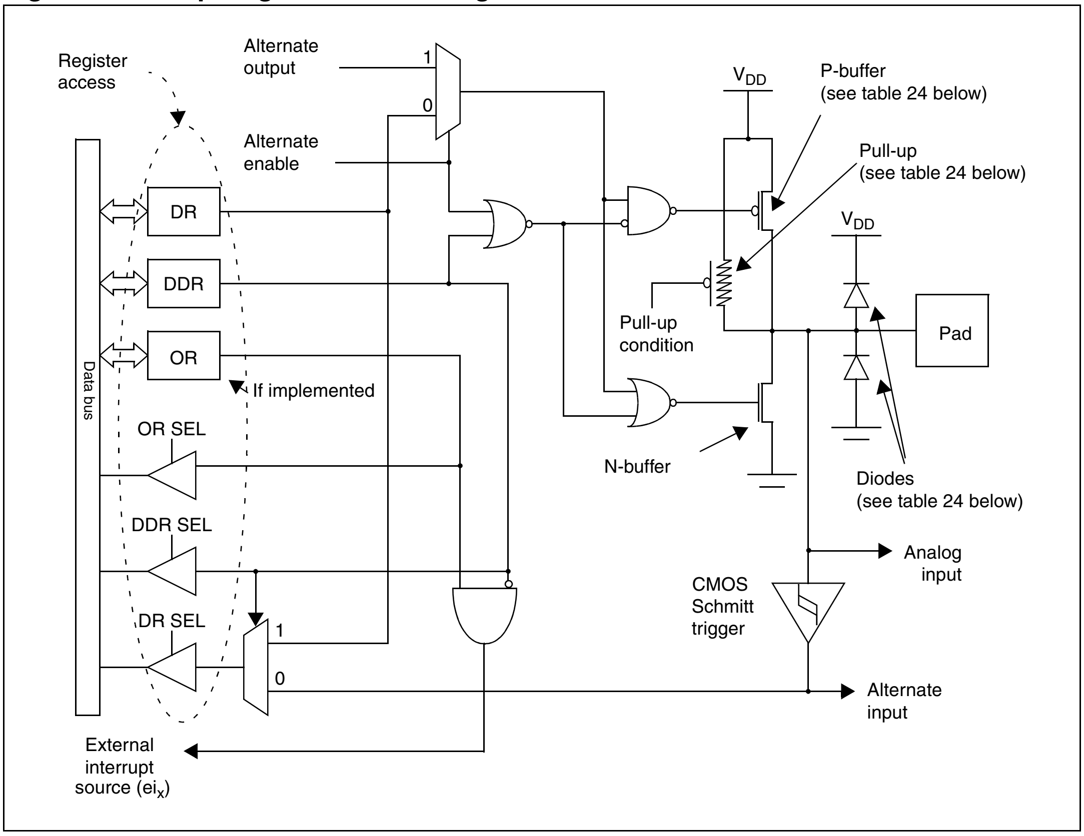


Table 28. I/O port mode options

Configuration mode		Pull-up	P-buffer	Diodes: to V_{DD}[1]	Diodes: to V_{SS}[2]
Input	Floating with/without Interrupt	Off[3]	Off	On	On
	Pull-up with/without Interrupt	On[4]			
Output	Push-pull	Off	On		
	Open drain (logic level)		Off		
	True open drain	NI	NI	NI[5]	

1. The diode to V_{DD} is not implemented in the true open drain pads.
2. A local protection between the pad and V_{SS} is implemented to protect the device against positive stress.
3. Off = implemented not activated.
4. On = implemented and activated.
5. NI = not implemented

External clock

The external clock (where available) is selected if CC0 = 1 and CC1 = 1 in the CR2 register.

The status of the EXEDG bit in the CR2 register determines the type of level transition on the external clock pin EXTCLK that will trigger the free running counter.

The counter is synchronized with the falling edge of the internal CPU clock.

A minimum of four falling edges of the CPU clock must occur between two consecutive active edges of the external clock; thus the external clock frequency must be less than a quarter of the CPU clock frequency.

Figure 36. Counter timing diagram, internal clock divided by 2

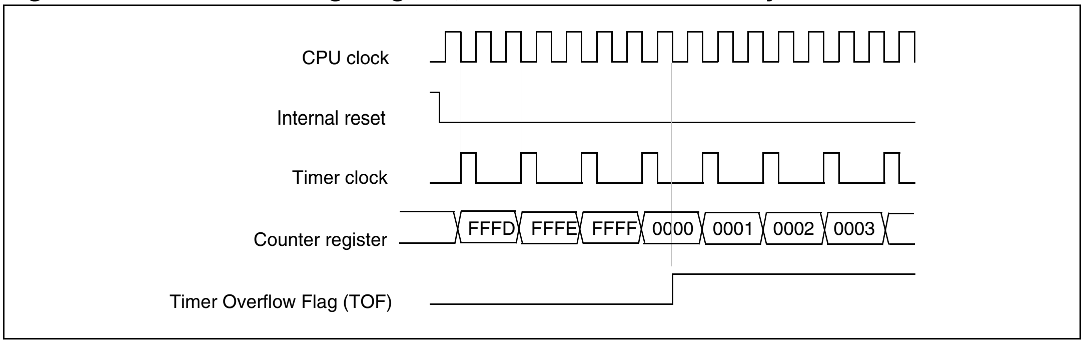


Figure 37. Counter timing diagram, internal clock divided by 4

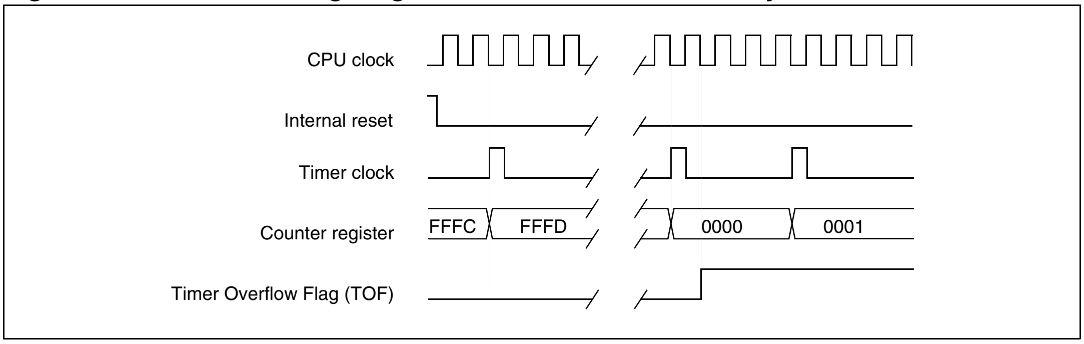
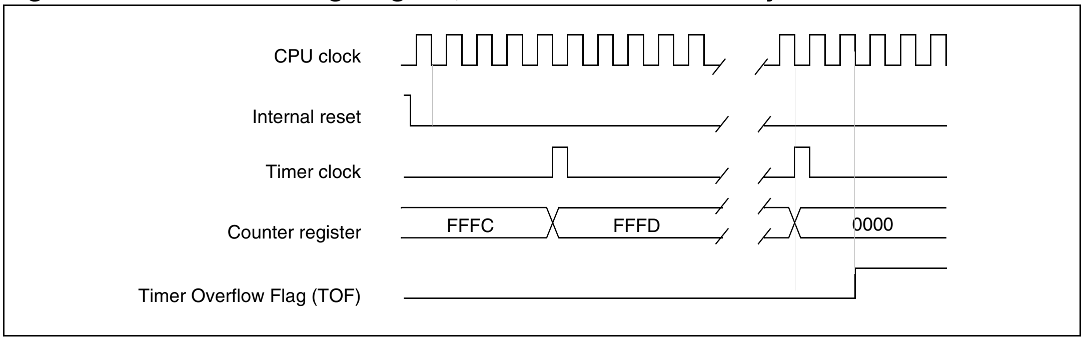
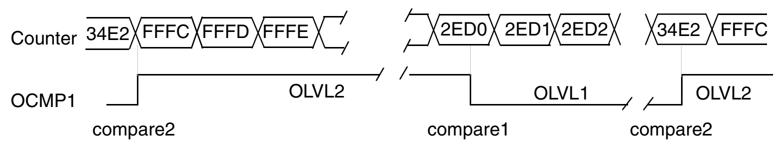


Figure 38. Counter timing diagram, internal clock divided by 8



Note: The MCU is in reset state when the internal reset signal is high, when it is low the MCU is running.

Figure 46. Pulse width modulation mode timing example with two output compare functions(1)(2)



1. OC1R = 2ED0h, OC2R = 34E2, OLVL1 = 0, OLVL2 = 1
2. On timers with only one Output Compare register, a fixed frequency PWM signal can be generated using the output compare and the counter overflow to define the pulse length.

Pulse Width Modulation mode

Pulse Width Modulation (PWM) mode enables the generation of a signal with a frequency and pulse length determined by the value of the OC1R and OC2R registers.

Pulse Width Modulation mode uses the complete Output Compare 1 function plus the OC2R register, and so this functionality can not be used when PWM mode is activated.

In PWM mode, double buffering is implemented on the output compare registers. Any new values written in the OC1R and OC2R registers are taken into account only at the end of the PWM period (OC2) to avoid spikes on the PWM output pin (OCMP1).

Procedure

To use Pulse Width Modulation mode:

1. Load the OC2R register with the value corresponding to the period of the signal using the formula below.
2. Load the OC1R register with the value corresponding to the period of the pulse if (OLVL1 = 0 and OLVL2 = 1) using the formula in the opposite column.
3. Select the following in the CR1 register:
   – Using the OLVL1 bit, select the level to be applied to the OCMP1 pin after a successful comparison with the OC1R register.
   – Using the OLVL2 bit, select the level to be applied to the OCMP1 pin after a successful comparison with the OC2R register.
4. Select the following in the CR2 register:
   – Set OC1E bit: the OCMP1 pin is then dedicated to the output compare 1 function.
   – Set the PWM bit.
   – Select the timer clock (CC[1:0]) (see *Table 50*).

Table 50. CR2 register description

Bit	Name	Function
7	OCIE	Output Compare 1 Pin Enable This bit is used only to output the signal from the timer on the OCMP1 pin (OLV1 in Output Compare mode, both OLV1 and OLV2 in PWM and One-Pulse mode). Whatever the value of the OC1E bit, the Output Compare 1 function of the timer remains active. 0: OCMP1 pin alternate function disabled (I/O pin free for general-purpose I/O). 1: OCMP1 pin alternate function enabled.
6	OC2E	Output Compare 2 Pin Enable This bit is used only to output the signal from the timer on the OCMP2 pin (OLV2 in Output Compare mode). Whatever the value of the OC2E bit, the Output Compare 2 function of the timer remains active. 0: OCMP2 pin alternate function disabled (I/O pin free for general-purpose I/O). 1: OCMP2 pin alternate function enabled.
5	OPM	One Pulse Mode 0: One Pulse mode is not active. 1: One Pulse mode is active, the ICAP1 pin can be used to trigger one pulse on the OCMP1 pin; the active transition is given by the IEDG1 bit. The length of the generated pulse depends on the contents of the OC1R register.
4	PWM	Pulse Width Modulation 0: PWM mode is not active. 1: PWM mode is active, the OCMP1 pin outputs a programmable cyclic signal; the length of the pulse depends on the value of OC1R register; the period depends on the value of OC2R register.
3:2	CC[1:0]	Clock Control The timer clock mode depends on these bits. 00: Timer clock = $f_{CPU}/4$ 01: Timer clock = $f_{CPU}/2$ 10: Timer clock = $f_{CPU}/8$ 11: Timer clock = external clock (where available) *Note: If the external clock pin is not available, programming the external clock configuration stops the counter.*
1	IEDG2	Input Edge 2 This bit determines which type of level transition on the ICAP2 pin will trigger the capture. 0: A falling edge triggers the capture. 1: A rising edge triggers the capture.
0	EXEDG	External Clock Edge This bit determines which type of level transition on the external clock pin EXTCLK will trigger the counter register. 0: A falling edge triggers the counter register. 1: A rising edge triggers the counter register.

Control/Status Register (CSR)

CSR Reset value: xxxx x0xx (xxh)

7	6	5	4	3	2	1	0
ICF1	OCF1	TOF	ICF2	OCF2	TIMD	Reserved	
RO	RO	RO	RO	RO	R/W	-	

Table 51. **CSR register description**

Bit	Name	Function
7	ICF1	Input Capture Flag 1 0: No Input Capture (reset value). 1: An Input Capture has occurred on the ICAP1 pin or the counter has reached the OC2R value in PWM mode. To clear this bit, first read the SR register, then read or write the low byte of the IC1R (IC1LR) register.
6	OCF1	Output Compare Flag 1 0: No match (reset value). 1: The content of the free running counter has matched the content of the OC1R register. To clear this bit, first read the SR register, then read or write the low byte of the OC1R (OC1LR) register.
5	TOF	Timer Overflow Flag 0: No timer overflow (reset value). 1: The free running counter rolled over from FFFFh to 0000h. To clear this bit, first read the SR register, then read or write the low byte of the CR (CLR) register. *Note: Reading or writing the ACLR register does not clear TOF.*
4	ICF2	Input Capture Flag 2 0: No input capture (reset value). 1: An Input Capture has occurred on the ICAP2 pin. To clear this bit, first read the SR register, then read or write the low byte of the IC2R (IC2LR) register.
3	OCF2	Output Compare Flag 2 0: No match (reset value). 1: The content of the free running counter has matched the content of the OC2R register. To clear this bit, first read the SR register, then read or write the low byte of the OC2R (OC2LR) register.
2	TIMD	Timer Disable This bit is set and cleared by software. When set, it freezes the timer prescaler and counter and disabled the output functions (OCMP1 and OCMP2 pins) to reduce power consumption. Access to the timer registers is still available, allowing the timer configuration to be changed, or the counter reset, while it is disabled. 0: Timer enabled. 1: Timer prescaler, counter and outputs disabled.
1:0	-	Reserved, must be kept cleared.

Note: In slave mode, continuous transmission is not possible at maximum frequency due to the software overhead for clearing status flags and to initiate the next transmission sequence.

10.4.3 General description

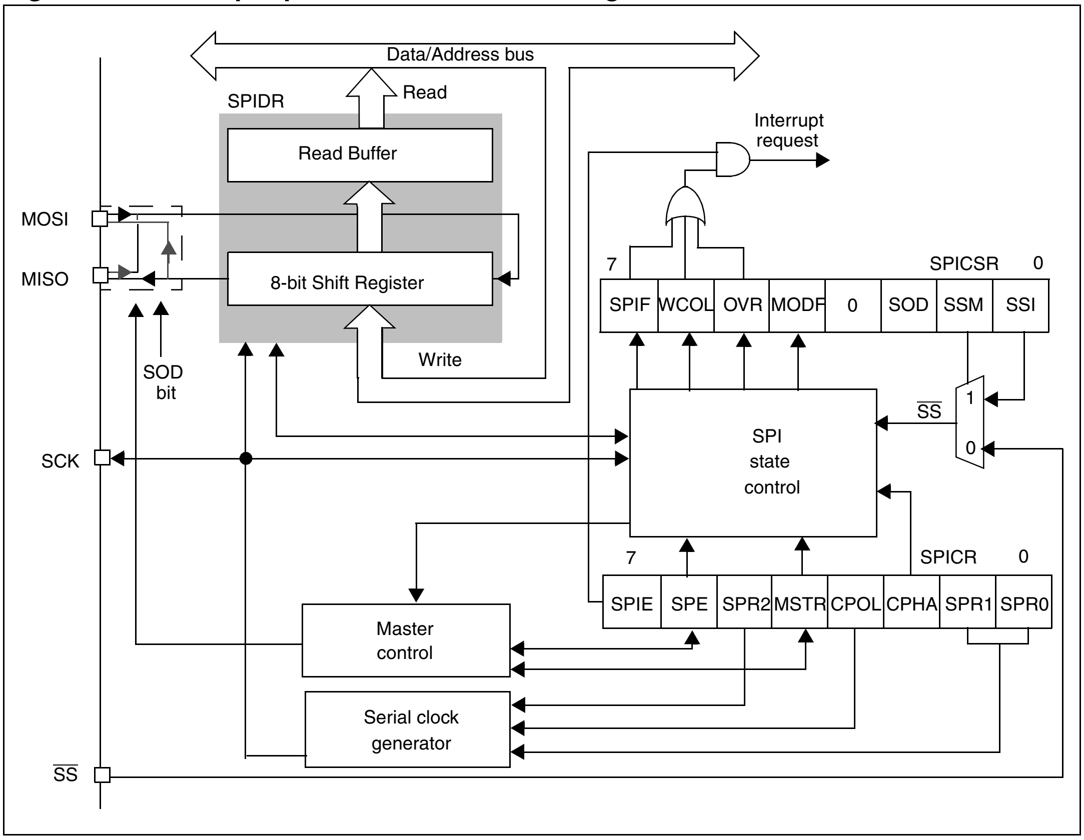
Figure 49 shows the serial peripheral interface (SPI) block diagram. The SPI has three registers:

- SPI Control Register (SPICR)
- SPI Control/Status Register (SPICSR)
- SPI Data Register (SPIDR)

The SPI is connected to external devices through four pins:

- MISO: Master In / Slave Out data
- MOSI: Master Out / Slave In data
- SCK: Serial Clock out by SPI masters and input by SPI slaves
- $\overline{SS}$: Slave select: This input signal acts as a 'chip select' to let the SPI master communicate with slaves individually and to avoid contention on the data lines. Slave $\overline{SS}$ inputs can be driven by standard I/O ports on the master MCU.

Figure 48. Serial peripheral interface block diagram



Functional description

A basic example of interconnections between a single master and a single slave is illustrated in *Figure 49*.

10.4.5 Error flags

Master mode fault (MODF)

Master mode fault occurs when the master device has its $\overline{SS}$ pin pulled low.

When a Master mode fault occurs:

- The MODF bit is set and an SPI interrupt request is generated if the SPIE bit is set.
- The SPE bit is reset. This blocks all output from the device and disables the SPI peripheral.
- The MSTR bit is reset, thus forcing the device into slave mode.

Clearing the MODF bit is done through a software sequence:

1. A read access to the SPICSR register while the MODF bit is set.
2. A write to the SPICR register.

Note: To avoid any conflicts in an application with multiple slaves, the $\overline{SS}$ pin must be pulled high during the MODF bit clearing sequence. The SPE and MSTR bits may be restored to their original state during or after this clearing sequence.

Hardware does not allow the user to set the SPE and MSTR bits while the MODF bit is set except in the MODF bit clearing sequence.

Overrun condition (OVR)

An overrun condition occurs, when the master device has sent a data byte and the slave device has not cleared the SPIF bit issued from the previously transmitted byte.

When an Overrun occurs the OVR bit is set and an interrupt request is generated if the SPIE bit is set.

In this case, the receiver buffer contains the byte sent after the SPIF bit was last cleared. A read to the SPIDR register returns this byte. All other bytes are lost.

The OVR bit is cleared by reading the SPICSR register.

Write collision error (WCOL)

A write collision occurs when the software tries to write to the SPIDR register while a data transfer is taking place with an external device. When this happens, the transfer continues uninterrupted and the software write is unsuccessful.

Write collisions can occur both in master and slave mode. See also *Slave Select management on page 99*.

Note: A read collision will never occur since the received data byte is placed in a buffer in which access is always synchronous with the MCU operation.

The WCOL bit in the SPICSR register is set if a write collision occurs.

No SPI interrupt is generated when the WCOL bit is set (the WCOL bit is a status flag only).

A software sequence clears the WCOL bit (see *Figure 53*).

10.4.8 SPI registers

SPI Control Register (SPICR)

SPICR Reset value: 0000 xxxx (0xh)

7	6	5	4	3	2	1	0
SPIE	SPE	SPR2	MSTR	CPOL	CPHA	SPR[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Table 55. SPICR register description

Bit	Name	Function
7	SPIE	Serial Peripheral Interrupt Enable This bit is set and cleared by software. 0: Interrupt is inhibited. 1: An SPI interrupt is generated whenever SPIF = 1, MODF = 1 or OVR = 1 in the SPICSR register.
6	SPE	Serial Peripheral Output Enable This bit is set and cleared by software. It is also cleared by hardware when, in master mode, $\overline{SS}$ = 0 (see *Master mode fault (MODF) on page 103*). The SPE bit is cleared by reset, so the SPI peripheral is not initially connected to the external pins. 0: I/O pins free for general purpose I/O 1: SPI I/O pin alternate functions enabled
5	SPR2	Divider Enable This bit is set and cleared by software and is cleared by reset. It is used with the SPR[1:0] bits to set the baud rate. Refer to *Table 56: SPI master mode SCK frequency*. 0: Divider by 2 enabled 1: Divider by 2 disabled *Note: This bit has no effect in slave mode.*
4	MSTR	Master mode This bit is set and cleared by software. It is also cleared by hardware when, in master mode, $\overline{SS}$ = 0 (see *Master mode fault (MODF) on page 103*). 0: Slave mode 1: Master mode. The function of the SCK pin changes from an input to an output and the functions of the MISO and MOSI pins are reversed.
3	CPOL	Clock Polarity This bit is set and cleared by software. This bit determines the idle state of the serial Clock. The CPOL bit affects both the master and slave modes. 0: SCK pin has a low level idle state 1: SCK pin has a high level idle state *Note: If CPOL is changed at the communication byte boundaries, the SPI must be disabled by resetting the SPE bit.*

10.5.4 Functional description

The block diagram of the serial control interface is shown in *Figure 55*. It contains six dedicated registers:

- 2 control registers (SCICR1 and SCICR2)
- a status register (SCISR)
- a baud rate register (SCIBRR)
- an extended prescaler receiver register (SCIERPR)
- an extended prescaler transmitter register (SCIETPR)

Refer to the register descriptions in *Section 10.5.7* for the definitions of each bit.

Serial data format

Word length may be selected as being either 8 or 9 bits by programming the M bit in the SCICR1 register (see *Figure 55*).

The TDO pin is in low state during the start bit.

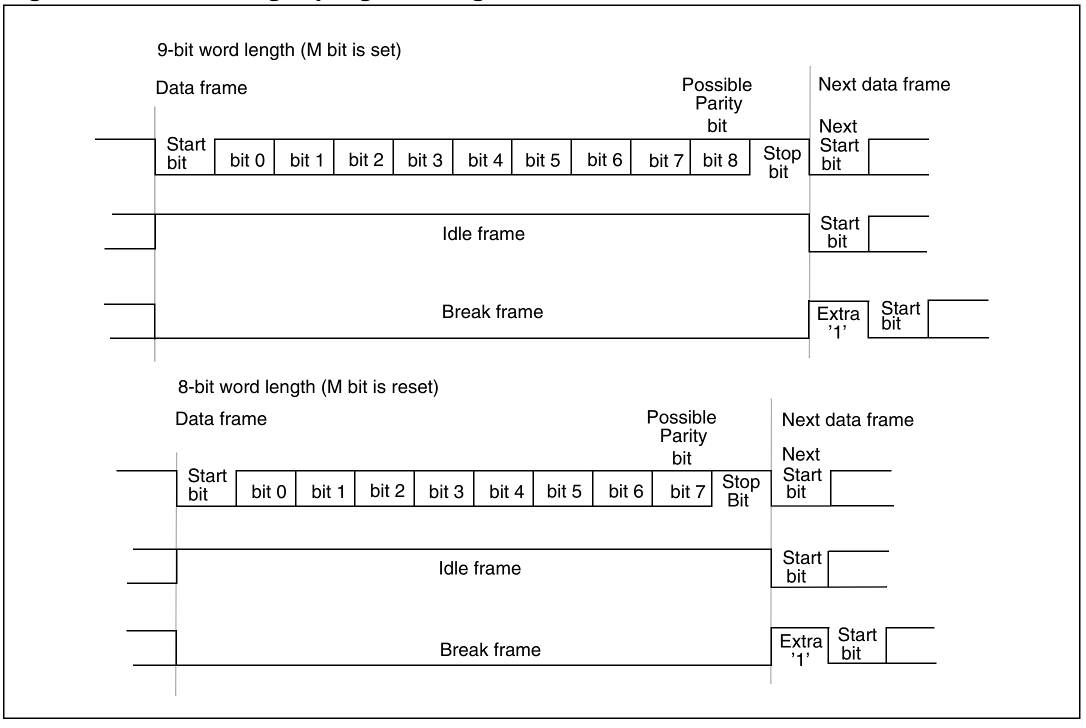
The TDO pin is in high state during the stop bit.

An Idle character is interpreted as an entire frame of '1's followed by the start bit of the next frame which contains data.

A Break character is interpreted on receiving '0's for some multiple of the frame period. At the end of the last break frame the transmitter inserts an extra '1' bit to acknowledge the start bit.

Transmission and reception are driven by their own baud rate generator.

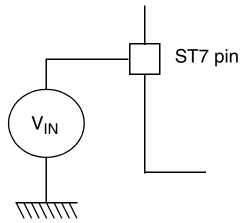
Figure 56. Word length programming



12.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 61*.

Figure 61. Pin input voltage



12.2 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

12.2.1 Voltage characteristics

Table 83. Voltage characteristics

Symbol	Ratings	Maximum value	Unit
V_{DD} - V_{SS}	Supply voltage	6.5	V
V_{PP} - V_{SS}	Programming voltage	13	
V_{IN}(1)(2)	Input voltage on true open drain pin	V_{SS} - 0.3 to 6.5	
	Input voltage on any other pin	V_{SS} - 0.3 to V_{DD} + 0.3	
$\lvert\Delta V_{DDx}\rvert$ and $\lvert\Delta V_{SSx}\rvert$	Variations between different digital power pins	50	mV
$\lvert V_{SSA}$ - $V_{SSx}\rvert$	Variations between digital and analog ground pins	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 12.8.3 on page 160*	
$V_{ESD(MM)}$	Electrostatic discharge voltage (machine model)		

1. Directly connecting the $\overline{RESET}$ and I/O pins to V_{DD} or V_{SS} could damage the device if an unintentional internal reset is generated or an unexpected change of the I/O configuration occurs (for example, due to a corrupted program counter). To guarantee safe operation, this connection has to be done through a pull-up or pull-down resistor (typical: 4.7kΩ for $\overline{RESET}$, 10kΩ for I/Os). For the same reason, unused I/O pins must not be directly tied to V_{DD} or V_{SS}.

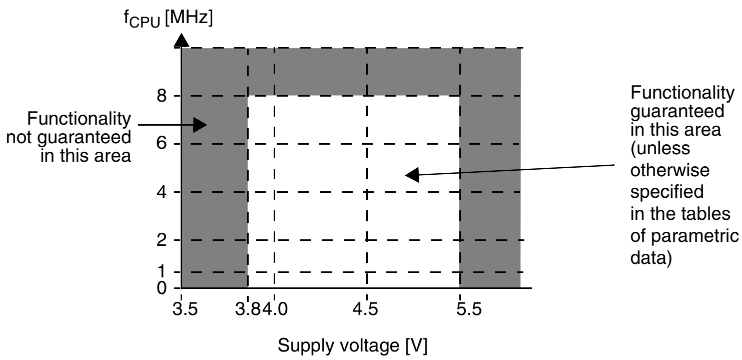
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly ensured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected.

12.3 Operating conditions

Table 86. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CPU}	Internal clock frequency		0	8	MHz
V_{DD}	Operating voltage (except Flash Write/Erase)		3.8	5.5	V
	Operating Voltage for Flash Write/Erase	V_{PP} = 11.4 to 12.6V	4.5	5.5	
T_A	Ambient temperature range	A-suffix versions	-40	85	°C
		B-suffix versions		105	
		C-suffix version		125	
		D-suffix version		150	

Figure 62. f_{CPU} max versus V_{DD}



Note: Some temperature ranges are only available with a specific package and memory size. Refer to Section 14: Device configuration and ordering information.

Warning: Do not connect 12V to V_{PP} before V_{DD} is powered on, as this may damage the device.

12.5 Supply current characteristics

The following current consumption specified for the ST7 functional operating modes over temperature range does not take into account the clock source current consumption. To obtain the total device consumption, the two current values must be added (except for Halt mode for which the clock is stopped).

12.5.1 ROM current consumption

Table 89. ROM current consumption

Symbol	Parameter	Conditions	32K ROM devices		16K/8K ROM devices		Unit
			Typ	Max(1)	Typ	Max(1)	
I_{DD}	Supply current in Run mode(2)	f_{OSC} = 2 MHz, f_{CPU} = 1 MHz f_{OSC} = 4 MHz, f_{CPU} = 2 MHz f_{OSC} = 8 MHz, f_{CPU} = 4 MHz f_{OSC} = 16 MHz, f_{CPU} = 8 MHz	0.55 1.10 2.20 4.38	0.87 1.75 3.5 7.0	0.46 0.93 1.9 3.7	0.69 1.4 2.7 5.5	mA
	Supply current in Slow mode(2)	f_{OSC} = 2 MHz, f_{CPU} = 62.5 kHz f_{OSC} = 4 MHz, f_{CPU} = 125 kHz f_{OSC} = 8 MHz, f_{CPU} = 250 kHz f_{OSC} = 16 MHz, f_{CPU} = 500 kHz	53 100 194 380	87 175 350 700	30 70 150 310	60 120 250 500	µA
	Supply current in Wait mode(2)	f_{OSC} = 2 MHz, f_{CPU} = 1 MHz f_{OSC} = 4 MHz, f_{CPU} = 2 MHz f_{OSC} = 8 MHz, f_{CPU} = 4 MHz f_{OSC} = 16 MHz, f_{CPU} = 8 MHz	0.31 0.61 1.22 2.44	0.5 1.0 2.0 4.0	0.22 0.45 0.91 1.82	0.37 0.75 1.5 3	mA
	Supply current in Slow Wait mode(2)	f_{OSC} = 2 MHz, f_{CPU} = 62.5 kHz f_{OSC} = 4 MHz, f_{CPU} = 125 kHz f_{OSC} = 8 MHz, f_{CPU} = 250 kHz f_{OSC} = 16 MHz, f_{CPU} = 500 kHz	36 69 133 260	63 125 250 500	20 40 90 190	40 90 180 350	µA
	Supply current in Halt mode(3)	$-40°C \leq T_A \leq +85°C$	<1	10	<1	10	
		$-40°C \leq T_A \leq +125°C$	<1	50	<1	50	
	Supply current in Active Halt mode(4)	f_{OSC} = 2 MHz f_{OSC} = 4 MHz f_{OSC} = 8 MHz f_{OSC} = 16 MHz	15 28 55 107	20 38 75 200	11 22 43 85	15 30 60 150	

1. Data based on characterization results, tested in production at V_{DD} max. and f_{CPU} max.
2. Measurements are done in the following conditions:
   - Program executed from RAM, CPU running with RAM access. The increase in consumption when executing from Flash is 50%.
   - All I/O pins in input mode with a static value at V_{DD} or V_{SS} (no load)
   - All peripherals in reset state
   - LVD disabled.
   - Clock input (OSC1) driven by external square wave
   - In Slow and Slow Wait modes, f_{CPU} is based on f_{OSC} divided by 32
   To obtain the total current consumption of the device, add the clock source (*Section 12.6.3*) and the peripheral power consumption (*Section 12.5.4*).
3. All I/O pins in push-pull 0 mode (when applicable) with a static value at V_{DD} or V_{SS} (no load), LVD disabled. Data based on characterization results, tested in production at V_{DD} max. and f_{CPU} max.
4. Data based on characterization results, not tested in production. All I/O pins in push-pull 0 mode (when applicable) with a static value at V_{DD} or V_{SS} (no load); clock input (OSC1) driven by external square wave, LVD disabled. To obtain the total current consumption of the device, add the clock source consumption (*Section 12.6.3*).

12.6.3 Crystal and ceramic resonator oscillators

The ST7 internal clock can be supplied with four different crystal/ceramic resonator oscillators. All the information given in this paragraph are based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and start-up stabilization time. Refer to the crystal/ceramic resonator manufacturer for more details (frequency, package, accuracy...).

Table 95. Crystal and ceramic resonator oscillators

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC}	Oscillator frequency(1)	LP: low power oscillator MP: medium power oscillator MS: medium speed oscillator HS: high speed oscillator	1 >2 >4 >8		2 4 8 16	MHz
R_F	Feedback resistor(2)		20		40	kΩ
C_{L1} C_{L2}	Recommended load capacitance versus equivalent serial resistance of the crystal or ceramic resonator (R_S)(3)	R_S = 200Ω LP oscillator R_S = 200Ω MP oscillator R_S = 200Ω MS oscillator R_S = 100Ω HS oscillator	22 22 18 15		56 46 33 33	pF
i_2	OSC2 driving current	V_{DD} = 5V, V_{IN} = V_{SS} LP oscillator MP oscillator MS oscillator HS oscillator		 80 160 310 610	 150 250 460 910	µA

1. The oscillator selection can be optimized in terms of supply current using an high quality resonator with small R_S value. Refer to crystal/ceramic resonator manufacturer for more details.
2. Data based on characterization results, not tested in production. The relatively low value of the RF resistor, offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the microcontroller is used in tough humidity conditions.
3. For C_{L1} and C_{L2} it is recommended to use high-quality ceramic capacitors in the 5pF to 25pF range (typ.) designed for high-frequency applications and selected to match the requirements of the crystal or resonator. C_{L1} and C_{L2}, are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included when sizing C_{L1} and C_{L2} (10 pF can be used as a rough estimate of the combined pin and board capacitance).

Figure 64. Typical application with a crystal or ceramic resonator (8/16 Kbyte Flash and ROM devices)

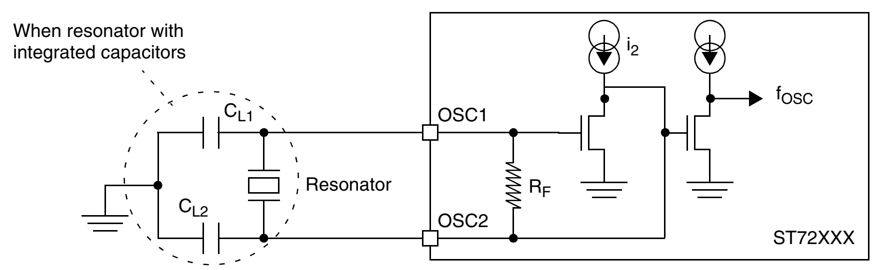
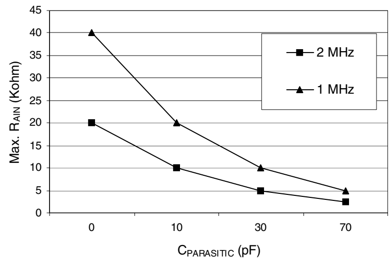


Table 111. 10-bit ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{ADC}	Conversion time (Sample + Hold) f_{CPU} = 8 MHz, Speed = 0, f_{ADC} = 2 MHz			7.5		µs
	No. of sample capacitor loading cycles No. of Hold conversion cycles			4 11		$1/f_{ADC}$

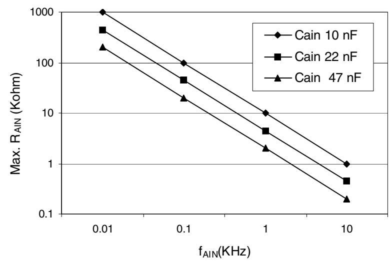
1. Any added external serial resistor will downgrade the ADC accuracy (especially for resistance greater than 10kΩ). Data based on characterization results, not tested in production.
2. Injecting negative current on adjacent pins may result in increased leakage currents. Software filtering of the converted analog value is recommended.

Figure 82. R_{AIN} max. vs f_{ADC} with C_{AIN} = 0pF(1)



1. $C_{PARASITIC}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (3pF). A high $C_{PARASITIC}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

Figure 83. Recommended C_{AIN} and R_{AIN} values(1)



1. This graph shows that, depending on the input signal variation (f_{AIN}), C_{AIN} can be increased for stabilization time and decreased to allow the use of a larger serial resistor (R_{AIN}).

Figure 84. Typical A/D converter application

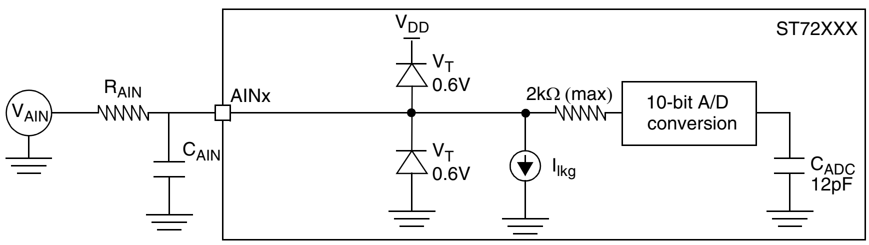


Table 113. 44-pin low profile quad flat package mechanical data

Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
Number of pins						
N	44					

13.2 LQFP32 package characteristics

Figure 88. 32-pin low profile quad flat package outline

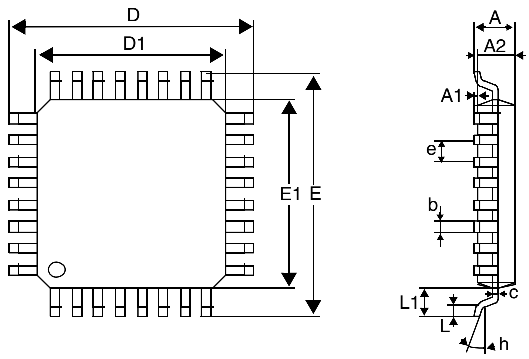


Table 114. 32-pin low profile quad flat package mechanical data

Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.30	0.37	0.45	0.012	0.015	0.018
C	0.09		0.20	0.004		0.008
D		9.00			0.354	
D1		7.00			0.276	
E		9.00			0.354	
E1		7.00			0.276	
e		0.80			0.031	
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.018	0.024	0.030