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Details

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Program Memory Type	-
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Voltage - Supply (Vcc/Vdd)	-
Data Converters	-
Oscillator Type	-
Operating Temperature	-
Mounting Type	-
Package / Case	-
Supplier Device Package	-
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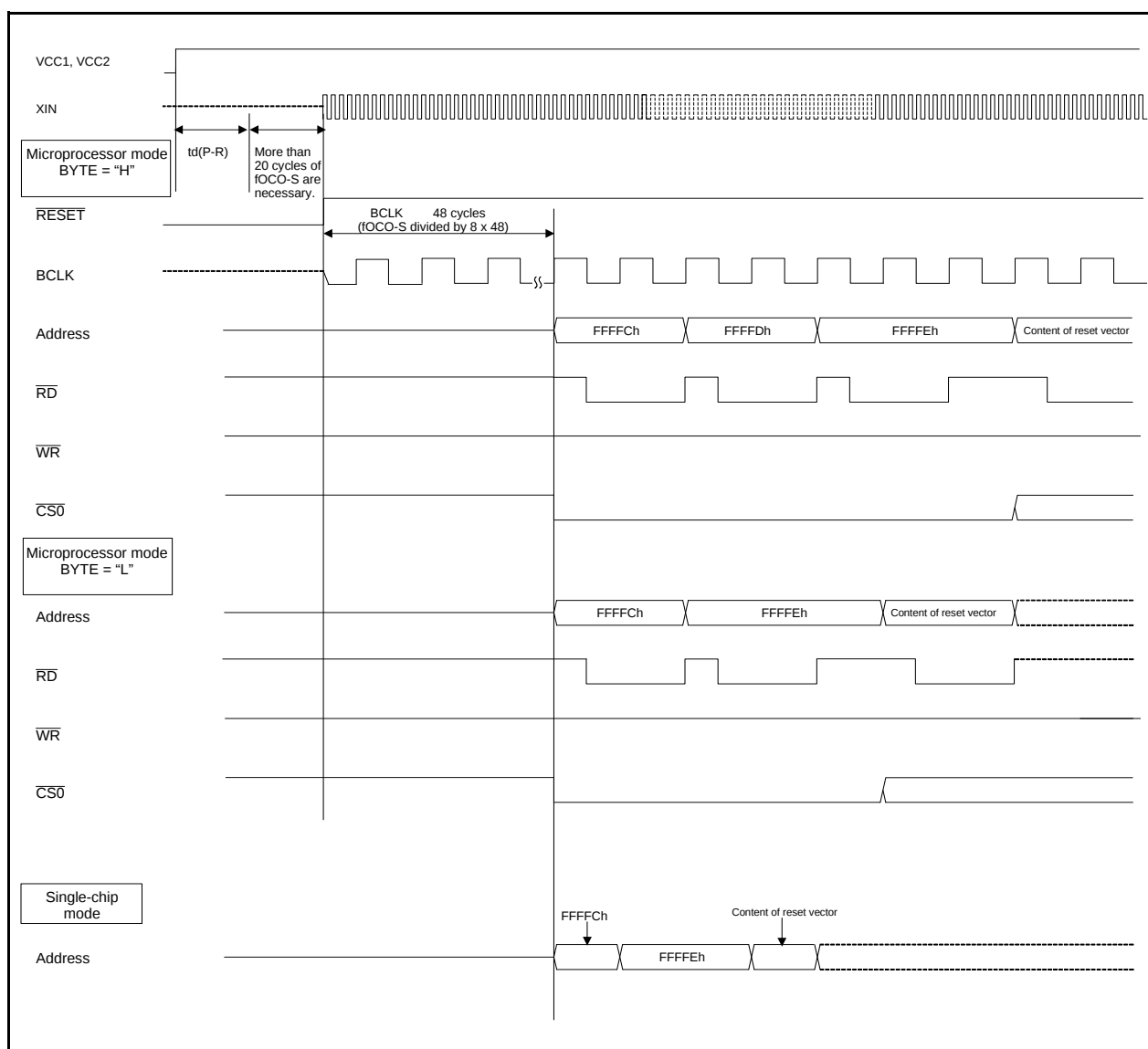


Figure 5.2 Reset Sequence

5.2 Brown-out Reset

The microcomputer resets pins, the CPU, or SFRs by setting the built-in voltage detection 0 circuit. The voltage detection 0 circuit monitors the voltage applied to the VCC1 pin (Vdet0).

The microcomputer resets pins, the CPU, and SFR as soon as the voltage that is applied to the VCC1 pin drops to Vdet0 or below.

Then, 125 kHz on-chip oscillator clock starts counting when the voltage that is applied to the VCC1 pin goes up to Vdet0 or above. The internal reset signal becomes "H" after the 125 kHz on-chip oscillator clock is counted 32 times, and then reset sequence starts (see Figure 5.2). The 125 kHz on-chip oscillator clock divided by 8 is automatically selected as a CPU clock after reset.

Refer to 4. **"Special Function Registers (SFRs)"** for the SFR status after brown-out reset.

The internal RAM is not reset. When the voltage that is applied to the VCC1 pin drops to Vdet0 or below while writing data to the internal RAM, the internal RAM is in an indeterminate state.

Refer to 6. **"Voltage Detection Circuit"** for details of the voltage detection 0 circuit.

5.3 Software Reset

The microcomputer resets pins, the CPU, and SFRs when the PM03 bit in the PM0 register is set to 1 (microcomputer reset). Then the microcomputer executes the program in an address determined by the reset vector. The 125 kHz on-chip oscillator clock divided by 8 is automatically selected as a CPU clock after reset.

In the software reset, the microcomputer does not reset a part of the SFRs. Refer to 4. **"Special Function Registers (SFRs)"** for details.

The internal RAM is not reset.

5.4 Watchdog Timer Reset

The microcomputer resets pins, the CPU, and SFRs when the PM12 bit in the PM1 register is set to 1 (reset when watchdog timer underflows) and the watchdog timer underflows. Then the microcomputer executes the program in an address determined by the reset vector. The 125 kHz on-chip oscillator clock divided by 8 is automatically selected as a CPU clock after reset.

In the watchdog timer reset, the microcomputer does not reset a part of the SFRs. Refer to 4. **"Special Function Registers (SFRs)"** for details.

The internal RAM is not reset. When the watchdog timer underflows while writing data to the internal RAM, the internal RAM is in an indeterminate state.

Refer to 13. **"Watchdog Timer"** for details.

5.5 Oscillation Stop Detection Reset

The microcomputer resets and stops pins, the CPU, and SFRs when the CM27 bit in the CM2 register is 0 (reset when oscillation stop detected), if it detects main clock oscillation circuit stop. Refer to 10.6 **"Oscillation Stop and Re-Oscillation Detect Function"** for details.

In the oscillation stop detection reset, the microcomputer does not reset a part of the SFRs. Refer to 4. **"Special Function Registers (SFRs)"** for details. Processor mode remains unchanged since bits PM01 to PM00 in the PM0 register are not reset.

6.5 Cold Start-up / Warm Start-up Discrimination

As for the cold start-up / warm start-up discrimination, the CWR bit in the RSTFR register determines either cold start-up (reset process) when power-on or warm start-up (reset process) when reset signal is applied during the microcomputer running.

The value of the CWR bit is 0 when power is applied. The CWR bit is also set to 0 after brown-out reset. The CWR bit is set to 1 by writing a 1 in a program and does not change at hardware reset 1, software reset, watchdog timer reset, and oscillation stop detection reset.

Use brown-out reset for cold start-up / warm start-up discrimination.

Follow Table 6.1 Setting Procedures of the Bits for Brown-out Reset to set the bits for brown-out reset.

Figure 6.9 shows Cold Start-up / Warm Start-up Discrimination Example. Figure 6.10 shows RSTFR Register.

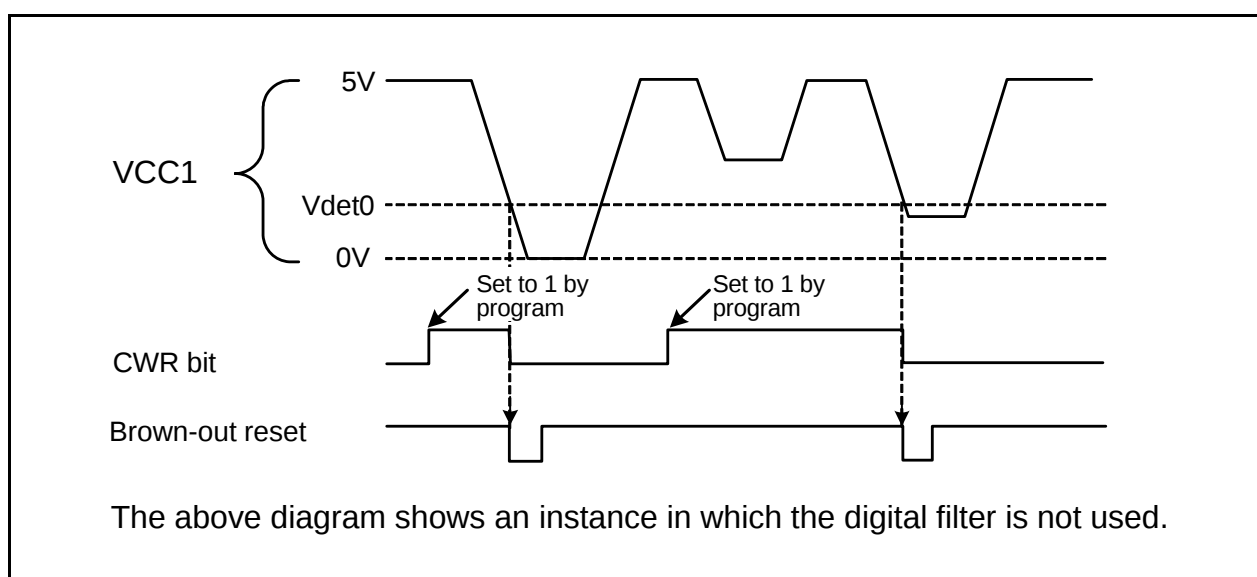


Figure 6.9 Cold Start-up / Warm Start-up Discrimination Example

7. Processor Mode

7.1 Types of Processor Mode

Three processor modes are available to choose from: single-chip mode, memory expansion mode, and microprocessor mode. Table 7.1 shows the Features of Processor Modes.

Table 7.1 Features of Processor Modes

Processor Modes	Access Space	Pins Which Are Assigned I/O Ports
Single-chip mode	SFR, internal RAM, internal ROM	All pins are I/O ports or peripheral function I/O pins
Memory expansion mode	SFR, internal RAM, internal ROM, external area ⁽¹⁾	Some pins serve as bus control pins ⁽¹⁾
Microprocessor mode	SFR, internal RAM, external area ⁽¹⁾	Some pins serve as bus control pins ⁽¹⁾

Note:

1. Refer to 8. “Bus” for details.

7.2 Setting Processor Modes

Processor mode is set by using the CNVSS pin and bits PM01 to PM00 in the PM0 register.

Table 7.2 shows the Processor Mode After Hardware Reset. Table 7.3 shows Bits PM01 to PM00 Set Values and Processor Modes

Table 7.2 Processor Mode After Hardware Reset

CNVSS Pin Input Level	Processor Modes
VSS	Single-chip mode
VCC1 ^(1, 2)	Microprocessor mode

Notes:

1. If the microcomputer is reset in hardware by applying VCC1 to the CNVSS pin (hardware reset 1 or brown-out reset), the internal ROM cannot be accessed regardless of the status of bits PM10 to PM00.
2. The multiplexed bus cannot be assigned to the entire $\overline{CS}$ space.

Table 7.3 Bits PM01 to PM00 Set Values and Processor Modes

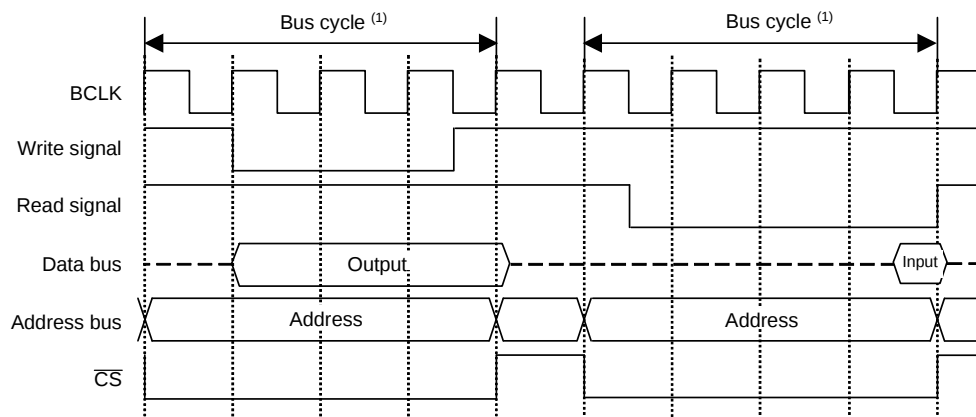
Bits PM01 to PM00	Processor Modes
00b	Single-chip mode
01b	Memory expansion mode
10b	Do not set
11b	Microprocessor mode

Rewriting bits PM01 to PM00 places the microcomputer in the corresponding processor mode regardless of whether the input level on the CNVSS pin is “H” or “L”. Note, however, that bits PM01 to PM00 cannot be rewritten to 01b (memory expansion mode) or 11b (microprocessor mode) at the same time bits PM07 to PM02 are rewritten. Note also that these bits cannot be rewritten to enter microprocessor mode in the internal ROM, nor can they be rewritten to exit microprocessor mode in areas overlapping the internal ROM.

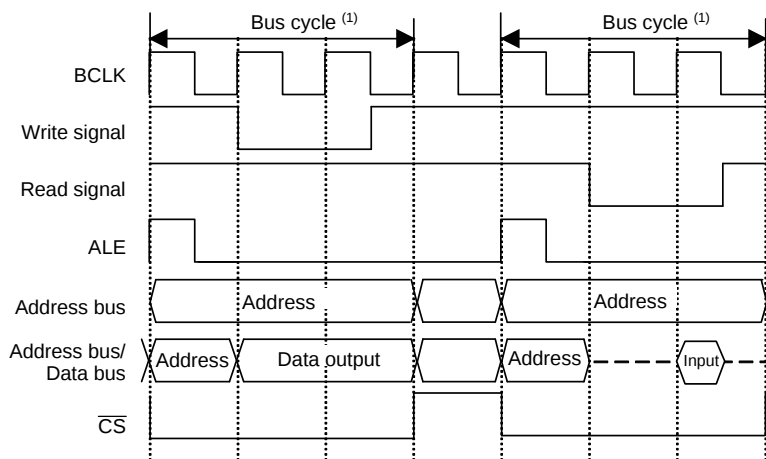
If the microcomputer is reset in hardware by applying VCC1 to the CNVSS pin (hardware reset 1 or brown-out reset), the internal ROM cannot be accessed regardless of bits PM01 to PM00.

Figures 7.1 to 7.3 show the PM0 Register and PM1 Register.

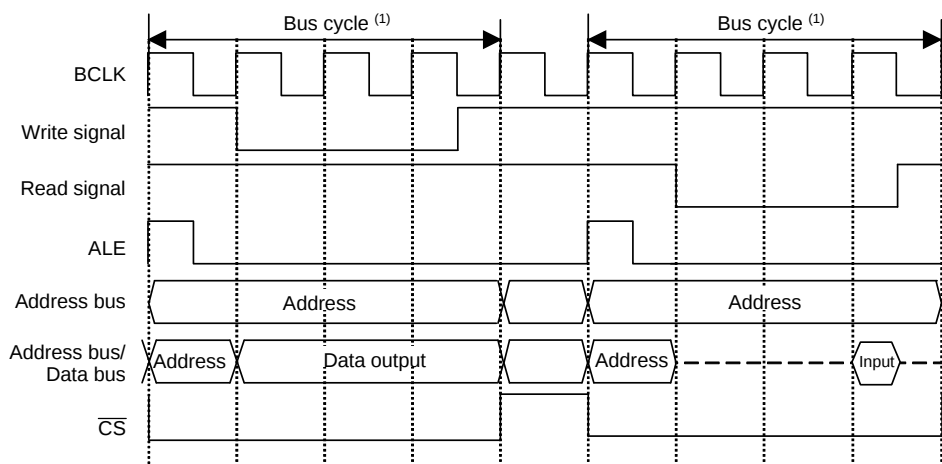
(1) Separate Bus, 3-Wait Setting



(2) Multiplexed Bus, 1- or 2-Wait Setting



(3) Multiplexed Bus, 3-Wait Setting



Note :

1. These example timing charts indicate bus cycle length. After this bus cycle sometimes come read and write cycles in succession.

Figure 8.8 Typical Bus Timings Using Software Wait (2)

9. Memory Space Expansion Function

The following describes a memory space expansion function.

During memory expansion or microprocessor mode, the memory space expansion function allows the access space to be expanded using the appropriate register bits.

Table 9.1 shows Setting of Memory Space Expansion Function, Memory Space.

Table 9.1 Setting of Memory Space Expansion Function, Memory Space

Memory Space Expansion Function	Setting (PM15 to PM14)	Memory Space
1-Mbyte Mode	00b	1 Mbyte (no expansion)
4-Mbyte Mode	11b	4 Mbytes

9.1 1-Mbyte Mode

In this mode, the memory space is 1 Mbyte. In 1-Mbyte mode, the external area to be accessed is specified using the $\overline{CSi}$ ($i = 0$ to 3) signals (hereafter referred to as the $\overline{CSi}$ area). Figures 9.2 and 9.3 show the Memory Mapping and $\overline{CS}$ Area in 1-Mbyte mode.

9.2 4-Mbyte Mode

In this mode, the memory space is 4 Mbytes. Figure 9.1 shows the DBR Register. Bits BSR2 to BSR0 in the DBR register select a bank number which is to be accessed to read or write data. Setting the OFS bit to 1 (with offset) allows the accessed address to be offset by 40000h.

In 4-Mbyte mode, the $\overline{CSi}$ ($i = 0$ to 3) pin function differs depending on an area to be accessed.

9.2.1 Addresses 04000h to 3FFFFh, C0000h to FFFFFh

- The $\overline{CSi}$ signal is output from the $\overline{CSi}$ pin (same operation as 1-Mbyte mode; however, the last address of the $\overline{CS1}$ area is 3FFFFh).

9.2.2 Addresses 40000h to BFFFFh

- The $\overline{CS0}$ pin outputs "L"
- Pins $\overline{CS1}$ to $\overline{CS3}$ output the setting values of bits BSR2 to BSR0 (bank number)

Figures 9.4 and 9.5 show the Memory Mapping and $\overline{CS}$ Area in 4-Mbyte mode. Note that banks 0 to 6 are data-only areas. Locate the program in bank 7 or the $\overline{CSi}$ area.

10.1.2 Sub Clock

The sub clock is generated by the sub clock oscillation circuit. This clock is used as the clock source for the CPU clock, as well as the timer A and timer B count sources. In addition, an fC clock with the same frequency as that of the sub clock can be output from the CLKOUT pin.

The sub clock oscillation circuit is configured by connecting a crystal resonator between pins XCIN and XCOU. The sub clock oscillation circuit contains a feedback resistor, which is disconnected from the oscillation circuit during stop mode in order to reduce the amount of power consumed in the chip. The sub clock oscillation circuit may also be configured by feeding an externally generated clock to the XCIN pin.

Figure 10.8 shows the Examples of Sub Clock Connection Circuit.

After reset, the sub clock is turned off. At this time, the feedback resistor is disconnected from the oscillation circuit.

To use the sub clock for the CPU clock, set the CM07 bit in the CM0 register to 1 (sub clock) after the sub clock becomes oscillating stably.

During stop mode, all clocks including the sub clock are turned off. Refer to **10.4 “Power Control”** for details.

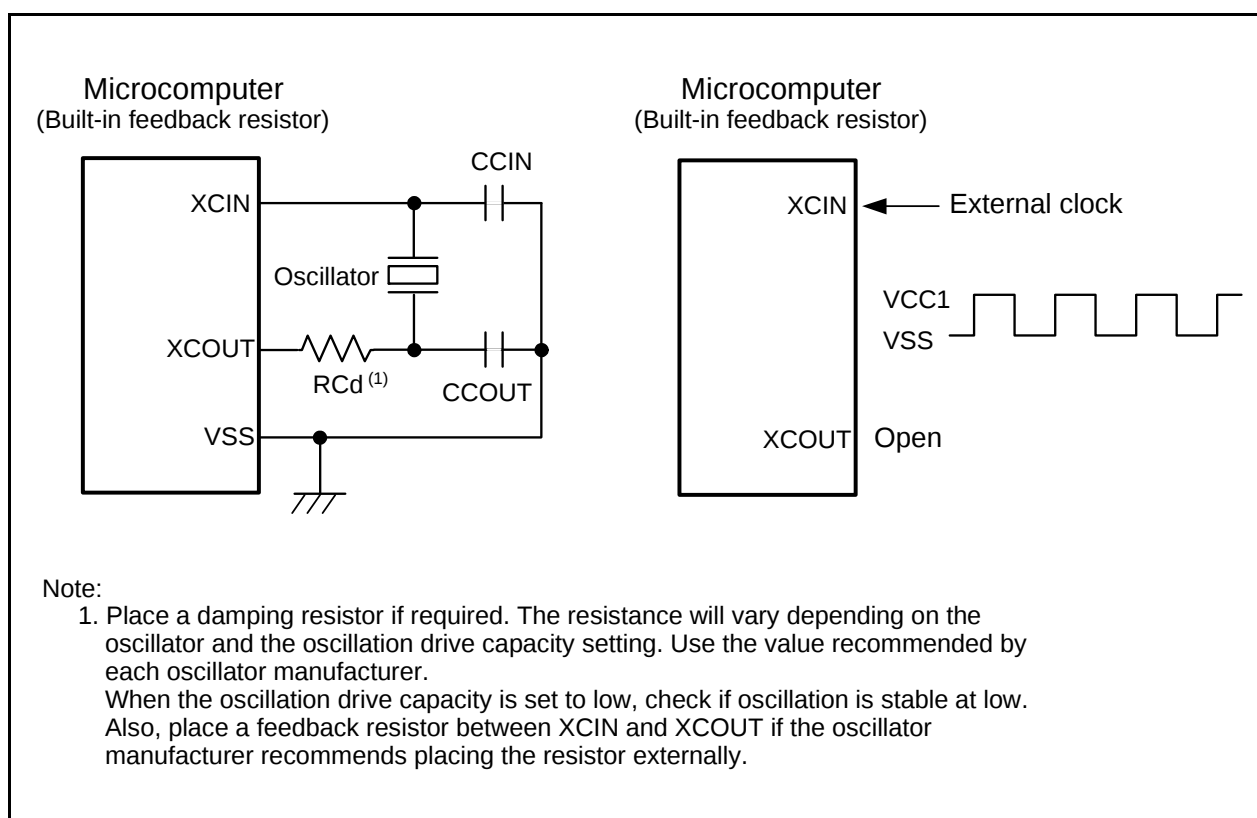


Figure 10.8 Examples of Sub Clock Connection Circuit

10.1.3 125 kHz On-Chip Oscillator Clock (fOCO-S)

This clock, approximately 125 kHz, is supplied by 125 kHz on-chip oscillator. This clock is used as the clock source for the CPU and peripheral function clocks. In addition, if the CSPRO bit in the CSPR register is 1 (count source protection mode enabled), this clock is used as the count source for the watchdog timer (Refer to **13.2 “Count Source Protection Mode Enabled”**).

After reset, the 125 kHz on-chip oscillator divided by 8 provides the CPU clock. It stops when the CM14 bit in the CM1 register is set to 0 (125 kHz on-chip oscillator stops). If the main clock stops oscillating when the CM20 bit in the CM2 register is 1 (oscillation stop, re-oscillation detection function enabled) and the CM27 bit is 1 (oscillation stop, re-oscillation detection interrupt), the 125 kHz on-chip oscillator automatically starts operating and supplying the necessary clock for the microcomputer.

10.1.4 PLL Clock

The PLL clock is generated by the PLL frequency synthesizer. This clock is used as the clock source for the CPU and peripheral function clocks. After reset, the PLL frequency synthesizer is turned off. The PLL frequency synthesizer is activated by setting the PLC07 bit to 1 (PLL operation). When the PLL clock is used as the clock source for the CPU clock, wait for t_{su} (PLL) until the PLL clock to be stable, and then set the CM11 bit in the CM1 register to 1.

Before entering wait mode or stop mode, be sure to set the CM11 bit to 0 (CPU clock source is the main clock). Furthermore, before entering stop mode, be sure to set the PLC07 bit in the PLC0 register to 0 (PLL stops). Figure 10.10 shows the Procedure to Use PLL Clock as CPU Clock Source.

The PLL clock is the main clock divided by the selected values of bits PLC05 and PLC04 in the PLC0 register, and then multiplied by the selected values of bits PLC02 to PLC00. Set bits PLC05 and PLC04 to fit divided frequency between 2 MHz and 5 MHz. Figure 10.9 shows the Relation between the Main Clock and the PLL Clock.

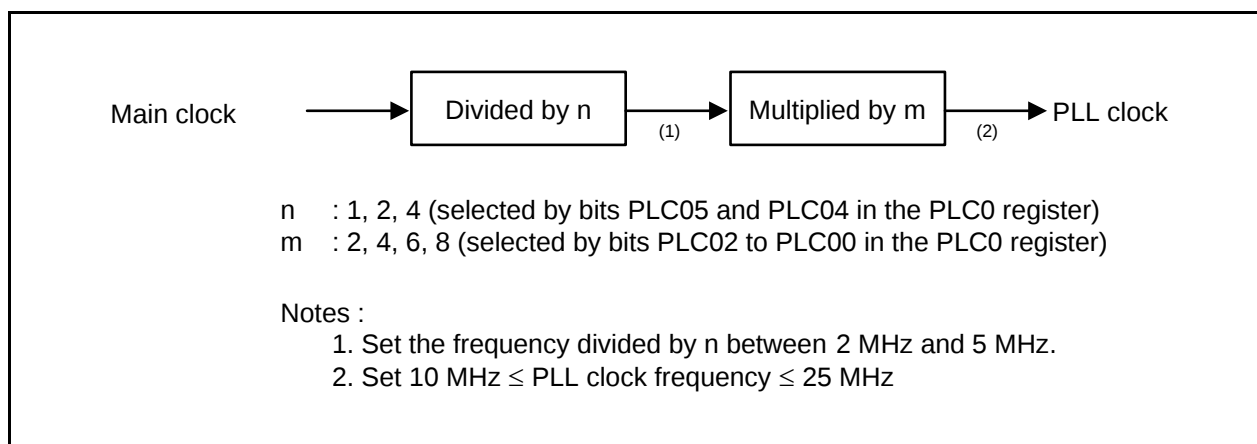


Figure 10.9 Relation between the Main Clock and the PLL Clock

10.4.2 Wait Mode

In wait mode, the CPU clock is turned off, so are the CPU and the watchdog timer because they are operated by the CPU clock. However, if the CSPRO bit in the CSPR register is 1 (count source protection enabled), the watchdog timer remains active. Because the main clock, sub clock, and 125 kHz on-chip oscillator clock all are on, the peripheral functions using these clocks keep operating.

10.4.2.1 Peripheral Function Clock Stop Function

If the CM02 bit in the CM0 register is 1 (peripheral function clock f1 turned off during wait mode), the f1 clock is turned off while in wait mode, with the power consumption reduced that much. However, fC32 and fOCO-S (clock source of Timers A and B) remain on for the CM02 bit.

10.4.2.2 Entering Wait Mode

The microcomputer is placed into wait mode by executing the WAIT instruction.

When the CM11 bit = 1 (CPU clock source is the PLL clock), be sure to clear the CM11 bit in the CM1 register to 0 (CPU clock source is the main clock) before going to wait mode. The power consumption of the chip can be reduced by clearing the PLC07 bit in the PLC0 register to 0 (PLL stops).

10.4.2.3 Pin Status during Wait Mode

Table 10.4 lists Pin Status during Wait Mode.

Table 10.4 Pin Status during Wait Mode

Pin		Memory Expansion Mode Microprocessor Mode	Single-Chip Mode
A0 to A19, D0 to D15, CS0 to CS3, BHE		Retains status just prior to entering wait mode	Cannot be used as a bus control pin
RD, WR, WRL, WRH		"H"	
HLDA, BCLK		"H"	
ALE		"L"	
I/O ports		Retains status just prior to entering wait mode	Retains status before wait mode
CLKOUT	When fC selected	Cannot be used as a CLKOUT pin	Does not stop
	When f8, f32 selected		Does not stop when the CM02 bit is 0. When the CM02 bit is 1, the status immediately prior to entering wait mode is maintained

12.4 Interrupts and Interrupt Vector

One interrupt vector consists of 4 bytes. Set the start address of each interrupt routine in the respective interrupt vectors. When an interrupt request is accepted, the CPU branches to the address set in the corresponding interrupt vector. Figure 12.2 shows the Interrupt Vector.

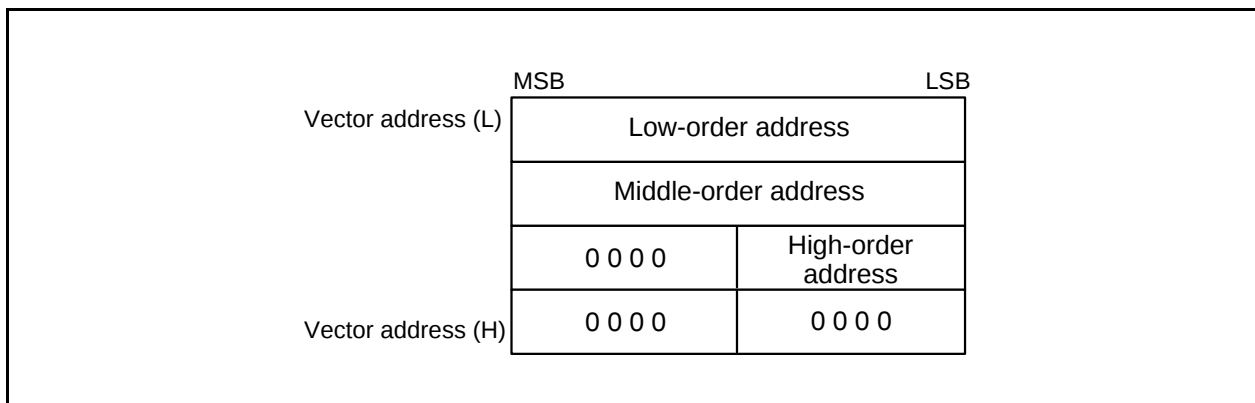


Figure 12.2 Interrupt Vector

12.4.1 Fixed Vector Tables

The fixed vector tables are allocated to the addresses from FFFDCh to FFFFFh. Table 12.1 lists the Fixed Vector Table. In the flash memory version of microcomputer, the vector addresses (H) of fixed vectors are used by the ID code check function. For details, refer to **22.2 “Functions to Prevent Flash Memory from Rewriting”**.

Table 12.1 Fixed Vector Table

Interrupt Source	Vector Table Addresses Address (L) to Address (H)	Reference
Undefined Instruction (UND instruction)	FFFDCh to FFFDFh	M16C/60, M16C/20, M16C/Tiny Series Software Manual
Overflow (INTO instruction)	FFFE0h to FFFE3h	
BRK Instruction ⁽²⁾	FFFE4h to FFFE7h	
Address Match	FFFE8h to FFEFBh	12.9 “Address Match Interrupt”
Single Step ⁽¹⁾	FFFECh to FFEFh	-
Watchdog Timer, Oscillation Stop and Re-Oscil- lation Detection, Low Voltage Detection	FFFF0h to FFFF3h	13. “Watchdog Timer” 10. “Clock Generation Circuit” 6. “Voltage Detection Circuit”
DBC ⁽¹⁾	FFFF4h to FFFF7h	-
NMI	FFFF8h to FFFFBh	12.7 “NMI Interrupt”
Reset	FFFFCh to FFFFFh	5. “Reset”

Notes:

- Do not normally use this interrupt because it is provided exclusively for use by development tools.
- If the contents of address FFFE6h is FFh, program execution starts from the address shown by the vector in the relocatable vector table.

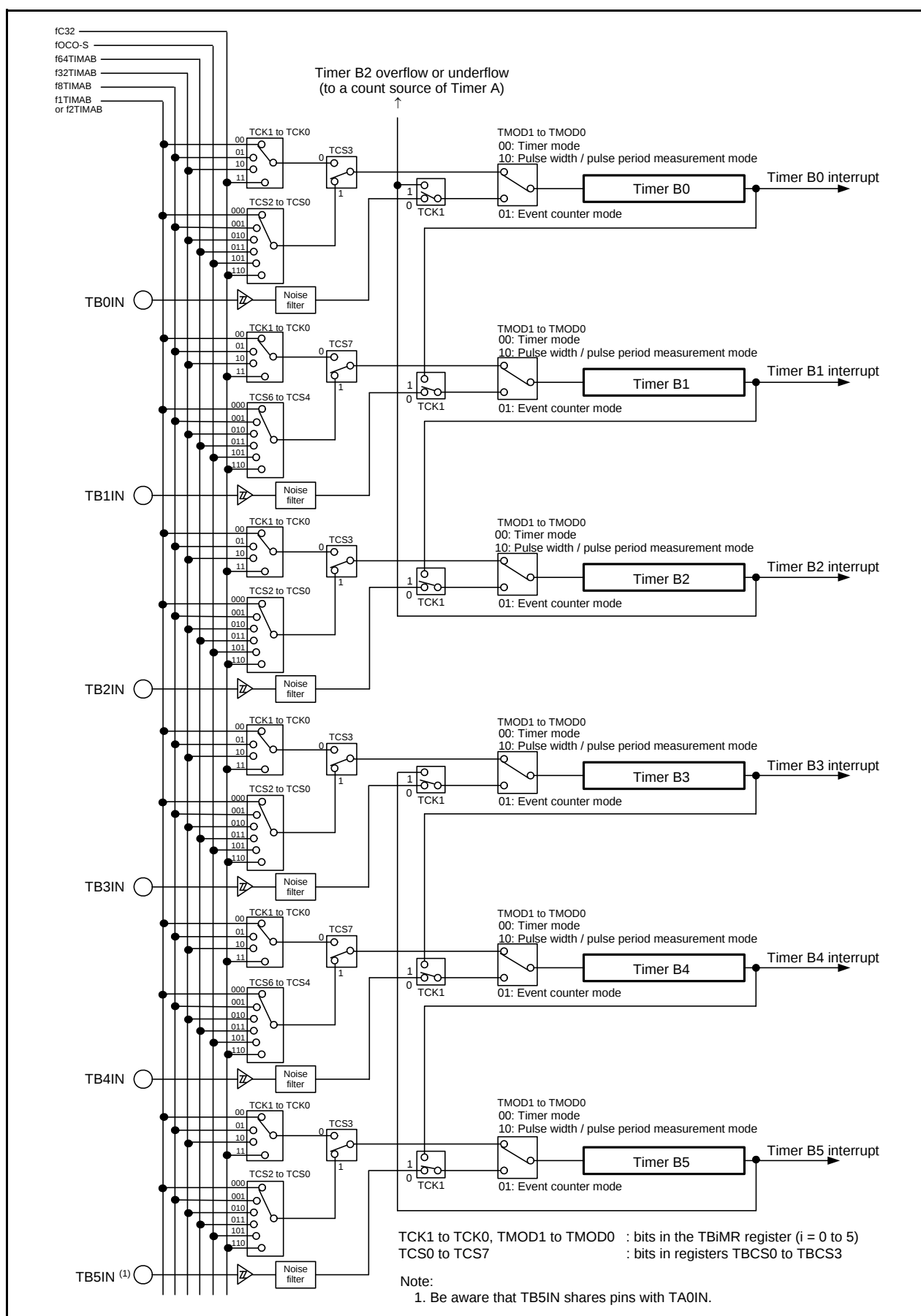


Figure 15.3 Timer B Configuration

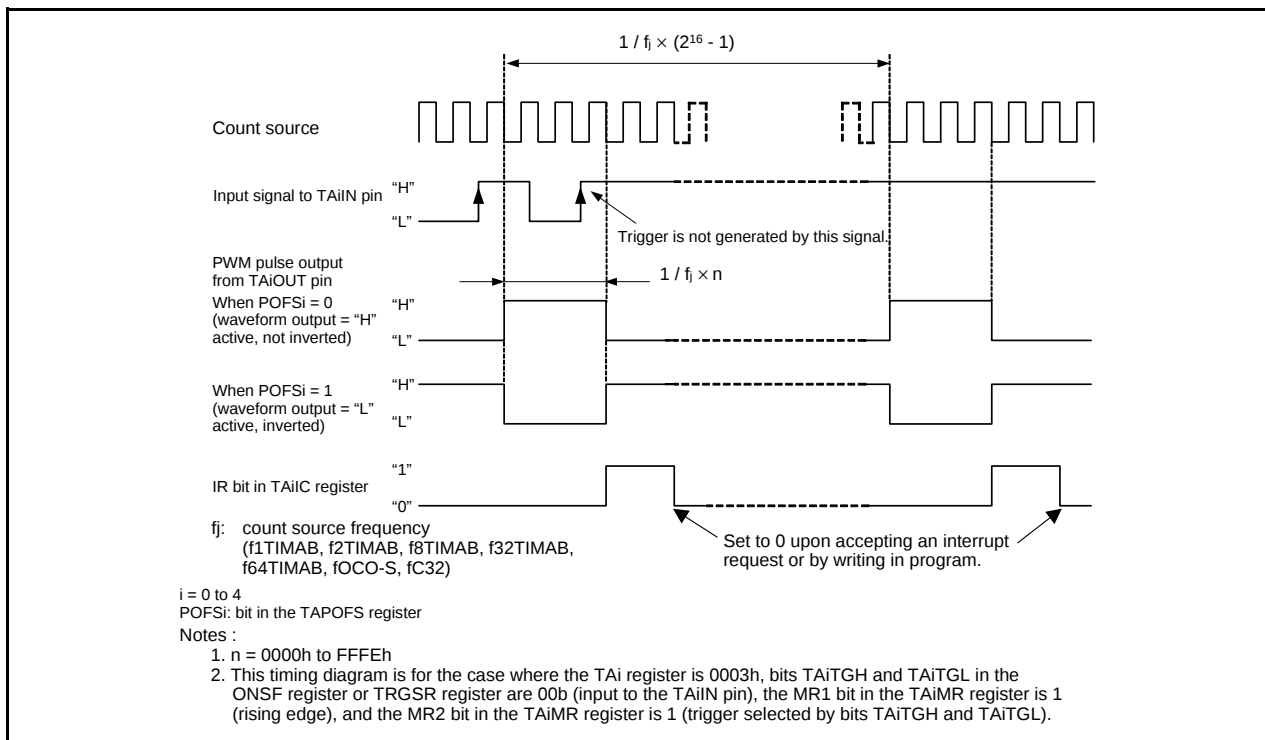


Figure 15.16 Example of 16-Bit Pulse Width Modulator Operation

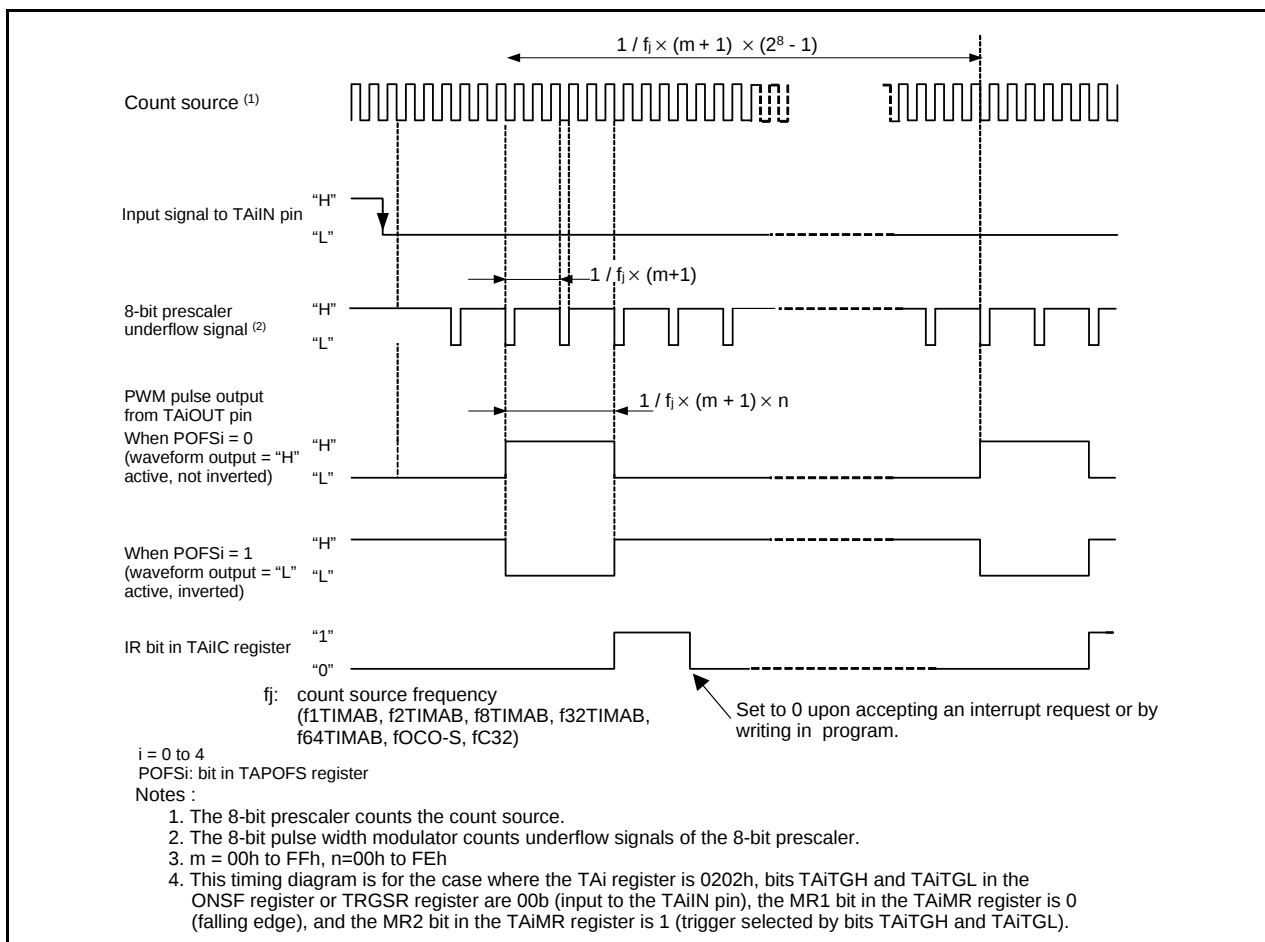
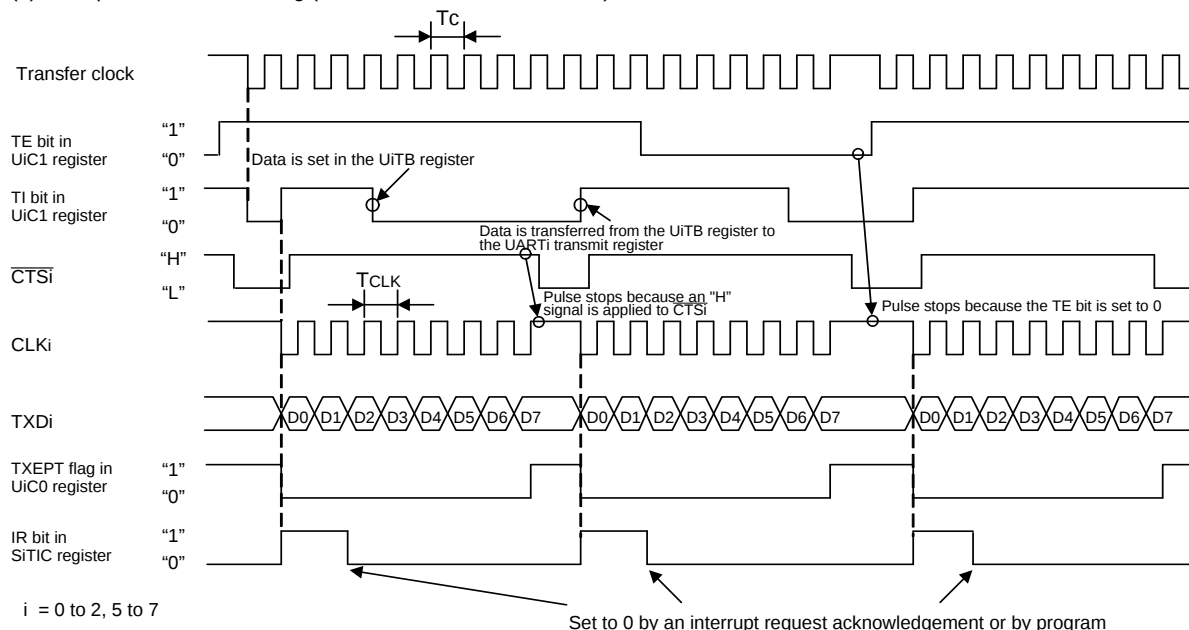


Figure 15.17 Example of 8-Bit Pulse Width Modulator Operation

(1) Example of Transmit Timing (when internal clock is selected)



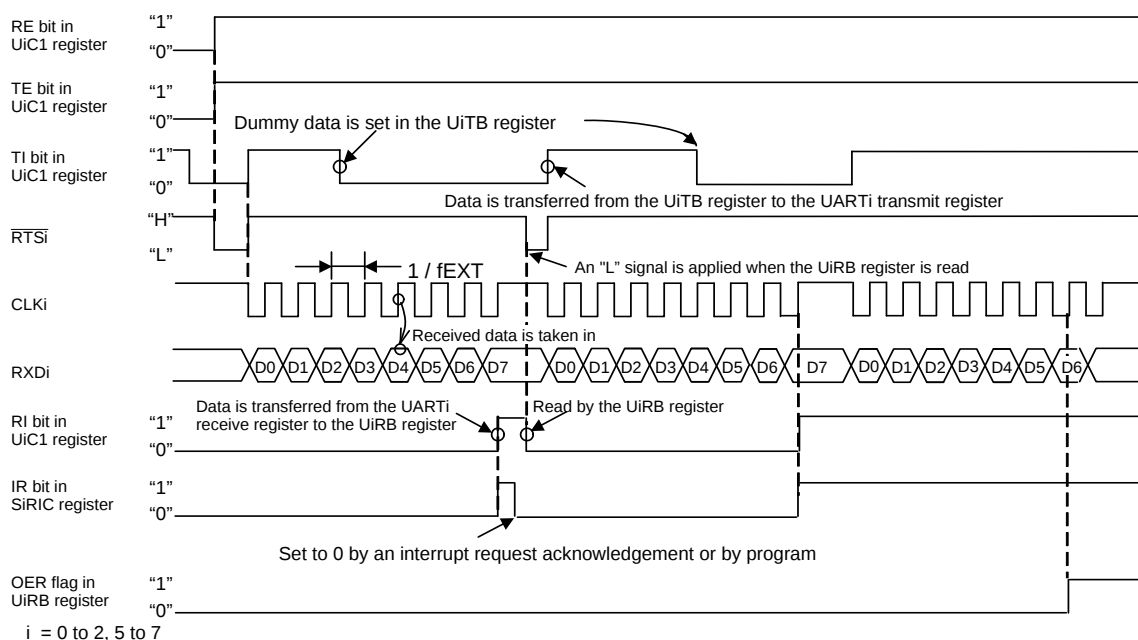
The above timing diagram applies to the case where the register bits are set as follows:

- The CKDIR bit in the UiMR register = 0 (internal clock)
- The CRD bit in the UiC0 register = 0 (CTS / RTS enabled), the CRS bit = 0 (CTS selected)
- The CKPOL bit in the UiC0 register = 0 (transmit data output at the falling edge and receive data taken in at the rising edge of the transfer clock)
- The UiIRS bit in the UiC1 register = 0 (an interrupt request occurs when the UiTB register becomes empty)

$$T_C = T_{CLK} = 2(n + 1) / f_j$$

f_j : frequency of UiBRG count source (f1SIO, f2SIO, f8SIO, f32SIO)
 n : value set to the UiBRG register

(2) Example of Receive Timing (when external clock is selected)



The above timing diagram applies to the case where the register bits are set as follows:

- The CKDIR bit in the UiMR register = 1 (external clock)
- The CRD bit in the UiC0 register = 0 (CTS / RTS enabled), the CRS bit = 1 (RTS selected)
- The CKPOL bit in the UiC0 register = 0 (transmit data output at the falling edge and receive data taken in at the rising edge of the transfer clock)

f_{EXT} : frequency of the external clock

Make sure the following conditions are met when input to the CLKi pin before receiving data is high:

- The TE bit in the UiC0 register = 1 (transmit enabled)
- The RE bit in the UiC1 register = 1 (receive enabled)
- Write dummy data to the UiTB register

Figure 17.12 Transmit and Receive Operation during Clock Synchronous Serial I/O Mode

22.3.3 Flash Memory Control Register (Registers FMR0, FMR1, FMR2 and FMR6)

Figures 22.5 to 22.8 show the registers FMR0, FMR1, FMR2 and FMR6, respectively.

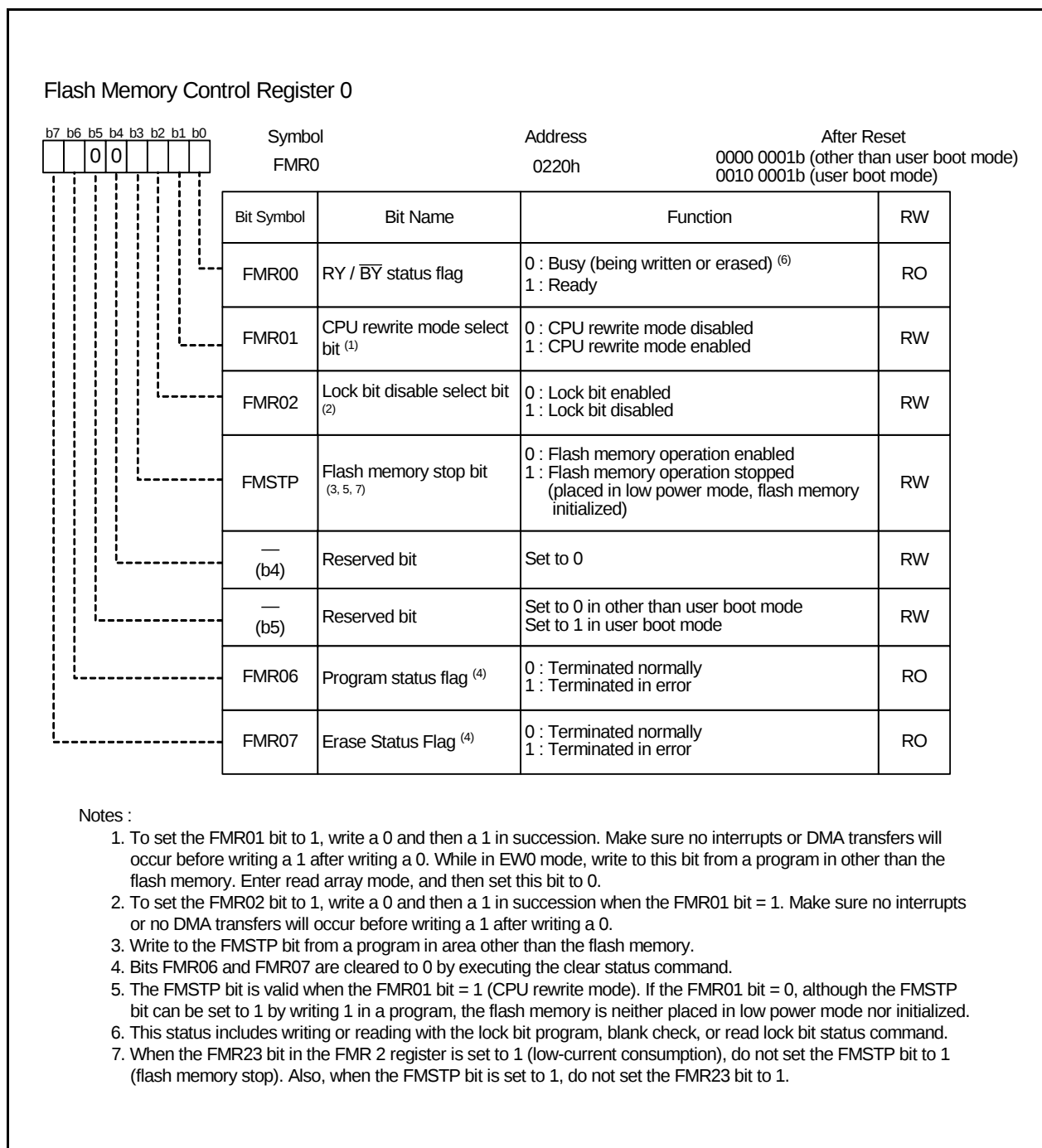


Figure 22.5 FMR0 Register

$$VCC1=VCC2=5V$$

Switching Characteristics

(VCC1 = VCC2 = 5V, VSS = 0V, at T_{opr} = –20 to 85°C/-40 to 85°C unless otherwise specified)

Table 23.24 Memory Expansion and Microprocessor Modes (for setting with no wait)

Symbol	Parameter	Measuring Condition	Standard		Unit
			Min.	Max.	
td(BCLK-AD)	Address Output Delay Time	See Figure 23.2		25	ns
th(BCLK-AD)	Address Output Hold Time (in relation to BCLK)		2		ns
th(RD-AD)	Address Output Hold Time (in relation to RD)		0		ns
th(WR-AD)	Address Output Hold Time (in relation to WR)		(NOTE 2)		ns
td(BCLK-CS)	Chip Select Output Delay Time			25	ns
th(BCLK-CS)	Chip Select Output Hold Time (in relation to BCLK)		2		ns
td(BCLK-ALE)	ALE Signal Output Delay Time			15	ns
th(BCLK-ALE)	ALE Signal Output Hold Time		–4		ns
td(BCLK-RD)	RD Signal Output Delay Time			25	ns
th(BCLK-RD)	RD Signal Output Hold Time		0		ns
td(BCLK-WR)	WR Signal Output Delay Time			25	ns
th(BCLK-WR)	WR Signal Output Hold Time		0		ns
td(BCLK-DB)	Data Output Delay Time (in relation to BCLK)			40	ns
th(BCLK-DB)	Data Output Hold Time (in relation to BCLK) ⁽³⁾		2		ns
td(DB-WR)	Data Output Delay Time (in relation to WR)		(NOTE 1)		ns
th(WR-DB)	Data Output Hold Time (in relation to WR) ⁽³⁾		(NOTE 2)		ns
td(BCLK-HLDA)	HLDA Output Delay Time			40	ns

Notes:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 40[\text{ns}] \quad f(\text{BCLK}) \text{ is } 12.5\text{MHz or less.}$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 10[\text{ns}]$$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.

Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.

Hold time of data bus is expressed in

$$t = -CR \times \ln(1 - \text{VOL} / VCC2)$$

by a circuit of the right figure.

For example, when VOL = 0.2VCC2, C = 30pF, R = 1kΩ, hold time of output "L" level is

$$t = -30\text{pF} \times 1\text{k}\Omega \times \ln(1 - 0.2VCC2 / VCC2)$$

$$= 6.7\text{ns.}$$

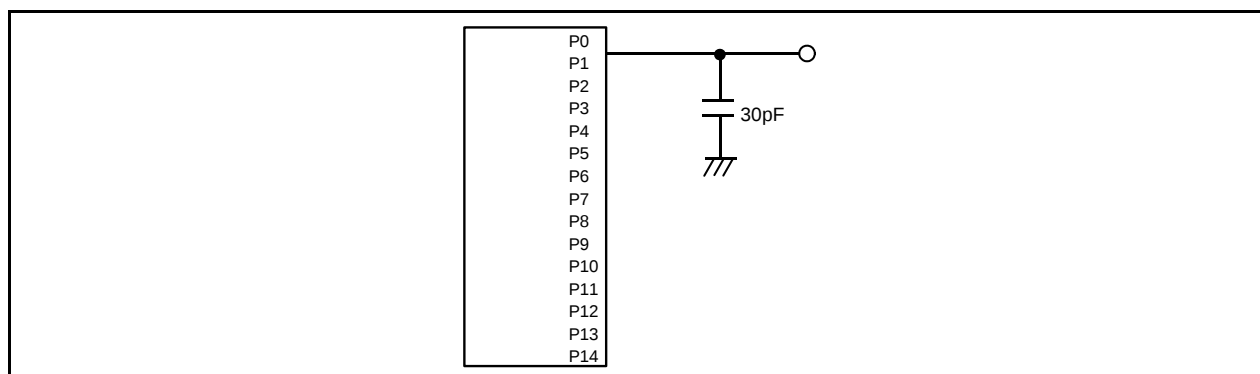
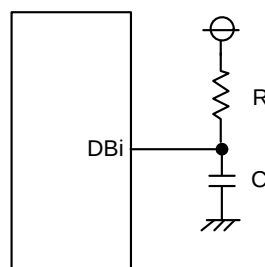


Figure 23.2 Ports P0 to P14 Measurement Circuit

Table 23.28 Electrical Characteristics (2) ⁽¹⁾

Symbol	Parameter		Measuring Condition		Standard			Unit
					Min.	Typ.	Max.	
ICC	Power Supply Current (VCC1=2.7V to 3.6V)	In single-chip mode, the output pins are open and other pins are VSS	Flash Memory	f(BCLK)=25MHz, No division		20	30	mA
				125 kHz On-chip oscillation, No division, FMR22=1		450		μA
			Flash Memory Program	f(BCLK)=10MHz, VCC1=3.0V		20		mA
			Flash Memory Erase	f(BCLK)=10MHz, VCC1=3.0V		30		mA
			Flash Memory	f(BCLK)=32kHz Low power dissipation mode, RAM ⁽³⁾		40		μA
				f(BCLK)=32kHz Low power dissipation mode, Flash Memory ⁽³⁾ FMR22=FMR23=1		200		μA
				125 kHz On-chip oscillation, Wait mode		20		μA
				f(BCLK)=32kHz Wait mode ⁽²⁾ , Oscillation capability High		7.0		μA
				f(BCLK)=32kHz Wait mode ⁽²⁾ , Oscillation capability Low		5.0		μA
				Stop mode Topr =25°C		1.8	4	μA
Idet2	Low Voltage Detection Dissipation Current ⁽⁴⁾				3		μA	
Idet0	Reset Area Detection Dissipation Current ⁽⁴⁾				6		μA	

Notes:

1. Referenced to VCC1=VCC2=2.7 to 3.3V, VSS = 0V at T_{opr} = -20 to 85°C/-40 to 85°C, f(BCLK)=25MHz unless otherwise specified.
2. With one timer operated using fC32.
3. This indicates the memory in which the program to be executed exists.
4. I_{det} is dissipation current when the following bit is set to "1" (detection circuit enabled).
Idet2: VC27 bit in the VCR2 register
Idet0: VC25 bit in the VCR2 register

24.9.1.4 Timer A (Pulse Width Modulation Mode)

The timer is stopped after reset. Set the mode, count source, counter value, and others using the TAI_iMR register, the TAI_i register, bits TA0TGL and TA0TGH in the ONSF register, the TRGSR register, registers TACS0 to TACS2, and the TAPOF register before setting the TAI_iS bit in the TABSR register to 1 (count starts) (*i* = 0 to 4).

Always make sure the TAI_iMR register, bits TA0TGL and TA0TGH in the ONSF register, the TRGSR register, registers TACS0 to TACS2, and the TAPOFS register are modified while the TAI_iS bit is 0 (count stops) regardless of whether after reset or not.

The IR bit is set to 1 when setting a timer operating mode with any of the following procedures:

- Select PWM mode after reset.
- Change an operating mode from timer mode to PWM mode.
- Change an operating mode from event counter mode to PWM mode.

To use the timer A_i interrupt (IR bit), set the IR bit to 0 by program after the changes listed above are made.

When setting the TAI_iS register to 0 (count stops) during PWM pulse output, the following action occurs.

When the POFS_i bit in the TAPOFS register is 0:

- Stop counting.
- When the TAI_iOUT pin is output "H," output level is set to "L" and the IR bit is set to 1.
- When the TAI_iOUT pin is output "L," both output level and the IR bit remains unchanged.

When the POFS_i bit in the TAPOFS register is 1:

- Stop counting.
- When the TAI_iOUT pin is output "L," output level is set to "H" and the IR bit is set to 1.
- When the TAI_iOUT pin is output "H," both output level and the IR bit remains unchanged.

If a low-level signal is applied to the $\overline{SD}$ pin when the IVPCR1 bit in the TB2SC register = 1 (three-phase output forcible cutoff by input on the $\overline{SD}$ pin enabled), pins TA1OUT, TA2OUT, and TA4OUT go to high-impedance state.

24.9.2 Timer B

24.9.2.1 Timer B (Timer Mode)

The timer is stopped after reset. Set the mode, count source, counter value, and others using registers TBiMR, TBi, and TBCS0 to TBCS3 before setting the TBiS bit in the TABSR or the TBSR register to 1 (count starts) ($i = 0$ to 5).

Always make sure the TBiMR register and registers TBCS0 to TBCS3 are modified while the TBiS bit is 0 (count stops) regardless of whether after reset or not.

A value of a counter while counting, can be read in the TBi register at any time. FFFFh is read while reloading. If the counter is read before it starts counting after a value is set in the TBi register while not counting, the set value is read.

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