Renesas Electronics America Inc - R5F3640MDFA#UZ Datasheet

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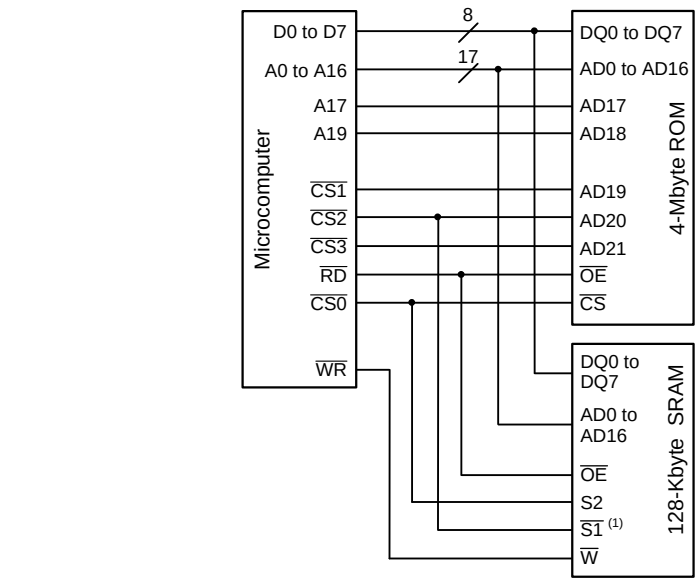
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	-
Core Size	-
Speed	-
Connectivity	-
Peripherals	-
Number of I/O	-
Program Memory Size	-
Program Memory Type	-
EEPROM Size	-
RAM Size	-
Voltage - Supply (Vcc/Vdd)	-
Data Converters	-
Oscillator Type	-
Operating Temperature	-
Mounting Type	-
Package / Case	-
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f3640mdfa-uz

Table 1.2 Specifications (2)

Item	Function	Specification
A/D Converter		10-bit resolution × 26 channels, including sample and hold function, Conversion time: 1.72 µs
D/A Converter		8-bit resolution × 2
CRC Calculation Circuit		CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$) compliant
Flash Memory		Programming and erasure power supply voltage: 2.7 V to 5.5 V Programming and erasure endurance: 100 times Program security: ROM code protect, ID code check
Debug Function		Functions on-chip debug, on-board flash rewrite function, address match × 4
Operation Frequency/Supply Voltage		25 MHz/VCC1 = VCC2 = 2.7 to 5.5 V
Power Consumption		20 mA (25 MHz/VCC1 = VCC2 = 3 V)TBD 3.0 µA(VCC1 = VCC2 = 3 V, in stop mode)
Operating Temperature		-20°C to 85°C, -40°C to 85°C
Package		100-pin QFP: PRQP0100JD-B (Previous package code: 100P6F-A) 100-pin LQFP: PLQP0100KB-A (Previous package code: 100P6Q-A)

Figure 9.6 shows the External Memory Connect Example in 4-Mbyte Mode.
In this example, the $\overline{CS}$ pin of 4-Mbyte ROM is connected to the $\overline{CS0}$ pin of the microcomputer. The 4-Mbyte ROM address input pins AD21, AD20, and AD19 are connected to pins $\overline{CS3}$, $\overline{CS2}$, and $\overline{CS1}$ of the microcomputer, respectively. The address input AD18 pin is connected to the A19 pin of microcomputer. Figures 9.7 to 9.9 show the relationship of addresses between the 4-Mbyte ROM and the microcomputer for the case of a connection example in Figure 9.6.
In microprocessor mode or in memory expansion mode where the PM13 bit in the PM1 register is 0, banks are located every 512 Kbytes. Setting the OFS bit in the DBR register to 1 (offset) allows the accessed address to be offset by 40000h, so that even the data overlapping at a bank boundary can be accessed in succession.
In memory expansion mode where the PM13 bit is 1, each 512-Kbyte bank can be accessed in 256 Kbyte units by switching them over with the OFS bit.
Because the SRAM can be accessed on condition that the chip select signals S2 = “H” and $\overline{S1}$ = “L”, $\overline{CS0}$ and $\overline{CS2}$ can be connected to S2 and $\overline{S1}$, respectively. If the SRAM does not have the input pins which accept “H” active and “L” active chip select signals ($\overline{S1}$, S2), $\overline{CS0}$ and $\overline{CS2}$ should be decoded external to the chip.



Note :
1. If only one chip select pin ($\overline{S1}$ or S2) is present, using an external circuit is required for decode.

Figure 9.6 External Memory Connect Example in 4-Mbyte Mode

10.6 Oscillation Stop and Re-Oscillation Detect Function

The oscillation stop and re-oscillation detect function is such that main clock oscillation circuit stop and re-oscillation are detected. At oscillation stop or re-oscillation detection, reset oscillation stop or re-oscillation detection interrupt are generated. Which is to be generated can be selected using the CM27 bit in the CM2 register. The oscillation stop and re-oscillation detect function can be enabled and disabled by the CM20 bit in the CM2 register. Table 10.8 lists a Specification Overview of Oscillation Stop and Re-Oscillation Detect Function.

Table 10.8 Specification Overview of Oscillation Stop and Re-Oscillation Detect Function

Item	Specification
Oscillation Stop Detectable Clock and Frequency Bandwidth	f(XIN) ≥ 2 MHz
Enabling Condition for Oscillation Stop, Re-Oscillation Detect Function	Set CM20 bit to 1 (enabled)
Operation at Oscillation Stop, Re-Oscillation Detection	Reset occurs (when CM27 bit = 0) Oscillation stop, re-oscillation detection interrupt generated (when CM27 bit = 1)

10.6.1 Operation When CM27 bit = 0 (Oscillation Stop Detection Reset)

When main clock stop is detected when the CM20 bit is 1 (oscillation stop, re-oscillation detection function enabled), the microcomputer is initialized, coming to a halt (oscillation stop reset. Refer to **4. "Special Function Registers (SFRs)", 5. "Reset"**).

This status is reset with hardware reset 1 or brown-out reset. Also, even when re-oscillation is detected, the microcomputer can be initialized and stopped; it is, however, necessary to avoid such usage (During main clock stop, do not set the CM20 bit to 1 and the CM27 bit to 0).

10.6.2 Operation When CM27 bit = 1 (Oscillation Stop and Re-oscillation Detect Interrupt)

When the main clock corresponds to the CPU clock source and the CM20 bit is 1 (oscillation stop and re-oscillation detect function enabled), the system is placed in the following state if the main clock comes to a halt.

- Oscillation stop and re-oscillation detect interrupt request occurs.
- CM14 bit = 0 (125 kHz on-chip oscillator clock oscillates)
- CM21 bit = 1 (125 kHz on-chip oscillator clock for CPU clock source and clock source of peripheral function.)
- CM22 bit = 1 (main clock stop detected)
- CM23 bit = 1 (main clock stopped)

When the PLL clock corresponds to the CPU clock source and the CM20 bit is 1, the system is placed in the following state if the main clock comes to a halt. Since the CM21 bit remains unchanged, set it to 1 (125 kHz on-chip oscillator clock) inside the interrupt routine.

- Oscillation stop and re-oscillation detect interrupt request occurs.
- CM14 bit = 0 (125 kHz on-chip oscillator clock oscillates)
- CM22 bit = 1 (main clock stop detected)
- CM23 bit = 1 (main clock stopped)
- CM21 bit remains unchanged

When the CM20 bit is 1, the system is placed in the following state if the main clock re-oscillates from the stop condition.

- Oscillation stop and re-oscillation detect interrupt request occurs.
- CM14 bit = 0 (125 kHz on-chip oscillator clock oscillates)
- CM22 bit = 1 (main clock re-oscillation detected)
- CM23 bit = 0 (main clock oscillation)
- CM21 bit remains unchanged

12.6 $\overline{\text{INT}}$ Interrupt

$\overline{\text{INTi}}$ interrupt (i = 0 to 7) is triggered by the edges of external inputs. The edge polarity is selected using the IFSRi bit in the IFSR register, or the IFSR30 or IFSR31 bit in the IFSR3A register.

$\overline{\text{INT4}}$ and $\overline{\text{INT5}}$ share the interrupt vector and interrupt control register with SI/O3 and SI/O4, respectively. To use the $\overline{\text{INT4}}$ interrupt, set the IFSR6 bit in the IFSR register to 1 ($\overline{\text{INT4}}$). To use the $\overline{\text{INT5}}$ interrupt, set the IFSR7 bit in the IFSR register to 1 ($\overline{\text{INT5}}$).

After modifying the IFSR6 or IFSR7 bit, clear the corresponding IR bit to 0 (interrupt not requested) before enabling the interrupt.

To use the $\overline{\text{INT6}}$ interrupt, set the PCR5 bit in the PCR register to 0 ($\overline{\text{INT6}}$ input enabled). To use the $\overline{\text{INT7}}$ interrupt, set the PCR6 bit in the PCR register to 0 ($\overline{\text{INT7}}$ input enabled).

Figure 12.11 shows the IFSR Register, and Figure 12.12 shows Registers IFSR2A, IFSR3A, and PCR.

Interrupt Source Select Register

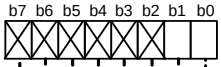
b7	b6	b5	b4	b3	b2	b1	b0	Symbol	Address	After Reset
								IFSR	0207h	00h

Bit Symbol	Bit Name	Function	RW
IFSR0	INT0 interrupt polarity switch bit	0 : One edge 1 : Both edges (1)	RW
IFSR1	INT1 interrupt polarity switch bit	0 : One edge 1 : Both edges (1)	RW
IFSR2	INT2 interrupt polarity switch bit	0 : One edge 1 : Both edges (1)	RW
IFSR3	INT3 interrupt polarity switch bit	0 : One edge 1 : Both edges (1)	RW
IFSR4	INT4 interrupt polarity switch bit	0 : One edge 1 : Both edges (1)	RW
IFSR5	INT5 interrupt polarity switch bit	0 : One edge 1 : Both edges (1)	RW
IFSR6	Interrupt request source select bit (2)	0 : SI/O3 (3) 1 : $\overline{\text{INT4}}$	RW
IFSR7	Interrupt request source select bit (2)	0 : SI/O4 (3) 1 : $\overline{\text{INT5}}$	RW

Notes :
1. When setting this bit to 1 (both edges), make sure the POL bit in registers INT0IC to INT5IC are set to 0 (falling edge).
2. During memory expansion and microprocessor modes, when the data bus is 16 bits wide (BYTE pin is “L”), set this bit to 0 (SI/O3, SI/O4).
3. When setting this bit to 0 (SI/O3, SI/O4), make sure the POL bit in registers S3IC and S4IC are set to 0 (falling edge).

Figure 12.11 IFSR Register

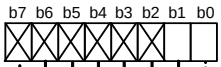
Address Match Interrupt Enable Register



Symbol	Address	After Reset
AIER	020Eh	XXXXXX00b

Bit Symbol	Bit Name	Function	RW
AIER0	Address match interrupt 0 enable bit	0 : Interrupt disabled 1 : Interrupt enabled	RW
AIER1	Address match interrupt 1 enable bit	0 : Interrupt disabled 1 : Interrupt enabled	RW
— (b7-b2)	No register bits. If necessary, set to 0. Read as undefined value		—

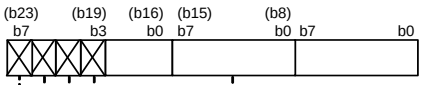
Address Match Interrupt Enable Register 2



Symbol	Address	After Reset
AIER2	020Fh	XXXXXX00b

Bit Symbol	Bit Name	Function	RW
AIER20	Address match interrupt 2 enable bit	0 : Interrupt disabled 1 : Interrupt enabled	RW
AIER21	Address match interrupt 3 enable bit	0 : Interrupt disabled 1 : Interrupt enabled	RW
— (b7-b2)	No register bits. If necessary, set to 0. Read as undefined value		—

Address Match Interrupt Register i (i = 0 to 3)

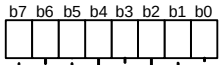


Symbol	Address	After Reset
RMAD0	0212h to 0210h	X00000h
RMAD1	0216h to 0214h	X00000h
RMAD2	021Ah to 0218h	X00000h
RMAD3	021Eh to 021Ch	X00000h

Function	Setting Range	RW
Address setting register for address match interrupt (b19 to b0)	00000h to FFFFFh	RW
No register bits. If necessary, set to 0. Read as undefined value		—

Figure 12.14 Registers AIER, AIER2, and RMAD0 to RMAD3

UARTi Transmit / Receive Control Register 0 (i = 0 to 2, 5 to 7)



Symbol	Address	After Reset
U0C0, U1C0, U2C0	024Ch, 025Ch, 026Ch	00001000b
U5C0, U6C0, U7C0	028Ch, 029Ch, 02ACh	00001000b

Bit Symbol	Bit Name	Function	RW
CLK0	UiBRG count source select bit (6)	b1 b0 0 0 : f1SIO or f2SIO is selected (5) 0 1 : f8SIO is selected 1 0 : f32SIO is selected 1 1 : Do not set to this value	RW
CLK1			RW
CRS	$\overline{CTS}$ / $\overline{RTS}$ function select bit (4)	Valid when CRD = 0 0 : $\overline{CTS}$ function selected (1) 1 : $\overline{RTS}$ function selected	RW
TXEPT	Transmit register empty flag	0 : Data present in transmit register (during transmission) 1 : No data present in transmit register (transmission completed)	RO
CRD	$\overline{CTS}$ / $\overline{RTS}$ disable bit	0 : $\overline{CTS}$ / $\overline{RTS}$ function enabled 1 : $\overline{CTS}$ / $\overline{RTS}$ function disabled (P6_0, P6_4, P7_3, P8_1, P1_0, and P4_4 can be used as I/O ports)	RW
NCH	Data output select bit (2)	0 : Pins TXDi / SDAi and SCLi are CMOS output 1 : Pins TXDi / SDAi and SCLi are N-channel open-drain output	RW
CKPOL	CLK polarity select bit	0 : Transmit data is output at the falling edge of transfer clock and receive data is input at the rising edge 1 : Transmit data is output at the rising edge of transfer clock and receive data is input at the falling edge	RW
UFORM	Transfer format select bit (3)	0 : LSB first 1 : MSB first	RW

Notes :
1. Set the corresponding port direction bit for each $\overline{CTSi}$ pin to 0 (input mode).
2. TXD2 / SDA2 and SCL2 are N-channel open-drain output. Cannot be set to the CMOS output. No NCH bit in the U2C0 register is assigned. If necessary, set to 0.
3. The UFORM bit is enabled when bits SMD2 to SMD0 in the UiMR register are set to 001b (clock synchronous serial I/O mode), or 101b (UART mode, 8-bit transfer data).
   Set this bit to 1 when bits SMD2 to SMD0 are set to 010b (I^2C mode), and to 0 when bits SMD2 to SMD0 are set to 100b (UART mode, 7-bit transfer data) or 110b (UART mode, 9-bit transfer data).
4. $\overline{CTS1}$ / $\overline{RTS1}$ can be used when the CLKMD1 bit in the UCON register = 0 (only CLK1 output) and the RCSP bit in the UCON register = 0 ($\overline{CTS0}$ / $\overline{RTS0}$ not separated).
5. Selected by the PCLK1 bit in the PCLKR register.
6. When changing bits CLK1 and CLK0, set the UiBRG register.

Figure 17.7 Registers U0C0 to U2C0 and U5C0 to U7C0

17.1.6.2 Format

Two formats are available: direct format and inverse format.
In direct format, set the PRYE bit in the U2MR register to 1 (parity enabled), the PRY bit to 1(even parity), the UFORM bit in the U2C0 register to 0 (LSB first) and the U2LCH bit in the U2C1 register to 0 (not inverted). When data are transmitted, data set in the U2TB register are transmitted with the even-numbered parity, starting from D0. When data are received, received data are stored in the U2RB register, starting from D0. The even-numbered parity determines whether a parity error occurs.
In inverse format, set the PRYE bit to 1, the PRY bit to 0 (odd parity), the UFORM bit to 1 (MSB first), and the U2LCH bit to 1 (inverted). When data are transmitted, values set in the U2TB register are logically inversed and are transmitted with the odd-numbered parity, starting from D7. When data are received, received data are logically inversed to be stored in the U2RB register, starting from D7. The odd-numbered parity determines whether a parity error occurs.

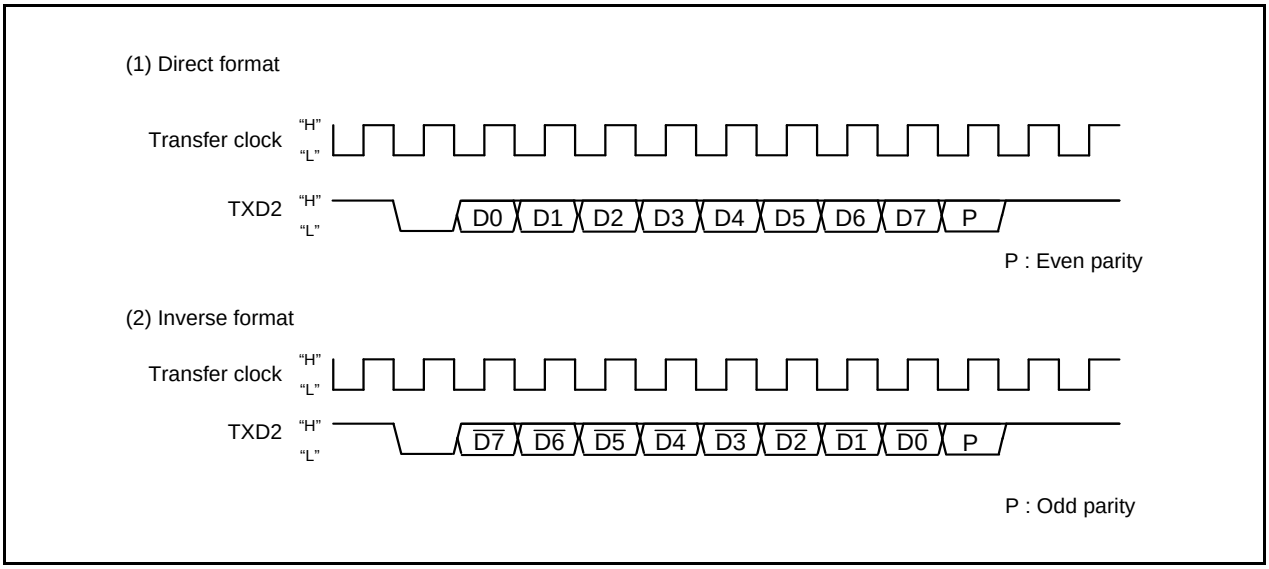


Figure 17.36 SIM Interface Format

22.3.3.5 FMR06 Bit

This is a read-only bit indicating an auto program operation state. The FMR06 bit is set to 1 when a program error occurs; otherwise, it is set to 0. Refer to **22.3.8 "Full Status Check"**.

22.3.3.6 FMR07 Bit

This is a read-only bit indicating the auto erase operation status. The FMR07 bit is set to 1 when an erase error occurs; otherwise, it is set to 0. The FMR07 bit is also used for blank check. For details, refer to **22.3.8 "Full Status Check"**.

22.3.3.7 FMR11 Bit

The FMR11 bit enables programming to the FMR6 register.

22.3.3.8 FMR16 Bit

This is a read-only bit indicating the execution result of the read lock bit status command.
When the block, where the read lock bit status command is executed, is locked, the FMR16 bit is set to 0.
When the block, where the read lock bit status command is executed, is unlocked, the FMR16 bit is set to 1.

22.3.3.9 FMR17 Bit

This is a bit to select wait state for data flash.

22.3.3.10 FMR22 Bit

This bit enables the mode to reduce the amount of current consumption when reading the flash memory. When rewriting the flash memory (CPU rewrite mode), set the FMR22 bit to 0 (slow read mode disabled).
Also, when f(BCLK) > 5 MHz, set the FMR22 bit to 0 (slow read mode disabled).
Figure 22.10 shows setting and resetting of the slow read mode.

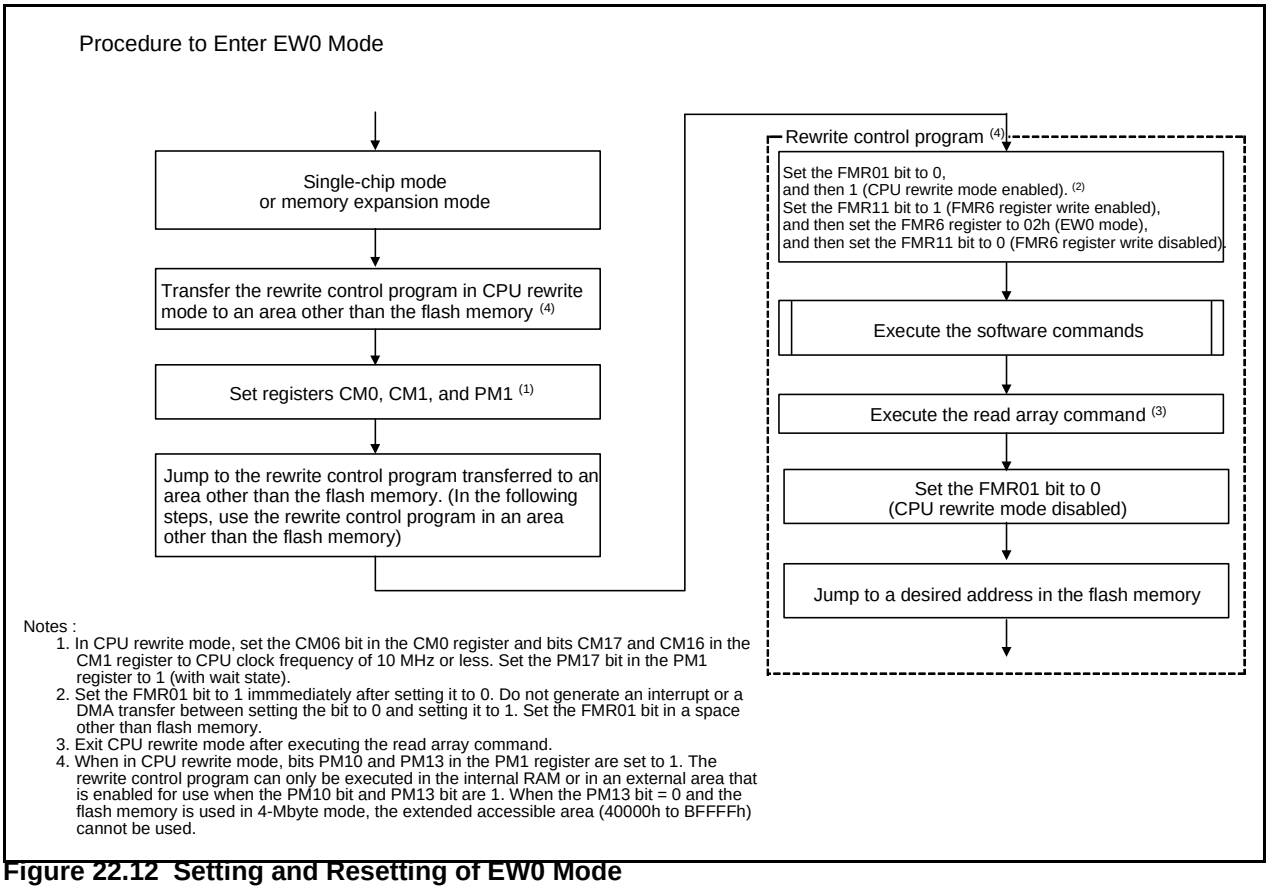


Figure 22.12 Setting and Resetting of EW0 Mode

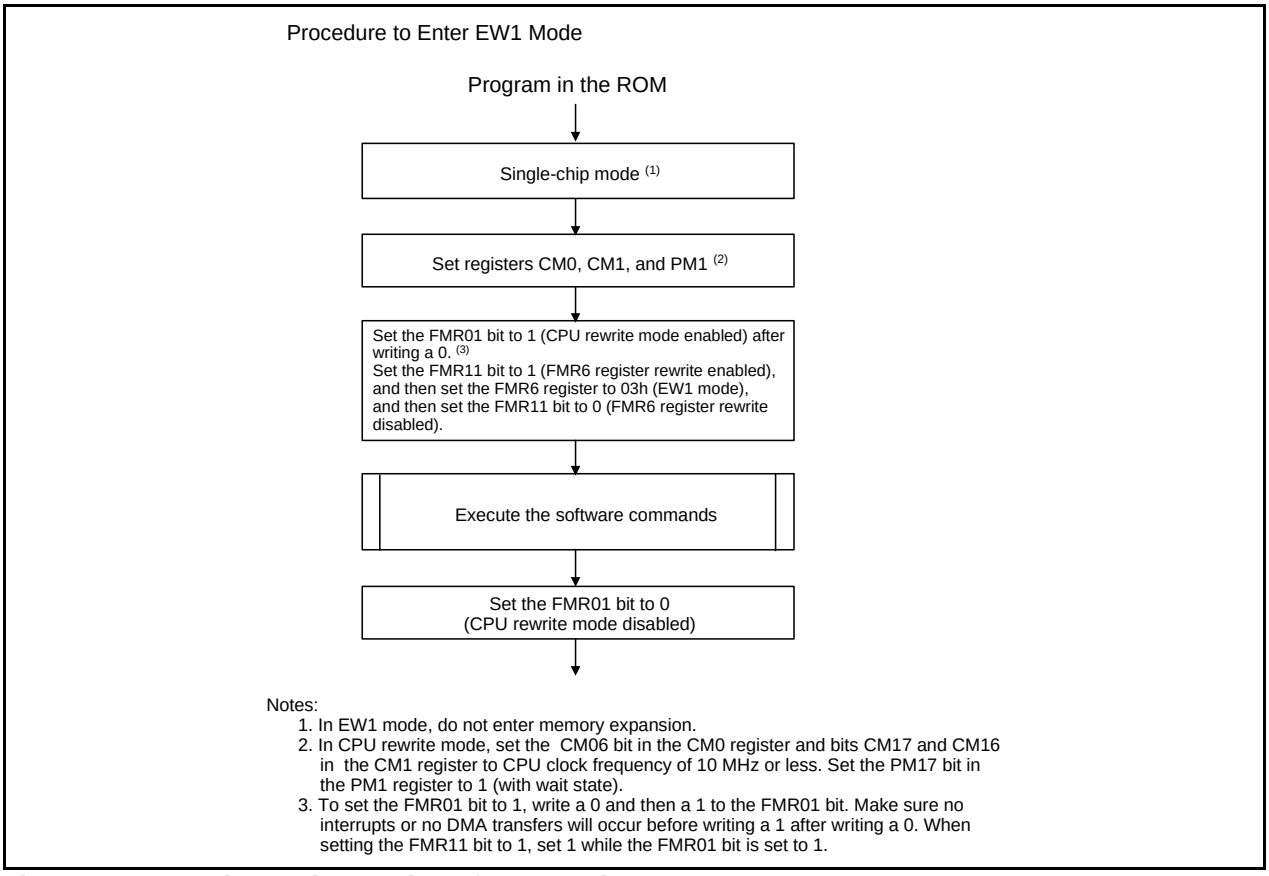


Figure 22.13 Setting and Resetting of EW1 Mode

23. Electrical Characteristics

23.1 Electrical Characteristics

Table 23.1 Absolute Maximum Ratings

Symbol	Parameter		Condition	Rated Value	Unit
VCC1, VCC2	Supply Voltage		VCC1=VCC2 =AVCC	−0.3 to 6.5	V
AVCC	Analog Supply Voltage		VCC1=AVCC	−0.3 to 6.5	V
VI	Input Voltage	$\overline{\text{RESET}}$, CNVSS, BYTE, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7 XIN		−0.3 to VCC1+0.3	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7,		−0.3 to VCC2+0.3	V
		P7_0, P7_1, P8_5		−0.3 to 6.5	V
VO	Output Voltage	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, XOUT		−0.3 to VCC1+0.3	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7		−0.3 to VCC2+0.3	V
		P7_0, P7_1, P8_5		−0.3 to 6.5	V
Pd	Power Dissipation		−40°C<Topr≤85°C	300	mW
Topr	Operating Ambient Temperature	When the Microcomputer is Operating		−20 to 85/-40 to 85	°C
		Flash Program Erase		0 to 60	
Tstg	Storage Temperature			−65 to 150	°C

Table 23.2 Recommended Operating Conditions (1)

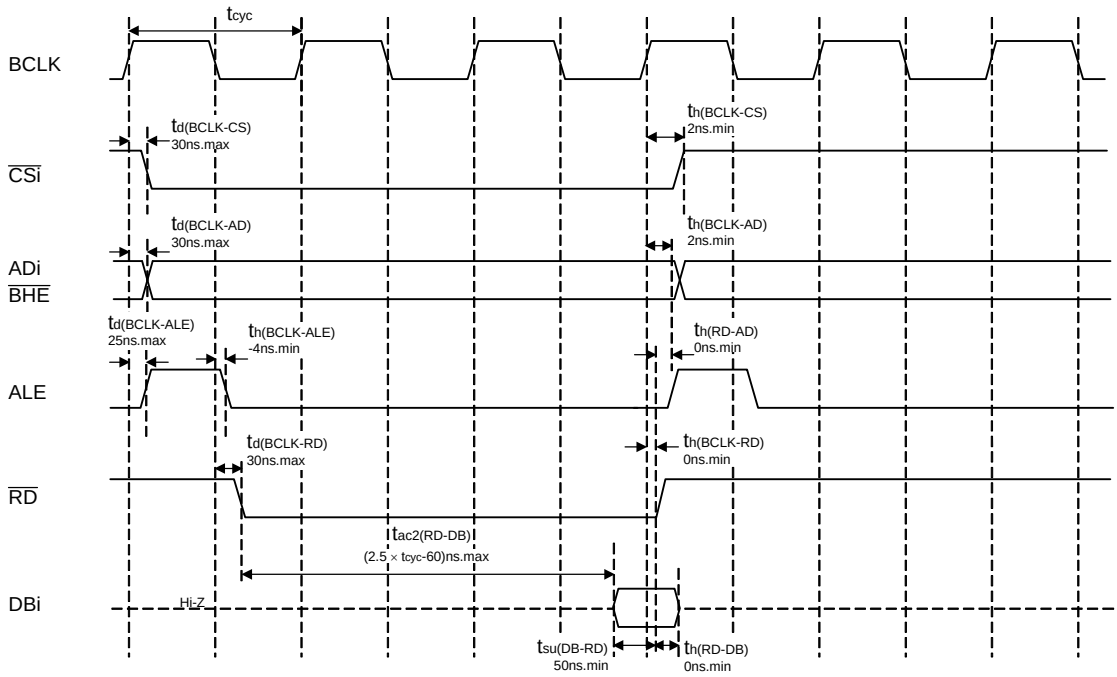
Symbol	Parameter			Standard			Unit
				Min.	Typ.	Max.	
VCC1, VCC2	Supply Voltage (VCC1 = VCC2)			2.7	5.0	5.5	V
AVCC	Analog Supply Voltage				VCC1		V
VSS	Supply Voltage				0		V
AVSS	Analog Supply Voltage				0		V
VIH	HIGH Input Voltage	P3_1 to P3_7, P4_0 to P4_7, P5_0 to P5_7		0.8VCC2		VCC2	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (during single-chip mode)		0.8VCC2		VCC2	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (data input during memory expansion and microprocessor mode)		0.5VCC2		VCC2	V
		P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, XIN, $\overline{\text{RESET}}$, CNVSS, BYTE		0.8VCC1		VCC1	V
		P7_0, P7_1, P8_5		0.8VCC1		6.5	V
VIL	LOW Input Voltage	P3_1 to P3_7, P4_0 to P4_7, P5_0 to P5_7		0		0.2VCC2	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (during single-chip mode)		0		0.2VCC2	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (data input during memory expansion and microprocessor mode)		0		0.16VCC2	V
		P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, XIN, $\overline{\text{RESET}}$, CNVSS, BYTE		0		0.2VCC	V
IOH(peak)	HIGH Peak Output Current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7				−10.0	mA
IOH(avg)	HIGH Average Output Current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7,				−5.0	mA
IOL(peak)	LOW Peak Output Current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7				10.0	mA
IOL(avg)	LOW Average Output Current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7				5.0	mA
f(XIN)	Main Clock Input Oscillation Frequency		VCC1=2.7V to 5.5V	0		20	MHz
f(XCIN)	Sub-Clock Oscillation Frequency				32.768	50	kHz
f(OCO)	125kHz On-chip Oscillation Frequency			100	125	150	kHz
f(PLL)	PLL Clock Oscillation Frequency		VCC1=2.7V to 5.5V	10		25	MHz
f(BCLK)	CPU Operation Clock			0		25	MHz
tSU(PLL)	PLL Frequency Synthesizer Stabilization Wait Time		VCC1=5.0V			3	ms
			VCC1=3.0V			2	ms

Notes:
1. Referenced to VCC1 = VCC2 = 2.7 to 5.5V at Topr = −20 to 85°C/-40 to 85°C unless otherwise specified.
2. The Average Output Current is the mean value within 100ms.
3. The total IOL(peak) for ports P0, P1, P2, P8_6, P8_7, P9 and P10 must be 80mA max. The total IOL(peak) for ports P3, P4, P5, P6, P7 and P8_0 to P8_5 must be 80mA max. The total IOH(peak) for ports P0, P1, and P2 must be −40mA max. The total IOH(peak) for ports P3, P4 and P5 must be −40mA max. The total IOH(peak) for ports P6, P7_2 to P7_7 and P8_0 to P8_4 must be −40mA max.

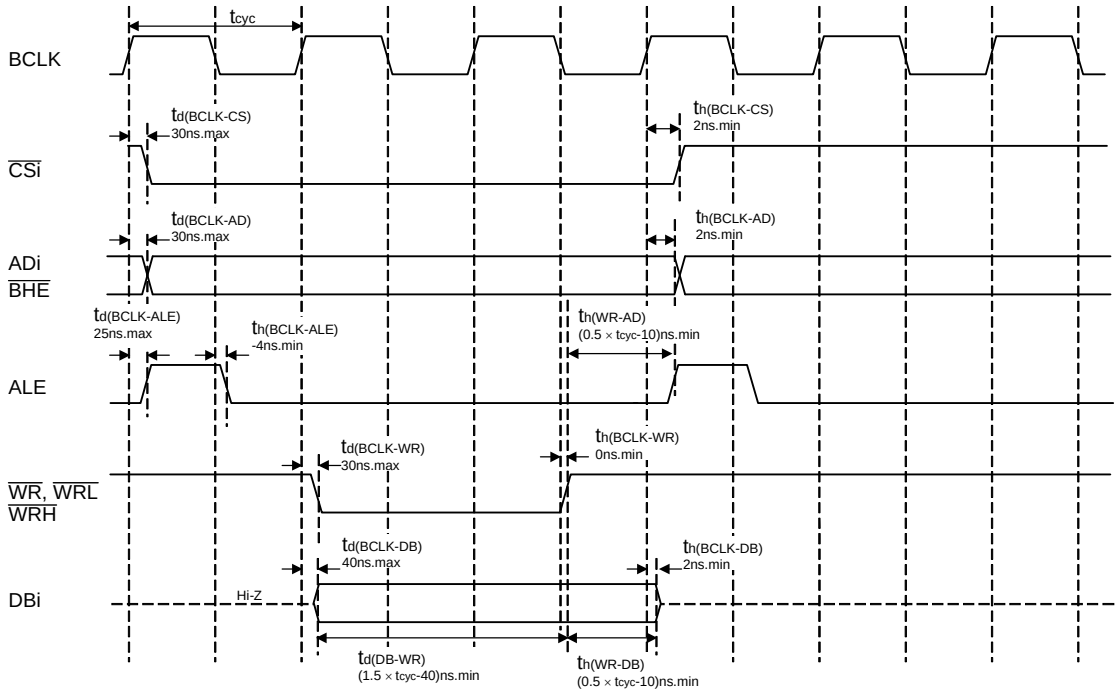
$V_{CC1}=V_{CC2}=3V$

Memory Expansion Mode, Microprocessor Mode
(for 2-wait setting and external area access**)**

Read timing



Write timing



$$t_{cyc}=\frac{1}{f(BCLK)}$$

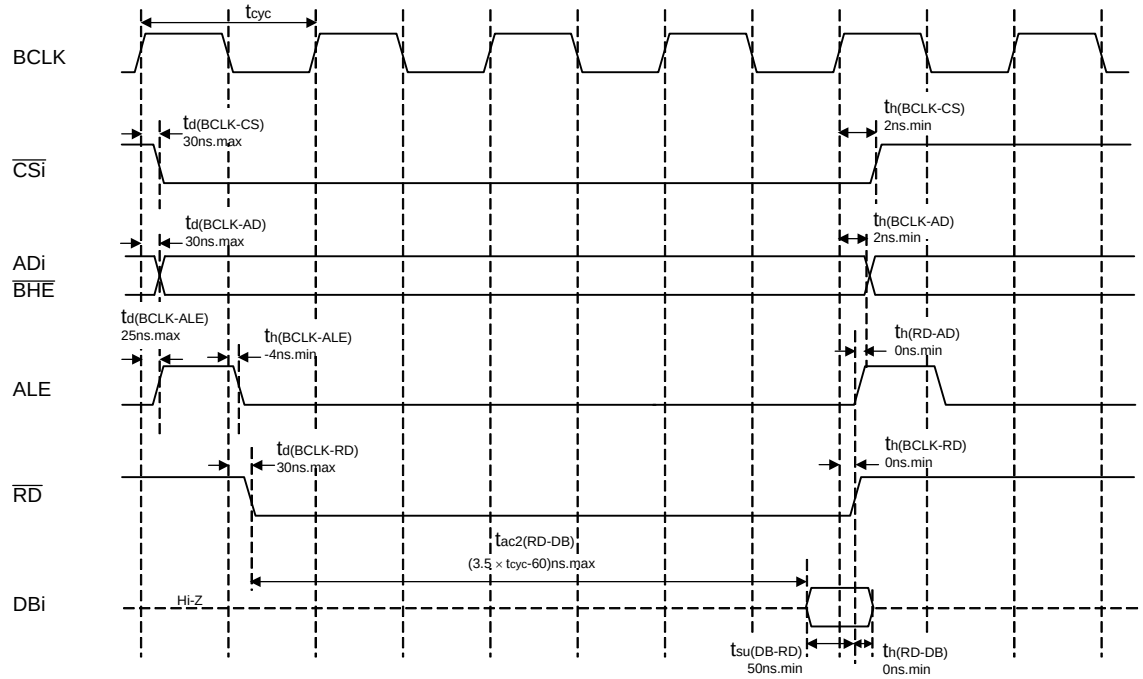
Measuring conditions
- $V_{CC1}=V_{CC2}=3V$
- Input timing voltage : $V_{IL}=0.6V$, $V_{IH}=2.4V$
- Output timing voltage : $V_{OL}=1.5V$, $V_{OH}=1.5V$

Figure 23.18 Timing Diagram (6)

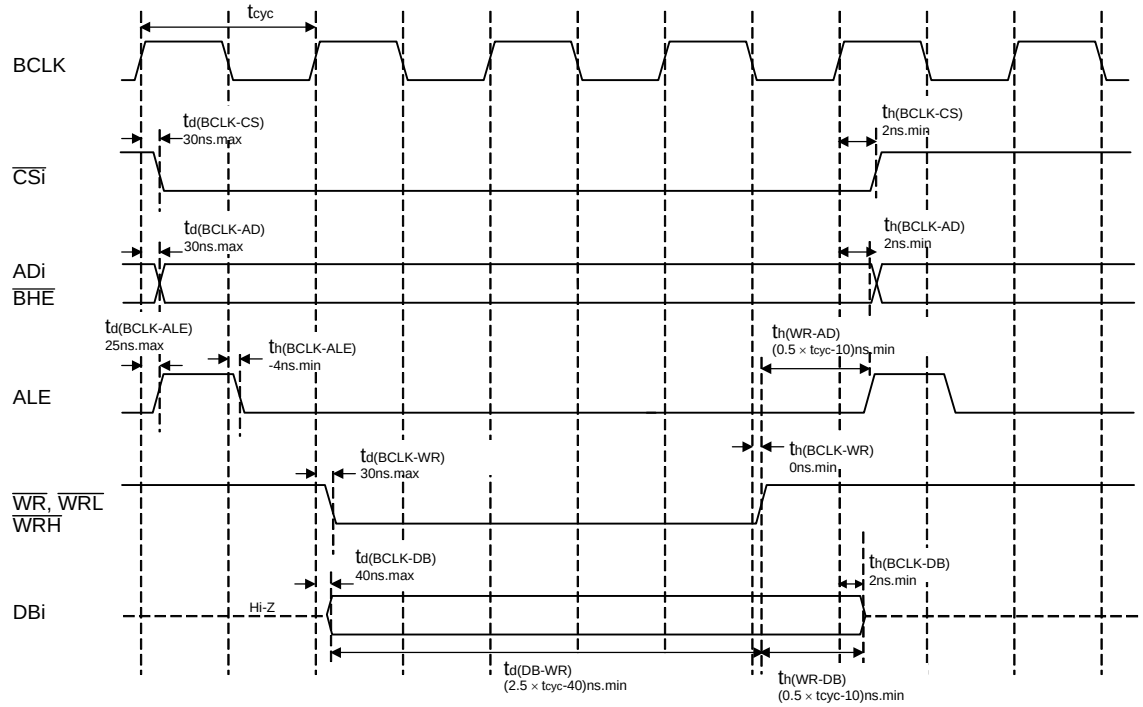
$V_{CC1} = V_{CC2} = 3V$

Memory Expansion Mode, Microprocessor Mode
(for 3-wait setting and external area access**)**

Read timing



Write timing



$$t_{cyc} = \frac{1}{f(BCLK)}$$

Measuring conditions
- V_{CC1}=V_{CC2}=3V
- Input timing voltage : V_{IL}=0.6V, V_{IH}=2.4V
- Output timing voltage : V_{OL}=1.5V, V_{OH}=1.5V

Figure 23.19 Timing Diagram (7)

24.2 Reset

24.2.1 VCC1

When supplying power to the microcomputer, the power supply voltage applied to the VCC1 pin must meet the conditions of SVCC.

Symbol	Parameter	Standard			Unit
		Min.	Typ.	Max.	
SVCC	Power supply rising gradient (VCC1) (Voltage range 0 to 2)	0.05			V / ms

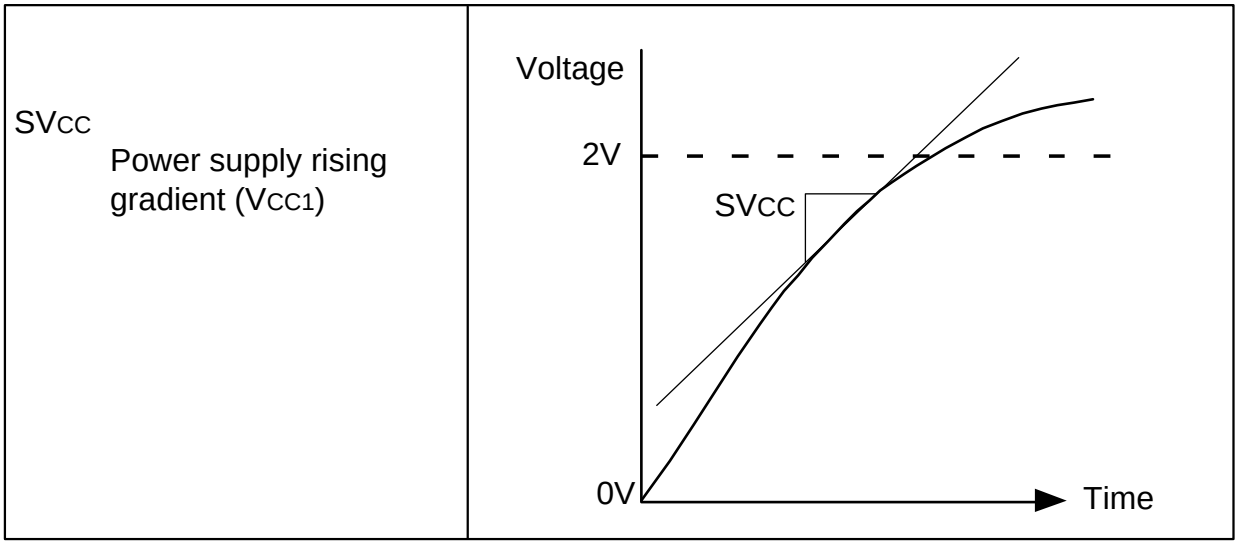


Figure 24.1 Timing of SVcc

24.2.2 CNVSS

To start to operate in single-chip mode after reset, connect to VSS via resistor. The internal pull-up of the CNVSS pin is on immediately after hardware reset 1 or 2 is released in single-chip mode. Therefore, the CNVSS pin level becomes high for two cycles of fOCO-S maximum.

24.7.6 Rewriting the Interrupt Control Register

(a) The interrupt control register for any interrupt should be modified in places where no requests for that interrupt may occur. Otherwise, disable the interrupt before rewriting the interrupt control register.

(b) To rewrite the interrupt control register for any interrupt after disabling that interrupt, be careful with the instruction to be used.

- Changing any bit other than the IR bit
  When interrupts corresponding to the register occur, the IR bit may not become 1 (interrupt requested) and the interrupts may be ignored. If this causes any troubles, use any of the following instructions to change registers.
  AND, OR, BCLR, or BSET.
- Changing the IR bit
  Depending on the instruction used, the IR bit may not always be cleared to 0 (interrupt not requested). Therefore, be sure to use the MOV instruction to clear the IR bit.

(c) When using the I flag to disable an interrupt, set the I flag while referring to the sample program fragments shown below. (Refer to (b) for details about rewriting the interrupt control registers in the sample program fragments.)

Examples 1 through 3 show how to prevent the I flag from being set to 1 (interrupt enabled) before the interrupt control register is rewritten, owing to the effects of the internal bus and the instruction queue buffer.

Example 1: Using the NOP instruction to keep the program waiting until the interrupt control register is modified

```
INT_SWITCH1:
  FCLR    I            ; Disable interrupts.
  AND.B   #00h, 0055h  ; Set the TA0IC register to 00h.
  NOP                  ;
  NOP
  FSET    I            ; Enable interrupts.
```

The number of the NOP instructions is as follows.
PM20 = 1 (1 wait) : 2, PM20 = 0 (2 waits) : 3, when using the HOLD function : 4.

Example 2: Using the dummy read to keep the FSET instruction waiting

```
INT_SWITCH2:
  FCLR    I            ; Disable interrupts.
  AND.B   #00h, 0055h  ; Set the TA0IC register to 00h.
  MOV.W   MEM, R0      ; Dummy read.
  FSET    I            ; Enable interrupts.
```

Example 3: Using the POPC instruction to change the I flag

```
INT_SWITCH3:
  PUSHC   FLG
  FCLR    I            ; Disable interrupts.
  AND.B   #00h, 0055h  ; Set the TA0IC register to 00h.
  POPC    FLG          ; Enable interrupts.
```

24.8 DMAC

24.8.1 Write to the DMAE Bit in the DMiCON Register (i = 0 to 3)

When both of the conditions below are met, follow the steps below.

Conditions

- The DMAE bit is set to 1 (DMAi is in active state) again while it remains 1.
- A DMA request may occur simultaneously when the DMAE bit is being written.

Steps

(1) Write a 1 to the DMAE bit and DMAS bit in the DMiCON register simultaneously (1).

(2) Make sure that the DMAi is in initial state (2) in a program.
If the DMAi is not in initial state, repeat the above steps.

Notes:

1. The DMAS bit remains unchanged even if a 1 is written. However, if a 0 is written to this bit, it is set to 0 (DMA not requested). In order to prevent the DMAS bit from being modified to 0, 1 should be written to the DMAS bit when 1 is written to the DMAE bit. In this way the state of the DMAS bit immediately before being written can be maintained.
2. Similarly, when writing to the DMAE bit with a read-modify-write instruction, 1 should be written to the DMAS bit in order to maintain a DMA request which is generated during execution.
3. Read the TCRi register to verify whether the DMAi is in initial state. If the read value is equal to a value which was written to the TCRi register before DMA transfer start, the DMAi is in initial state. (In the case a DMA request occurs after writing to the DMAE bit, the read value is a value written to the TCRi register minus one.) If the read value is a value in the middle of transfer, the DMAi is not in initial state.

24.8.2 DMAC Channel Priority

When a same DMA request source is selected for DMAC channels, the DMA transfer may not be executed in the priority order of DMA0>DMA1>DMA2>DMA3.

24.9.2.2 Timer B (Event Counter Mode)

The timer is stopped after reset. Set the mode, count source, counter value, and others using the TBiMR register and TBi register before setting the TBiS bit in the TABSR or the TBSR register to 1 (count starts) (i = 0 to 5).
Always make sure the TBiMR register is modified while the TBiS bit is 0 (count stops) regardless of whether after reset or not.

While counting is in progress, the counter value can be read out at any time by reading the TBi register. However, if this register is read at the same time the counter is reloaded, the read value is always FFFFh. If the TBi register is read after setting a value in it while not counting but before the counter starts counting, the read value is the value set in the register.

REGISTER INDEX

Rev.	Date	Description	
		Page	Summary
1.05	Feb 19, 2009	336	Figure 23.13 “Timing Diagram (1)” is partly modified.
		339	Figure 23.16 “Timing Diagram (4)” is partly modified.
		340	Figure 23.17 “Timing Diagram (5)” is partly modified.
		341	Figure 23.18 “Timing Diagram (6)” is partly modified.
		342	Figure 23.19 “Timing Diagram (7)” is partly modified.
		343	Figure 23.20 “Timing Diagram (8)” is partly modified.
		344	Figure 23.21 “Timing Diagram (9)” is partly modified.
		344	24.7.3 “NMI Interrupt” is partly modified.
		356	24.8.2 “DMAC Channel Priority” is partly modified.
		366	24.10.3.1 “Generating Conditions” and 24.10.3.2 “UART5, UART7” are added.
		368	24.11 “A/D Converter” is partly modified.
		370	24.11.1 “Repeat Mode, Repeat Sweep Mode 0, and Repeat Sweep Mode 1” is added.
		372	24.13.6 “Program Command” is added.
		373	24.13.11 “How to Access” is added.
		374	24.13.12 “Writing” is partly modified.
		375	24.13.15 “When Entering to Boot Mode” is added.
		377	Appendix 1. “Package Dimensions” is partly modified.
	Mar 17, 2009	312	Table 24.10 “Electrical Characteristics (2)” is partly modified.
		329	Table 24.28 “Electrical Characteristics (2)” is partly modified.
		379	Appendix 2. “Difference Between M16C/64 and M16C/62P” is added.