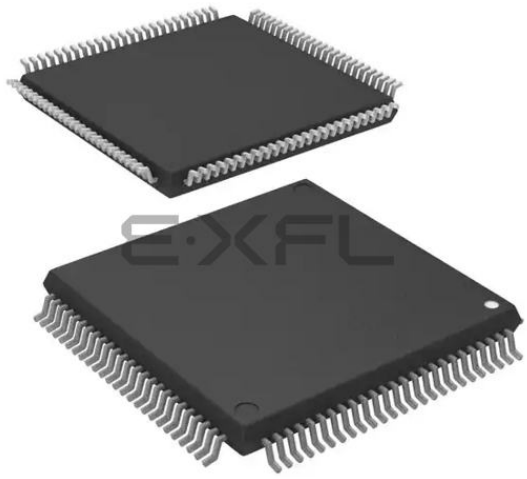
Renesas Electronics America Inc - R5F3640MDFB#UZ Datasheet



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Program Memory Type	-
EEPROM Size	-
RAM Size	-
Voltage - Supply (Vcc/Vdd)	-
Data Converters	-
Oscillator Type	-
Operating Temperature	-
Mounting Type	-
Package / Case	-
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f3640mdfb-uz

Table 4.3 SFR Information (3) (1)

Address	Register	Symbol	After Reset
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h	DMA2 Interrupt Control Register	DM2IC	XXXXX000b
006Ah	DMA3 Interrupt Control Register	DM3IC	XXXXX000b
006Bh	UART5 BUS Collision Detection Interrupt Control Register	U5BCNIC	XXXXX000b
006Ch	UART5 Transmit Interrupt Control Register	S5TIC	XXXXX000b
006Dh	UART5 Receive Interrupt Control Register	S5RIC	XXXXX000b
006Eh	UART6 BUS Collision Detection Interrupt Control Register	U6BCNIC	XXXXX000b
006Fh	UART6 Transmit Interrupt Control Register	S6TIC	XXXXX000b
0070h	UART6 Receive Interrupt Control Register	S6RIC	XXXXX000b
0071h	UART7 BUS Collision Detection Interrupt Control Register	U7BCNIC	XXXXX000b
0072h	UART7 Transmit Interrupt Control Register	S7TIC	XXXXX000b
0073h	UART7 Receive Interrupt Control Register	S7RIC	XXXXX000b
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			
0080h			
0081h			
0082h			
0083h			
0084h			
0085h			
0086h			
0087h			
0088h			
0089h			
008Ah			
008Bh			
008Ch			
008Dh			
008Eh			
008Fh			
0090h			
0091h			
0092h			
0093h			
0094h			
0095h			
0096h			
0097h			
0098h			
0099h			
009Ah			
009Bh			
009Ch			
009Dh			
009Eh			
009Fh to 015Fh			

Note: X: Undefined

1. The blank areas are reserved and cannot be accessed by users.

5.6 Internal Space

Figure 5.3 shows CPU Register Status After Reset. Refer to **4. "Special Function Registers (SFRs)"** for SFR states after reset.

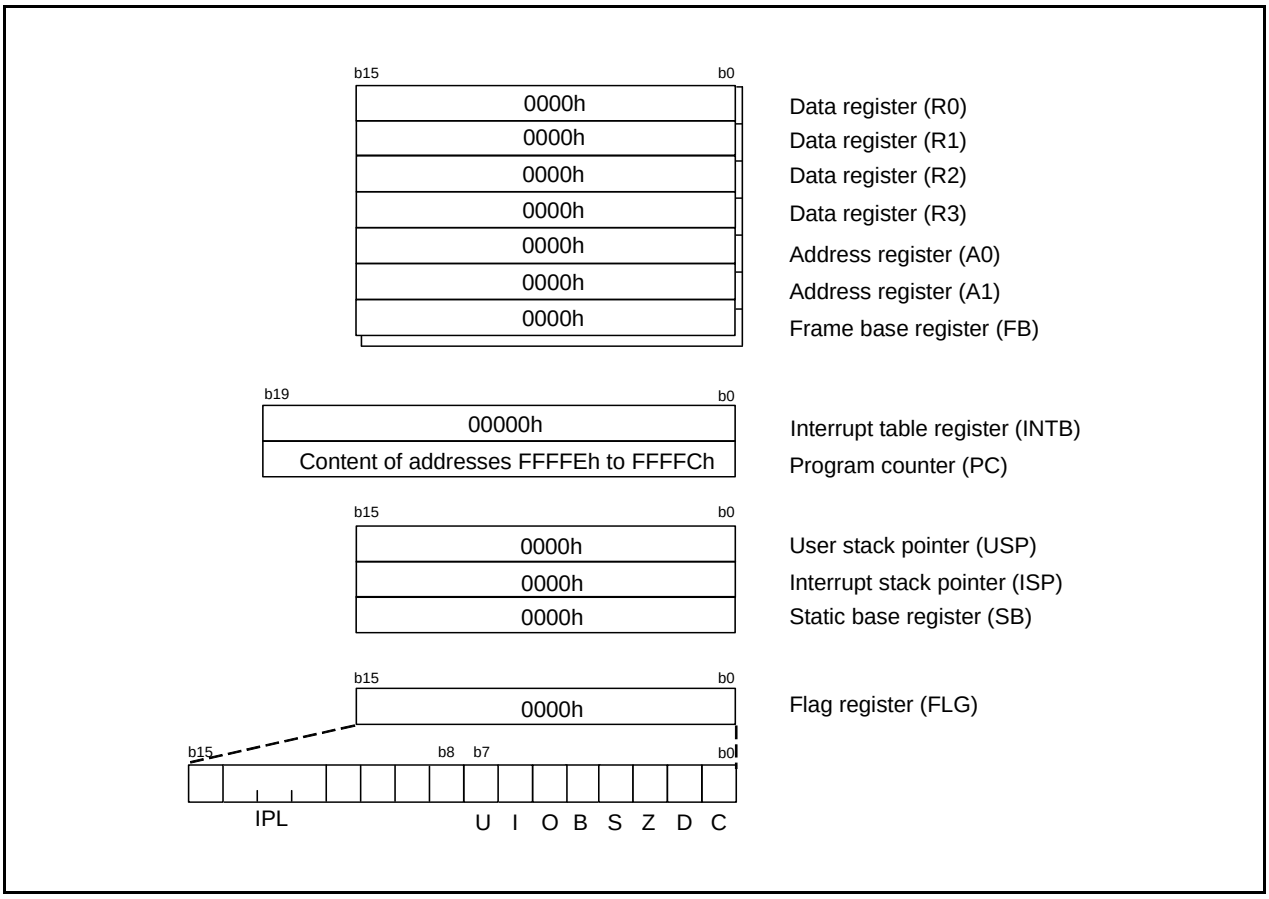
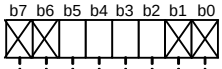


Figure 5.3 CPU Register Status After Reset

Data Bank Register (1)



Symbol	Address	After Reset
DBR	000Bh	00h

Bit Symbol	Bit Name	Function	RW
— (b1-b0)	No register bits. If necessary, set to 0. Read as 0		—
OFS	Offset bit	0 : Not offset 1 : Offset	RW
BSR0	Bank selection bits	b5 b4 b3 0 0 0 : Bank 0 0 1 0 : Bank 2 1 0 0 : Bank 4 1 1 0 : Bank 6 b5 b4 b3 0 0 1 : Bank 1 0 1 1 : Bank 3 1 0 1 : Bank 5 1 1 1 : Bank 7	RW
BSR1			RW
BSR2			RW
— (b7-b6)	No register bits. If necessary, set to 0. Read as 0		—

Note :
1. Effective when bits PM01 and PM00 in the PM0 register are set to 01b (memory expansion mode) or 11b (microprocessor mode).

Figure 9.1 DBR Register

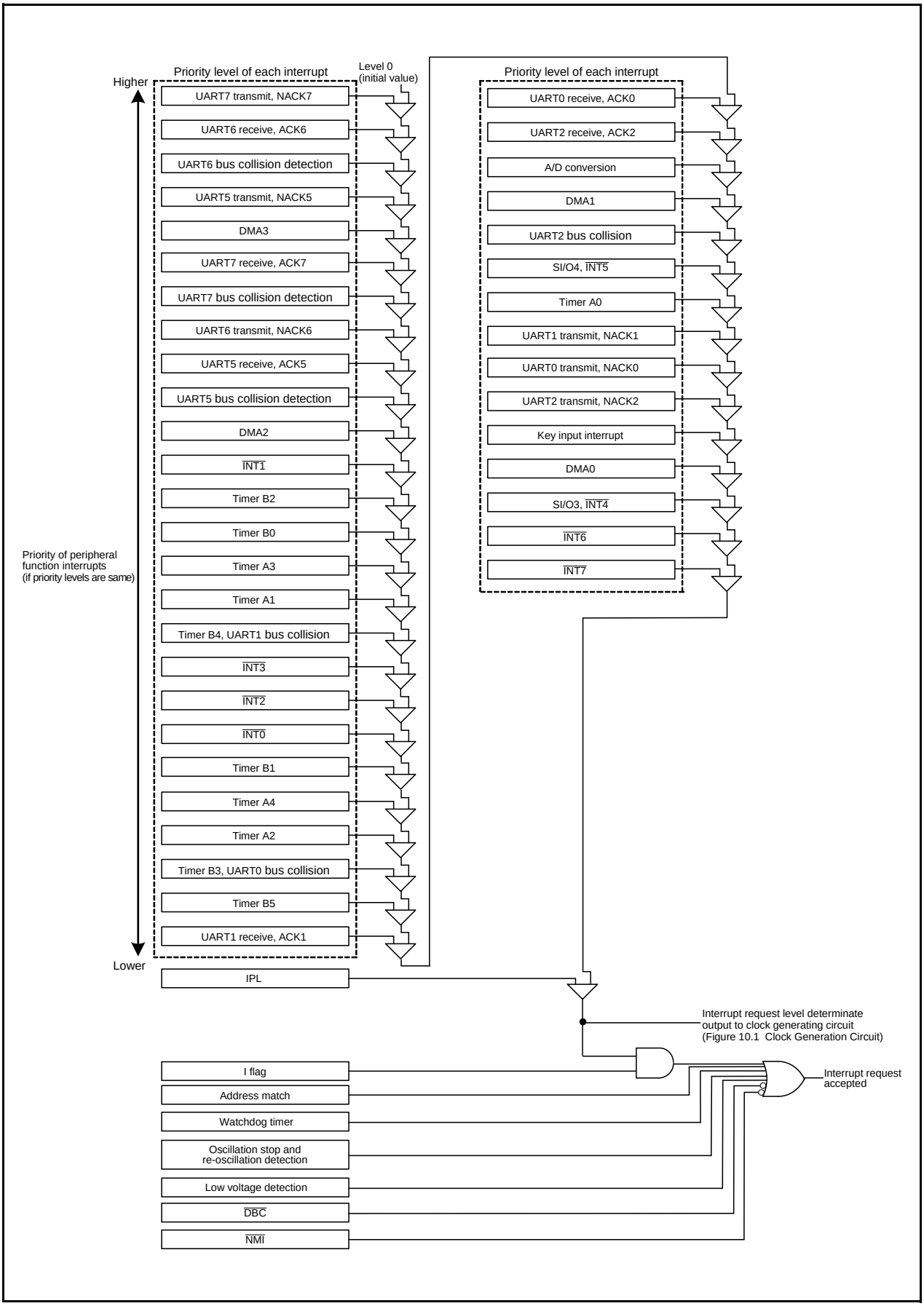


Figure 12.10 Interrupts Priority Select Circuit

Count Source Protection Mode Register

b7	b6	b5	b4	b3	b2	b1	b0	Symbol	Address	After Reset (1)
	0	0	0	0	0	0	0	CSPR	037Ch	00h

Bit Symbol	Bit Name	Function	RW
— (b6-b0)	Reserved bits	Set to 0	RW
CSPRO	Count source protection mode select bit (2)	0 : Count source protection mode disabled 1 : Count source protection mode enabled	RW

Notes :
1. When a 0 is written to the CSPROINI bit in the OFS1 address, 10000000b is set after reset.
2. Write a 0 and then a 1 to set the CSPRO bit to 1. 0 cannot be set in a program.

Optional Feature Select Address (1, 5)

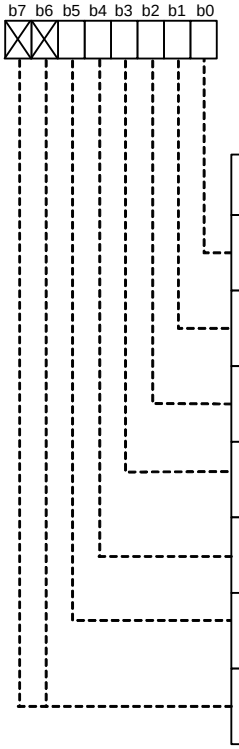
b7	b6	b5	b4	b3	b2	b1	b0	Symbol	Address	After Reset
	1	1	1		1	1		OFS1	FFFFFh	FFh (2)

Bit Symbol	Bit Name	Function	RW
WDTON	Watchdog timer start select bit (3, 4)	0 : Watchdog timer starts automatically after reset 1 : Watchdog timer is in a stopped state after reset	RW
— (b2-b1)	Reserved bits	Set to 1	RW
ROMCP1	ROM code protection bit	0 : ROM code protection enabled 1 : ROM code protection disabled	RW
— (b6-b4)	Reserved bits	Set to 1	RW
CSPROINI	After-reset count source protection mode select bit (3)	0 : Count source protection mode enabled after reset 1 : Count source protection mode disabled after reset	RW

Notes :
1. The OFS1 address exists in flash memory. Set the values when writing a program.
2. The OFS1 address is set to FFh when a block including the OFS1 address is erased.
3. Set the WDTON bit to 0 (watchdog timer starts automatically after reset) when setting the CSPROINI bit to 0 (count source protection mode enabled after reset).
4. This function is also effective in user boot mode.
5. The OFS1 address can be set in single-chip and memory expansion mode. The OFS1 address cannot be used in micro microprocessor mode. Before using the OFS1 address, clear the internal ROM.

Figure 13.3 CSPR Register and OFS1 Address

DMAi Control Register (i = 0 to 3)



Symbol	Address	After Reset
DM0CON	018Ch	00000X00b
DM1CON	019Ch	00000X00b
DM2CON	01ACh	00000X00b
DM3CON	01BCh	00000X00b

Bit Symbol	Bit Name	Function	RW
DMBIT	Transfer unit bit select bit	0 : 16 bits 1 : 8 bits	RW
DMASL	Repeat transfer mode select bit	0 : Single transfer 1 : Repeat transfer	RW
DMAS	DMA request bit	0 : DMA not requested 1 : DMA requested	RW (1)
DMAE	DMA enable bit	0 : Disabled 1 : Enabled	RW
DSD	Source address direction select bit (2)	0 : Fixed 1 : Forward	RW
DAD	Destination address direction select bit (2)	0 : Fixed 1 : Forward	RW
— (b7-b6)	No register bits. If necessary, set to 0. Read as 0		—

Notes :
1. The DMAS bit can be set to 0 by writing a 0 in a program (This bit remains unchanged even if 1 is written).
2. Set at least either the DAD bit or DSD bit to 0 (address direction fixed).

Figure 14.3 Registers DM0CON, DM1CON, DM2CON, and DM3CON

16. Three-Phase Motor Control Timer Function

Timers A1, A2, A4, and B2 can be used to output three-phase motor drive waveforms. Table 16.1 lists the Three-phase Motor Control Timer Functions Specifications. Figure 16.1 shows the Three-phase Motor Control Timer Functions Block Diagram. Also, the related registers are shown on Figures 16.2 to 16.7.

Table 16.1 Three-phase Motor Control Timer Functions Specifications

Item	Specification
Three-Phase Waveform Output Pin	Six pins (U, $\overline{U}$, V, $\overline{V}$, W, $\overline{W}$)
Forced Cutoff Input (1)	Input “L” to the $\overline{SD}$ pin
Used Timers	Timer A4, A1, A2 (used in one-shot timer mode) Timer A4: U- and $\overline{U}$-phase waveform control Timer A1: V- and $\overline{V}$-phase waveform control Timer A2: W- and $\overline{W}$-phase waveform control Timer B2 (used in timer mode) Carrier wave cycle control Dead time timer (3 eight-bit timers and shared reload register) Dead time control
Output Waveform	Triangular wave modulation, sawtooth wave modulation • Enable to output “H” or “L” for one cycle • Enable to set positive-phase level and negative-phase level independently
Carrier Wave Cycle	Triangular wave modulation : count source x (m + 1) x 2 Sawtooth wave modulation : count source x (m + 1) m: setting value of the TB2 register, 0000h to FFFFh Count source: f1TIMAB, f2TIMAB, f8TIMAB, f32TIMAB, f64TIMAB, fOCO-S, fC32
Three-Phase PWM Output Width	Triangular wave modulation: count source x n x 2 Sawtooth wave modulation: count source x n n: setting value of registers TA4, TA1, and TA2 (of registers TA4, TA41, TA1, TA11, TA2, and TA21 when setting the INV11 bit to 1), 0001h to FFFFh Count source: f1TIMAB, f2TIMAB, f8TIMAB, f32TIMAB, f64TIMAB, fOCO-S, fC32
Dead Time	Count source x p, or no dead time p: setting value of the DTT register, 01h to FFh Count source: f1TIMAB, f2TIMAB, f1TIMAB divided by 2, f2TIMAB divided by 2
Active Level	Enable to select “H” or “L”
Positive and Negative-Phase Concurrent Active Disable Function	Positive-and negative-phases concurrent active disable function Positive-and negative-phases concurrent active detect function
Interrupt Frequency	Timer B2 interrupt is generated every q times q: carrier wave cycle-to-cycle basis, 1 to 15

Notes:
1. Forced cutoff with $\overline{SD}$ input is effective when the IVPCR1 bit in the TB2SC register is set to 1 (three-phase output forcible cutoff by $\overline{SD}$ input enabled). If an “L” signal is applied to the $\overline{SD}$ pin when the IVPCR1 bit is 1, the related pins go to a high-impedance state regardless of which functions of those pins are being used.
2. Related pins: P7_2/CLK2/TA1OUT/V, P7_3/$\overline{CTS2}$/$\overline{RTS2}$/TA1IN/$\overline{V}$, P7_4/TA2OUT/W, P7_5/TA2IN/$\overline{W}$, P8_0/TA4OUT/RXD5/SCL5/U, P8_1/TA4IN/$\overline{CTS5}$/$\overline{RTS5}$/$\overline{U}$

17.1.2.6 $\overline{CTS}$ / $\overline{RTS}$ Function

The $\overline{CTS}$ function is used to start transmit operation when “L” is applied to the $\overline{CTSi}$ / $\overline{RTSi}$ (i = 0 to 2, 5 to 7) pin. Transmit operation begins when the $\overline{CTSi}$ / $\overline{RTSi}$ pin is held “L”. If the “L” signal is switched to “H” during a transmit operation, the operation stops after the ongoing transmit / receive operation is completed.

When the $\overline{RTS}$ function is used, the $\overline{CTSi}$ / $\overline{RTSi}$ pin outputs “L” when the microcomputer is ready to receive. The output level becomes “H” when a start bit is detected.

- The CRD bit in the UiC0 register = 1 (disable $\overline{CTS}$ / $\overline{RTS}$ function) — $\overline{CTSi}$ / $\overline{RTSi}$ pin is programmable I/O function
- The CRD bit = 0, the CRS bit = 0 ($\overline{CTS}$ function is selected) — $\overline{CTSi}$ / $\overline{RTSi}$ pin is $\overline{CTS}$ function
- The CRD bit = 0, the CRS bit = 1 ($\overline{RTS}$ function is selected) — $\overline{CTSi}$ / $\overline{RTSi}$ pin is $\overline{RTS}$ function

17.1.2.7 $\overline{CTS}$ / $\overline{RTS}$ Separate Function (UART0)

This function separates $\overline{CTS0}$ / $\overline{RTS0}$, outputs $\overline{RTS0}$ from the P6_0 pin, and inputs $\overline{CTS0}$ from the P6_4 pin. To use this function, set the register bits as shown below.

- The CRD bit in the U0C0 register = 0 (enable $\overline{CTS}$ / $\overline{RTS}$ of UART0)
- The CRS bit in the U0C0 register = 1 (output $\overline{RTS}$ of UART0)
- The CRD bit in the U1C0 register = 0 (enable $\overline{CTS}$ / $\overline{RTS}$ of UART1)
- The CRS bit in the U1C0 register = 0 (input $\overline{CTS}$ of UART1)
- The RCSP bit in the UCON register = 1 (inputs $\overline{CTS0}$ from the P6_4 pin)
- The CLKMD1 bit in the UCON register = 0 (CLKS1 not used)

Note that when using the $\overline{CTS}$ / $\overline{RTS}$ separate function, $\overline{CTS}$ / $\overline{RTS}$ of UART1 function cannot be used.

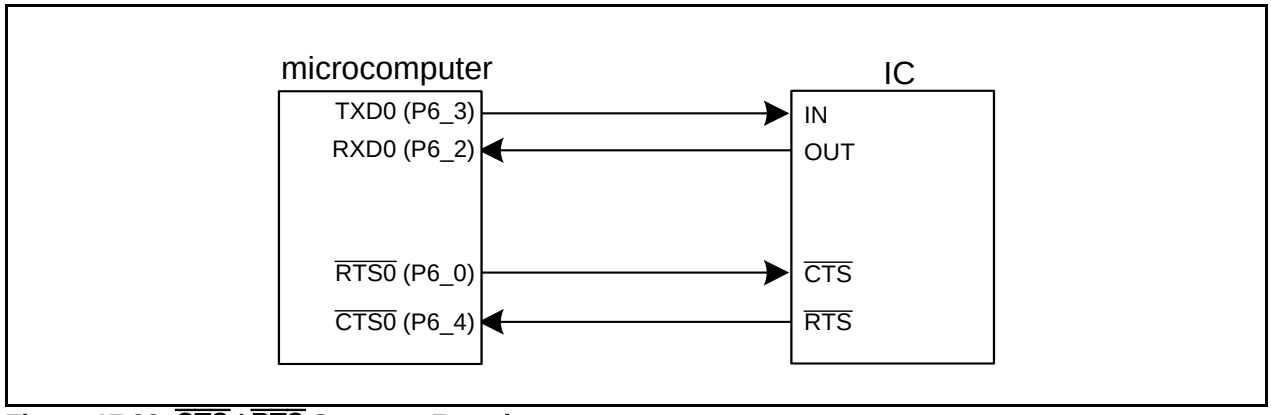


Figure 17.23 $\overline{CTS}$ / $\overline{RTS}$ Separate Function

18.1.2 Repeat Mode

In repeat mode, analog voltage applied to a selected pin is repeatedly converted to a digital code. Table 18.3 shows the Repeat Mode Specifications. Figure 18.5 shows the Registers ADCON0 and ADCON1 (Repeat Mode).

Table 18.3 Repeat Mode Specifications

Item	Specification
Function	Bits CH2 to CH0 in the ADCON0 register and bits ADGSEL1 and ADGSEL0 in the ADCON2 register, or bits ADEX1 and ADEX0 in the ADCON1 register select a pin. Analog voltage applied to this pin is repeatedly converted to a digital code.
A/D Conversion Start Condition	• When the TRG bit in the ADCON0 register is 0 (software trigger) the ADST bit in the ADCON0 register is set to 1 (A/D conversion start) • When the TRG bit is 1 ($\overline{\text{ADTRG}}$ trigger) input on the $\overline{\text{ADTRG}}$ pin changes state from high to low after the ADST bit is set to 1 (A/D conversion start)
A/D Conversion Stop Condition	Set the ADST bit to 0 (A/D conversion stop)
Interrupt Request Generation timing	No interrupt requests generated
Analog Input Pin	Select one pin from AN0 to AN7, AN0_0 to AN0_7, AN2_0 to AN2_7, ANEX0, and ANEX1
Reading of Result of A/D Converter	Read one of the registers AD0 to AD7 that corresponds to the selected pin

18.2 Conversion Rate

The conversion rate is defined as follows.
Start dummy time depends on which ϕAD is selected. Table 18.7 shows Start Dummy Time. When the ADST bit in the ADCON0 register is set to 1 (A/D conversion start), A/D conversion starts after start dummy time elapses. 0 (A/D conversion stop) is read if the ADST bit is read before A/D conversion starts.
For multiple pins or A/D conversion repeat mode, for each pin, between-execution dummy time is inserted between A/D conversion execution time and the next A/D conversion execution time.
The ADST bit is set to 0 during the end dummy time, and the last A/D conversion result is set to the ADi register in one-shot mode and single sweep mode.

While in one-shot mode:
Start dummy time + A/D conversion execution time + end dummy time

When two pins are selected while in single sweep mode:
Start dummy time + (A/D conversion execution time + between-execution dummy time + A/D conversion execution time) + end dummy time

Start dummy time: See **Table 18.7 “Start Dummy Time”**
A/D conversion execution time: 40 ϕAD cycles per pin
Between-execution dummy time: 1 ϕAD cycle
End dummy time: 2 to 3 cycles of fAD

Table 18.7 Start Dummy Time

ϕAD Selection	Start Dummy Time
fAD	1 to 2 cycles of fAD
fAD divided by 2	2 to 3 cycles of fAD
fAD divided by 3	3 to 4 cycles of fAD
fAD divided by 4	3 to 4 cycles of fAD
fAD divided by 6	4 to 5 cycles of fAD
fAD divided by 12	7 to 8 cycles of fAD

18.3 Extended Analog Input Pins

In one-shot and repeat modes, pins ANEX0 and ANEX1 can be used as analog input pins. Use bits ADEX1 and ADEX0 in the ADCON1 register to select whether or not to use ANEX0 and ANEX1.
The A/D conversion results of ANEX0 and ANEX1 inputs are stored in registers AD0 and AD1, respectively.

18.4 Current Consumption Reducing Function

When not using the A/D converter, power consumption can be reduced by setting the ADSTBY bit in the ADCON1 register to 0 (A/D operation stopped: standby) to shut off any analog circuit current flow.
To use the A/D converter, set the ADSTBY bit to 1 (A/D operation enabled) after operating longer than one cycle of a timer count source, and then set the ADST bit in the ADCON0 register to 1 (A/D conversion start). Do not set bits ADST and ADSTBY to 1 at the same time.
Also, do not set the ADSTBY bit to 0 (A/D operation stopped: standby) during A/D conversion.

22. Flash Memory Version

The flash memory can perform in three rewrite modes: CPU rewrite mode, standard serial I/O mode, and parallel I/O mode. Table 22.1 lists specifications of the flash memory version. See Tables 1.1 and 1.2 Specifications Overview for the items not listed in Table 22.1.

Table 22.1 Flash Memory Version Specifications

Item		Specification
Flash Memory Rewrite Mode		3 modes (CPU rewrite, standard serial I/O, parallel I/O)
Erase Block	Program ROM 1	See **Figure 22.1 "Flash Memory Block Diagram"**
	Program ROM 2	1 block (16 Kbytes)
	Data Flash	2 blocks (4 Kbytes each)
Program Method		In units of 2 words
Erase Method		Block erase
Program and Erase Control Method		Program and erase controlled by software command
Protect Method		The lock bit protects each block
Number of Commands		8 commands
Program and Erase Endurance		100 times (1)
Data Retention		10 years
ROM Code Protection		Parallel I/O and standard serial I/O modes are supported

Note:

1. Definition of program and erase endurance
   The program and erase endurance refers to the number of per-block erasures.
   For example, assume a case where a 4 Kbyte block is programmed in 1,024 operations, writing two words at a time, and erased thereafter. In this case, the block is reckoned as having been programmed and erased once. If the program and erase endurance is 100 times, each block can be erased up to 100 times.

Table 22.2 Flash Memory Rewrite Modes Overview

Flash Memory Rewrite Mode	CPU rewrite Mode (1)	Standard Serial I/O Mode	Parallel I/O Mode
Function	Program ROM 1, program ROM 2, and data flash are rewritten when the CPU executes software commands. EW0 mode: Rewritable in areas other than flash memory (2) EW1 mode: Rewritable in the flash memory	Program ROM 1, program ROM 2, and data flash are rewritten using a dedicated serial programmer. Standard serial I/O mode 1: clock synchronous serial I/O Standard serial I/O mode 2: clock asynchronous serial I/O Standard serial I/O mode 3: special clock asynchronous serial I/O	Program ROM 1, program ROM 2 and data flash are rewritten using a dedicated parallel programmer.
Areas Which Can Be Rewritten	Program ROM 1, program ROM 2, and data flash	Program ROM 1, program ROM 2, and data flash	Program ROM 1, program ROM 2, and data flash
Operating Mode	Single-chip mode Memory expansion mode (EW0 mode)	Boot mode	Parallel I/O mode
ROM Programmer	None	Serial programmer	Parallel programmer

Notes:

1. The PM13 bit remains set to 1 while the FMR01 bit in the FMR0 register = 1 (CPU rewrite mode enabled). The PM13 bit is reverted to its original value by clearing the FMR01 bit to 0 (CPU rewrite mode disabled). However, if the PM13 bit is changed during CPU rewrite mode, its changed value is not reflected until after the FMR01 bit is cleared to 0.
2. In CPU rewrite mode, bits PM10 and PM13 in the PM1 register are set to 1. The rewrite control program can only be executed in the internal RAM or in an external area that is enabled for use when the PM10 bit and PM13 bit are 1. When the PM13 bit = 0 and the flash memory is used in 4-Mbyte mode, the extended accessible area (40000h to BFFFFh) cannot be used.

22.3 CPU Rewrite Mode

In CPU rewrite mode, the flash memory can be rewritten when the CPU executes software commands. Program ROM 1, program ROM 2, and the data flash can be rewritten with the microcomputer mounted on a board without using a ROM programmer.

The program and block erase commands are executed only in each block area of program ROM 1, program ROM 2, and the data flash.

Erase-write 0 (EW0) mode and erase-write 1 (EW1) mode are provided as CPU rewrite mode. Table 22.9 lists differences between erase-write 0 (EW0) and erase-write 1 (EW1) modes.

Table 22.9 EW0 Mode and EW1 Mode

Item	EW0 Mode	EW1 Mode
Operating Mode	• Single-chip mode • Memory expansion mode	Single-chip mode
Rewrite Control Program Allocatable Area	• Program ROM 1 • Program ROM 2 • External memory area	• Program ROM 1 • Program ROM 2
Rewrite Control Program Executable Area	The rewrite control program must be transferred to any area other than the flash memory (e.g., RAM) before being executed (2)	The rewrite control program can be executed in program ROM 1 and program ROM 2.
Rewritable Area	• Program ROM 1 • Program ROM 2 • Data flash	Program ROM 1, program ROM 2, and data flash, excluding blocks with the rewrite control program
Software Command Restriction	None	• Program and block erase commands cannot be executed in a block having the rewrite control program. • Read status register command cannot be used.
Mode after Program or Erase	Read status register mode	Read array mode
CPU State during Auto Write and Auto Erase	Operating	Maintains hold state (I/O ports maintains the state before the command execution) (1)
Flash Memory Status Detection	• Read bits FMR00, FMR06, and FMR07 in the FMR0 register by program • Execute the read status register command to read bits SR7, SR5, and SR4 in the status register.	Read bits FMR00, FMR06, and FMR07 in the FMR0 register by program

Notes:
1. Do not generate an interrupt (except $\overline{\text{NMI}}$ interrupt) or start a DMA transfer.
2. When in CPU rewrite mode, bits PM10 and PM13 in the PM1 register are set to 1. The rewrite control program can only be executed in the internal RAM or in an external area that is enabled for use when the PM10 bit and PM13 bit are 1. When the PM13 bit = 0 and the flash memory is used in 4-Mbyte mode, the extended accessible area (40000h to BFFFFh) cannot be used.

VCC1=VCC2=5V

Timing Requirements
(VCC1 = VCC2 = 5V, VSS = 0V, at Topr = –20 to 85°C/-40 to 85°C unless otherwise specified)

Table 23.13 Timer A Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TA)	TAiIN Input Cycle Time	100		ns
tw(TAH)	TAiIN Input HIGH Pulse Width	40		ns
tw(TAL)	TAiIN Input LOW Pulse Width	40		ns

Table 23.14 Timer A Input (Gating Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TA)	TAiIN Input Cycle Time	400		ns
tw(TAH)	TAiIN Input HIGH Pulse Width	200		ns
tw(TAL)	TAiIN Input LOW Pulse Width	200		ns

Table 23.15 Timer A Input (External Trigger Input in One-shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TA)	TAiIN Input Cycle Time	200		ns
tw(TAH)	TAiIN Input HIGH Pulse Width	100		ns
tw(TAL)	TAiIN Input LOW Pulse Width	100		ns

Table 23.16 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tw(TAH)	TAiIN Input HIGH Pulse Width	100		ns
tw(TAL)	TAiIN Input LOW Pulse Width	100		ns

Table 23.17 Timer A Input (Two-phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TA)	TAiIN Input Cycle Time	800		ns
tsu(TAIN-TAOUT)	TAiOUT Input Setup Time	200		ns
tsu(TAOUT-TAIN)	TAiIN Input Setup Time	200		ns

VCC1=VCC2=5V

Switching Characteristics
(VCC1 = VCC2 = 5V, VSS = 0V, at Topr = –20 to 85°C/-40 to 85°C unless otherwise specified)

Table 23.26 Memory Expansion and Microprocessor Modes (for 1- to 3-wait setting, external area access and multiplex bus selection)(5)

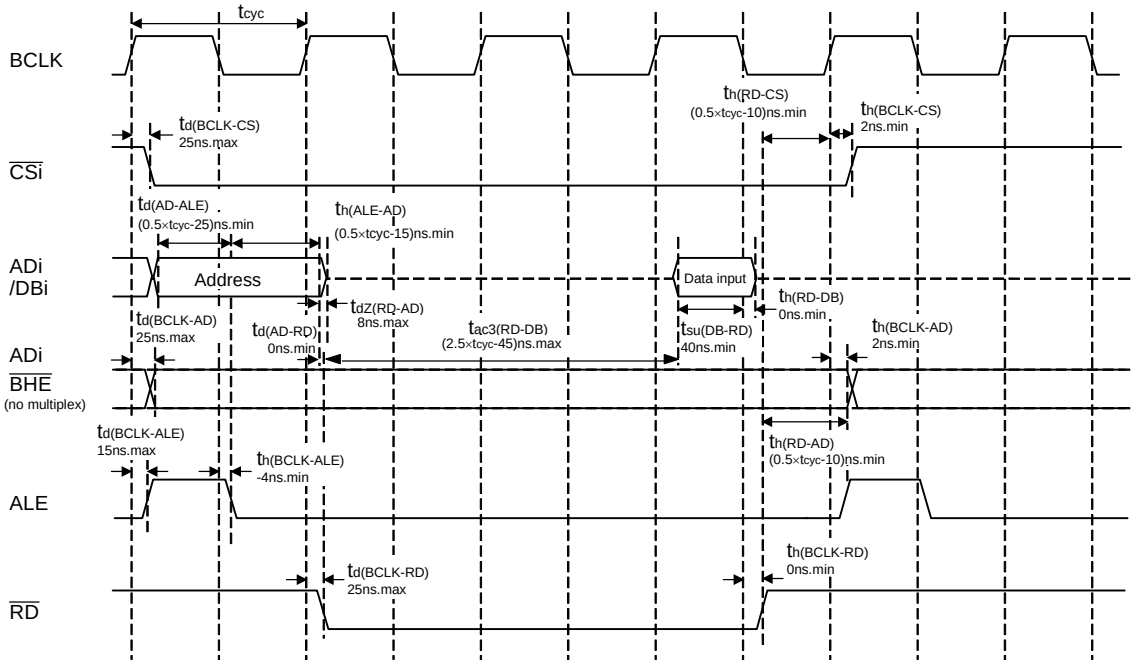
Symbol	Parameter	Measuring Condition	Standard		Unit
			Min.	Max.	
td(BCLK-AD)	Address Output Delay Time	See Figure 23.2		25	ns
th(BCLK-AD)	Address Output Hold Time (in relation to BCLK)		2		ns
th(RD-AD)	Address Output Hold Time (in relation to RD)		(NOTE 1)		ns
th(WR-AD)	Address Output Hold Time (in relation to WR)		(NOTE 1)		ns
td(BCLK-CS)	Chip Select Output Delay Time			25	ns
th(BCLK-CS)	Chip Select Output Hold Time (in relation to BCLK)		2		ns
th(RD-CS)	Chip Select Output Hold Time (in relation to RD)		(NOTE 1)		ns
th(WR-CS)	Chip Select Output Hold Time (in relation to WR)		(NOTE 1)		ns
td(BCLK-RD)	RD Signal Output Delay Time			25	ns
th(BCLK-RD)	RD Signal Output Hold Time		0		ns
td(BCLK-WR)	WR Signal Output Delay Time			25	ns
th(BCLK-WR)	WR Signal Output Hold Time		0		ns
td(BCLK-DB)	Data Output Delay Time (in relation to BCLK)			40	ns
th(BCLK-DB)	Data Output Hold Time (in relation to BCLK)		2		ns
td(DB-WR)	Data Output Delay Time (in relation to WR)		(NOTE 2)		ns
th(WR-DB)	Data Output Hold Time (in relation to WR)		(NOTE 1)		ns
td(BCLK-HLDA)	$\overline{\text{HLDA}}$ Output Delay Time			40	ns
td(BCLK-ALE)	ALE Signal Output Delay Time (in relation to BCLK)			15	ns
th(BCLK-ALE)	ALE Signal Output Hold Time (in relation to BCLK)		–4		ns
td(AD-ALE)	ALE Signal Output Delay Time (in relation to Address)		(NOTE 3)		ns
th(AD-ALE)	ALE Signal Output Hold Time (in relation to Address)		(NOTE 4)		ns
td(AD-RD)	RD Signal Output Delay From the End of Address		0		ns
td(AD-WR)	WR Signal Output Delay From the End of Address		0		ns
tdz(RD-AD)	Address Output Floating Start Time			8	ns

Notes:
1. Calculated according to the BCLK frequency as follows:
$$\frac{0.5 \times 10^9}{f(BCLK)} - 10[ns]$$
2. Calculated according to the BCLK frequency as follows:
$$\frac{(n-0.5) \times 10^9}{f(BCLK)} - 40[ns]$$ n is “2” for 2-wait setting, “3” for 3-wait setting.
3. Calculated according to the BCLK frequency as follows:
$$\frac{0.5 \times 10^9}{f(BCLK)} - 25[ns]$$
4. Calculated according to the BCLK frequency as follows:
$$\frac{0.5 \times 10^9}{f(BCLK)} - 15[ns]$$
5. When using multiplex bus, set f(BCLK) 12.5MHz or less.

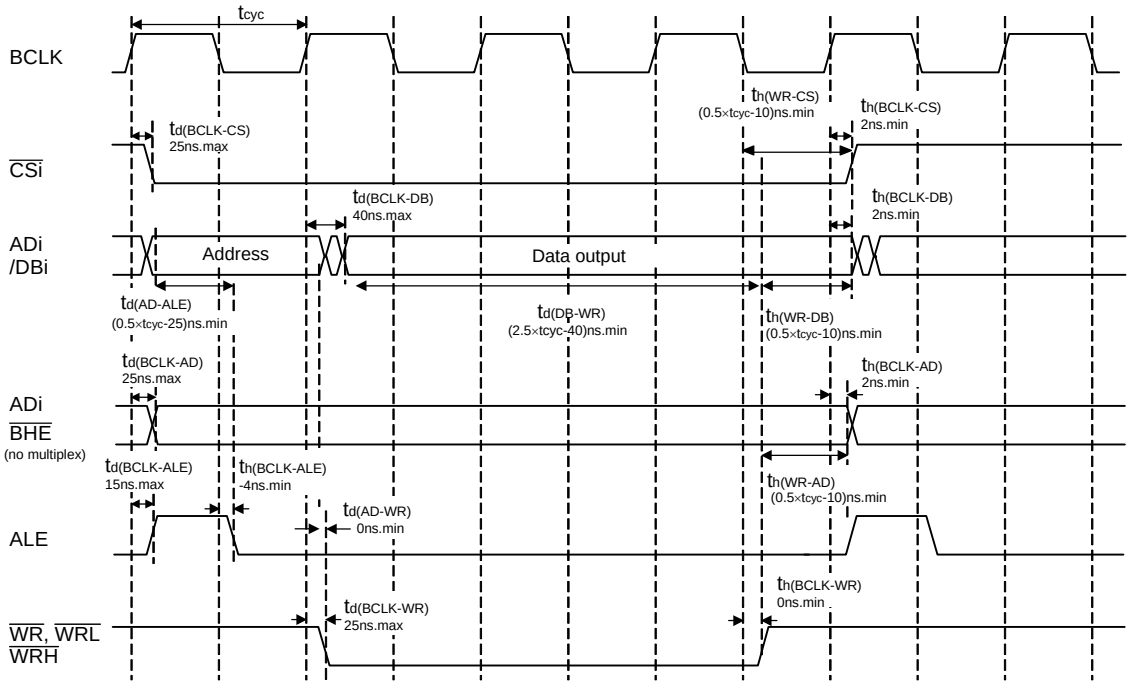
$V_{CC1}=V_{CC2}=5V$

Memory Expansion Mode, Microprocessor Mode
(For 3-wait setting, external area access and multiplex bus selection**)**

Read timing



Write timing



$$t_{cyc}=\frac{1}{f(BCLK)}$$

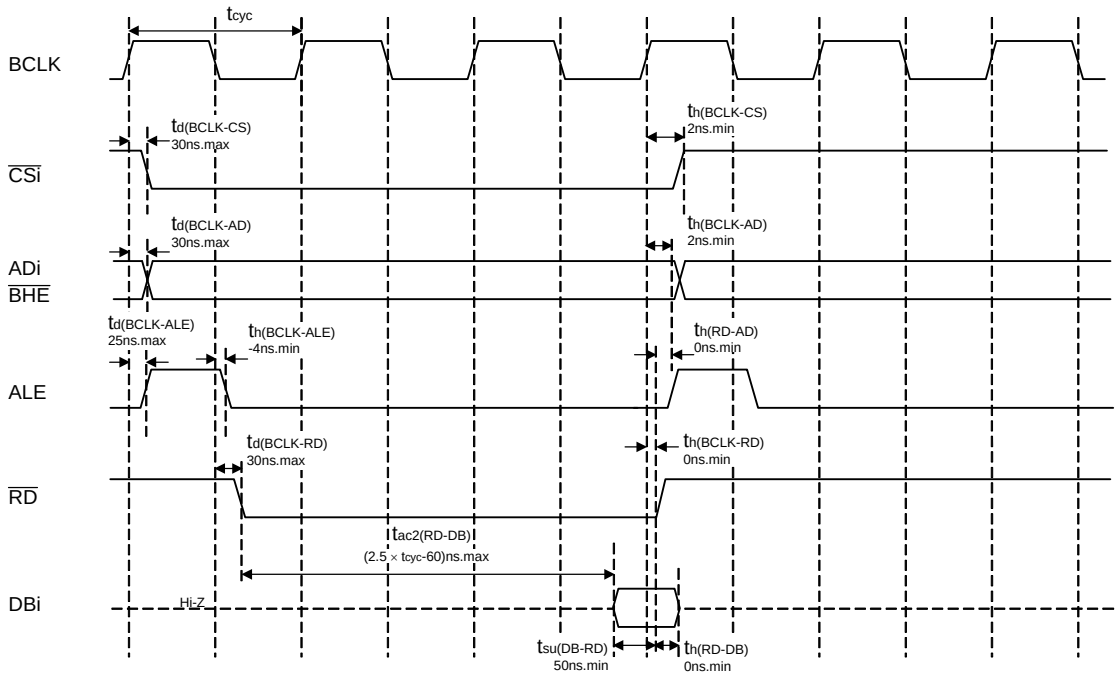
Measuring conditions
- $V_{CC1}=V_{CC2}=5V$
- Input timing voltage : $V_{IL}=0.8V$, $V_{IH}=2.0V$
- Output timing voltage : $V_{OL}=0.4V$, $V_{OH}=2.4V$

Figure 23.11 Timing Diagram (9)

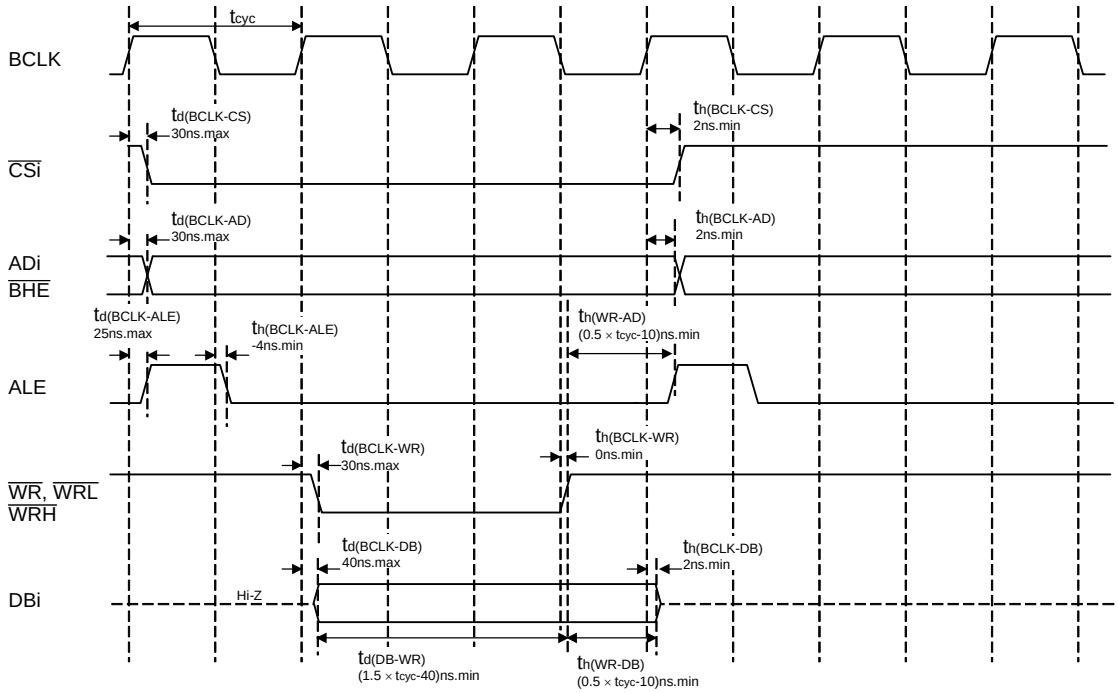
$V_{CC1}=V_{CC2}=3V$

Memory Expansion Mode, Microprocessor Mode
(for 2-wait setting and external area access**)**

Read timing



Write timing



$$t_{cyc}=\frac{1}{f(BCLK)}$$

Measuring conditions
- $V_{CC1}=V_{CC2}=3V$
- Input timing voltage : $V_{IL}=0.6V$, $V_{IH}=2.4V$
- Output timing voltage : $V_{OL}=1.5V$, $V_{OH}=1.5V$

Figure 23.18 Timing Diagram (6)

24.6 Protect

Set the PRC2 bit to 1 (write enabled) and then write to given SFR address, and the PRC2 bit will be cleared to 0 (write protected). Change the registers protected by the PRC2 bit in the next instruction after setting the PRC2 bit to 1. Make sure no interrupts or DMA transfers will occur between the instruction in which the PRC2 bit is set to 1 and the next instruction.

24.13.12 Writing

EW0 Mode

- If the power supply voltage drops while rewriting any block in which the rewrite control program is stored, the rewrite control program may not be correctly rewritten and, consequently, the flash memory becomes unable to be rewritten thereafter. In this case, use standard serial I/O or parallel I/O mode.

EW1 Mode

- Avoid rewriting any block in which the rewrite control program is stored.
- When a software command is executed for another block on the flash memory, the software command may not be executed as expected. This may occur when RAM is written by the rewriting program which is executed in EW1 mode.

Example Program (When the program command is executed)

```
PRG_CMD:
        MOV.W   PRG_ADDR    ,   A0          ;
        MOV.W   PRG_ADDR+2  ,   A1          ;
        STE.W   #0041h      ,   [A1A0]      ;   Program command
        STE.W   WR_DATA0    ,   [A1A0]      ;   The first word data to write
        ADD.W   #4          ,   PRG_ADDR    ;   ←Write to RAM
                                                (This is acknowledged as the second
                                                data to write)
        MOV.W   PRG_ADDR    ,   A0          ;
        STE.W   WR_DATA1    ,   [A1A0]      ;   The second word data to write
                                                (Depending on the value of
                                                WR_DATA1, this may be
                                                acknowledged as next software
                                                command)
                    :
                    :
        JMP     PRG_CMD
```

*PRG_ADDR; RAM address (the executing command address to be stored.)

When rewriting flash memory, execute a rewriting program on the area other than flash memory such as RAM or external area in EW0 mode. When using EW1 mode, do not write to RAM in EW1 mode.

24.13.13 DMA transfer

In EW1 mode, make sure that no DMA transfers will occur while the FMR00 bit in the FMR0 register = 0 (during the auto program or auto erase period).

Table Appendix 2.2 Difference Between M16C/64 and M16C/62P (2)

Item	M16C/62P	M16C/64
A/D converter	Operation frequency: 3.3V:f AD = 10MHz(±5LSB) 5.0V:f AD =12MHz(±3LSB)	Operation frequency: 3.0V:f AD =10MHz(±3LSB) 3.3V:f AD =16MHz (±3LSB) 5.0V:f AD =25MHz(±3LSB)
	VREFCUT: Wait 1μs after connecting.	A/D Standby: Start in 1cycle after connecting.
	Selectable 10 bit or 8 bit conversion mode	Fixed 10 bit conversion mode
	Selectable with/without sample and hold function	Fixed sample and hold function
	Available external operational amplifier connection mode	No external operational amplifier connection mode
	Can be used when operating with 2.0V≤VREF≤VCC1	Be sure to use VCC1, AVCC, VREF with same power supply
	ADST bit when using external trigger: After A/D conversion, ADST bit "1" is maintained.	ADST bit when using external trigger: After A/D conversion, ADST bit becomes "0".
	The operation after writing "1" in ADST bit: ADST bit set to "1" shortly.	The operation after writing "1" in ADST bit: After the passage of dummy time period, ADST bit is set to "1".
Timer A, B	Operating clocks: • 1, 2, 8, or 32 in f1 clock • fc32	Operating clocks: • 1, 2, 8, 32, or 64 in f1 clock(one frequency circuit in timer A and B and Three-phase timer) • fc32 • On-chip oscillator (125kHz)
	Fixed PWM output level	PWM output level can be inverted
	Select up count or down count: Selectable with TAjOUT pin (j=0 to 4)	Select up count or down count: Not selectable with TAjout pin (j=0 to 4)
	Timer Bi register (i=0 to 5) in pulse measurement mode / pulse period measurement mode: disable to set the initial value	Timer Bi register (i=0 to 5) in pulse measurement mode / pulse period measurement mode: enable to set the initial value
	Timer B over-flow flag: disable to clear the flag while not counting.	Timer B overflow flag: enable to clear the flag while not counting
	Timer A2 to A4 two-phase pulse signal Processing select bit in up/down flag register is write enable only.	Timer A2 to A4 two-phase pulse signal Processing Select bit in up/down flag register is read and write enable.
Three-phase timer	Three-phase timer output cutoff: $\overline{\text{NMI}}$ pin\	Three-phase timer output cutoff: $\overline{\text{SD}}$ pin
Watchdog timer	Common to start and refresh register	Reset register and Start register are divided. Optional function select address (OFS1) enables select and protect count source.
Serial interface UART	UART3ch (UART 0 to 2)	UART6ch (UART 0 to 2,5 to 7)
	Operating clock: diveded by 1, 2, 8, or 32 in f1 clock	Operating clock: diveded by 1, 2, 8, or 32 (Each UART0 to UART2, UART5 to UART7 has one divider circuit)
SIO	Operating clock: diveded by 1, 2, 8, or 32 in f1 clock	Operating clock: diveded by 1, 2, 8, or 32 in f1 clock (one divider circuit belongs to SI/O3 and SI/O4)
	SOUT output: high impedance	SOUT output: selectable "high impedance" and "last bit level hold" function.