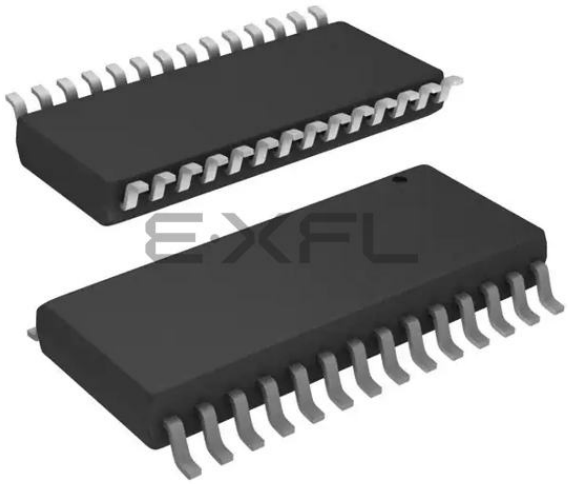

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	30 MIPs
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	21
Program Memory Size	12KB (4K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic30f2020-30i-so

Pin Diagrams

44-PIN QFN

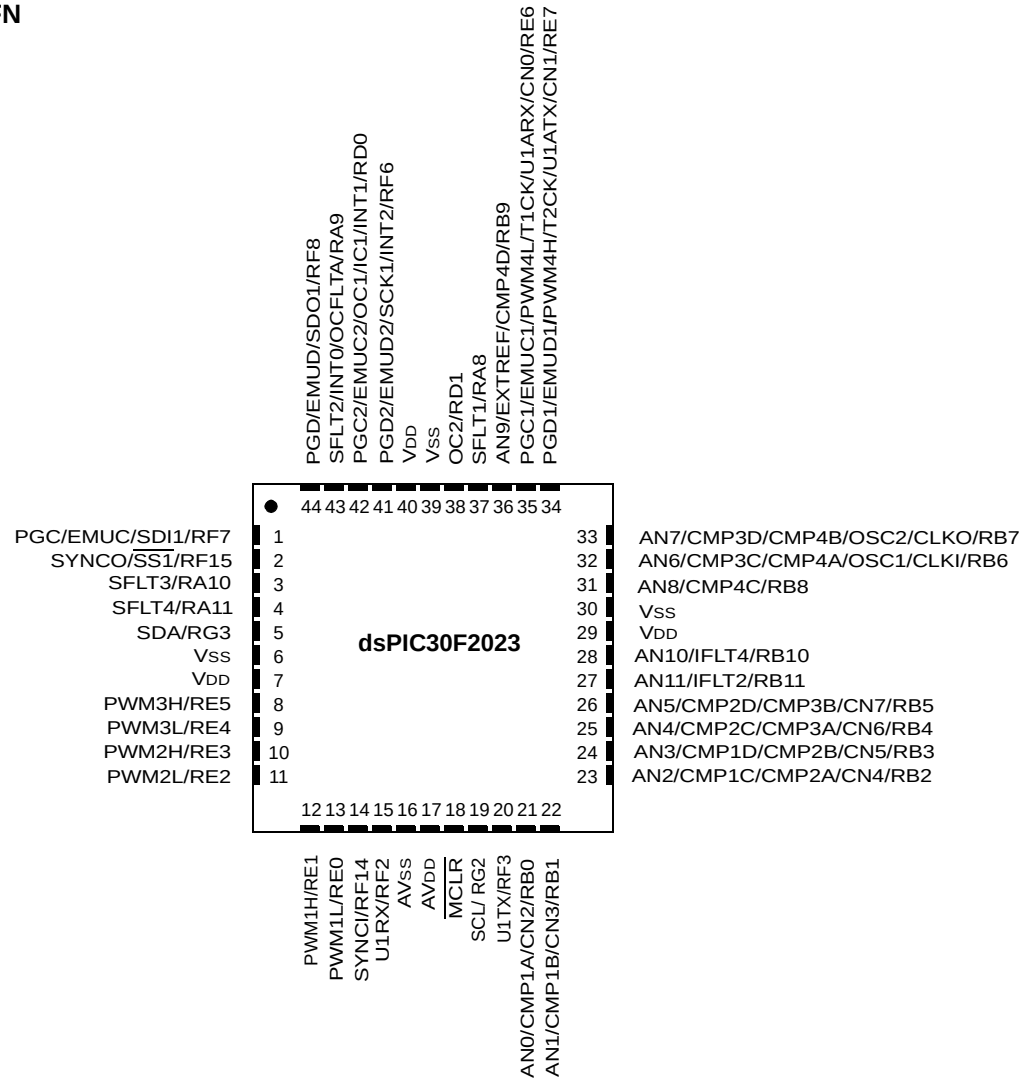


FIGURE 1-2: dsPIC30F2020 BLOCK DIAGRAM

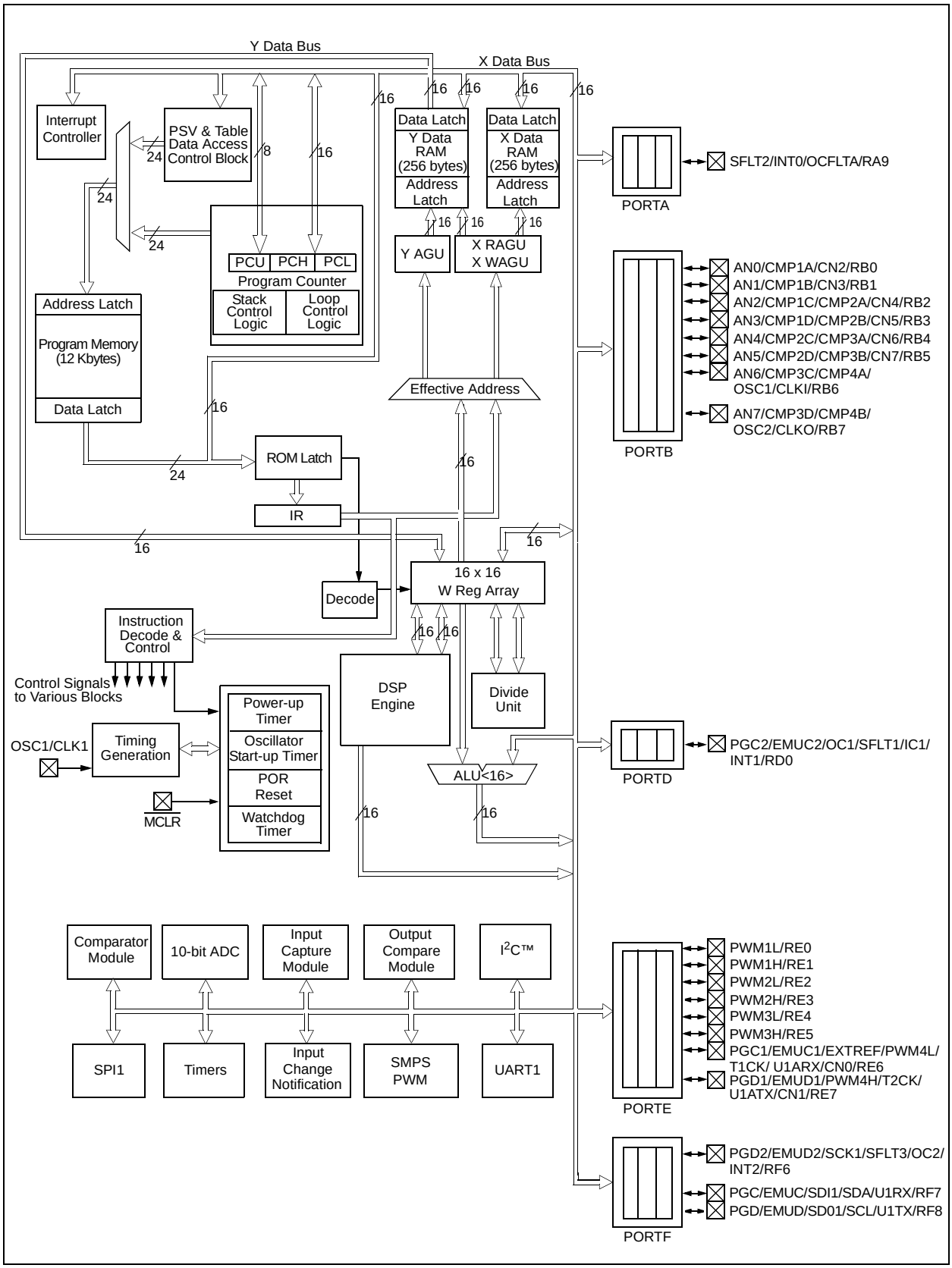


Table 1-2 provides a brief description of device I/O pin-outs for the dsPIC30F2020 and the functions that may be multiplexed to a port pin. Multiple functions may exist on one port pin. When multiplexing occurs, the peripheral module's functional requirements may force an override of the data direction of the port pin.

TABLE 1-2: PINOUT I/O DESCRIPTIONS FOR dsPIC30F2020

Pin Name	Pin Type	Buffer Type	Description
AN0-AN7	I	Analog	Analog input channels.
AVDD	P	P	Positive supply for analog module.
AVSS	P	P	Ground reference for analog module.
CLKI CLKO	I O	ST/CMOS —	External clock source input. Always associated with OSC1 pin function. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSC2 pin function.
EMUD EMUC EMUD1 EMUC1 EMUD2 EMUC2	I/O I/O I/O I/O I/O I/O	ST ST ST ST ST ST	ICD Primary Communication Channel data input/output pin. ICD Primary Communication Channel clock input/output pin. ICD Secondary Communication Channel data input/output pin. ICD Secondary Communication Channel clock input/output pin. ICD Tertiary Communication Channel data input/output pin. ICD Tertiary Communication Channel clock input/output pin.
IC1	I	ST	Capture input.
INT0 INT1 INT2	I I I	ST ST ST	External interrupt 0 External interrupt 1 External interrupt 2
SFLT1 SFLT2 SFLT3 PWM1L PWM1H PWM2L PWM2H PWM3L PWM3H PWM4L PWM4H	I I I O O O O O O O O	ST ST ST — — — — — — — —	Shared Fault Pin 1 Shared Fault Pin 2 Shared Fault Pin 3 PWM 1 Low output PWM 1 High output PWM 2 Low output PWM 2 High output PWM 3 Low output PWM 3 High output PWM 4 Low output PWM 4 High output
$\overline{\text{MCLR}}$	I/P	ST	Master Clear (Reset) input or programming voltage input. This pin is an active low Reset to the device.
OC1-OC2 OCFLTA	O I	— 	Compare outputs. Output Compare Fault pin
OSC1 OSC2	I I/O	CMOS —	Oscillator crystal input. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in FRC and EC modes.
PGD PGC PGD1 PGC1 PGD2 PGC2	I/O I I/O I I/O I	ST ST ST ST ST ST	In-Circuit Serial Programming™ data input/output pin. In-Circuit Serial Programming clock input pin. In-Circuit Serial Programming data input/output pin 1. In-Circuit Serial Programming clock input pin 1. In-Circuit Serial Programming data input/output pin 2. In-Circuit Serial Programming clock input pin 2.

Legend: CMOS = CMOS compatible input or output; Analog = Analog input
ST = Schmitt Trigger input with CMOS levels; O = Output
I = Input; P = Power

4.2.3 MODULO ADDRESSING APPLICABILITY

Modulo addressing can be applied to the Effective Address (EA) calculation associated with any W register. It is important to realize that the address boundaries check for addresses less than or greater than the upper (for incrementing buffers) and lower (for decrementing buffers) boundary addresses (not just equal to). Address changes may, therefore, jump beyond boundaries and still be adjusted correctly.

Note:	The modulo corrected effective address is written back to the register only when Pre-Modify or Post-Modify Addressing mode is used to compute the Effective Address. When an address offset (e.g., [W7 + W2]) is used, modulo address correction is performed, but the contents of the register remains unchanged.

4.3 Bit-Reversed Addressing

Bit-Reversed Addressing is intended to simplify data re-ordering for radix-2 FFT algorithms. It is supported by the X AGU for data writes only.

The modifier, which may be a constant value or register contents, is regarded as having its bit order reversed. The address source and destination are kept in normal order. Thus, the only operand requiring reversal is the modifier.

4.3.1 BIT-REVERSED ADDRESSING IMPLEMENTATION

Bit-Reversed Addressing is enabled when:

1. BWM (W register selection) in the MODCON register is any value other than 15 (the stack can not be accessed using Bit-Reversed Addressing) **and**
2. the BREN bit is set in the XBREV register **and**
3. the Addressing mode used is Register Indirect with Pre-Increment or Post-Increment.

If the length of a bit-reversed buffer is $M = 2^N$ bytes, then the last 'N' bits of the data buffer start address must be zeros.

XB<14:0> is the bit-reversed address modifier or 'pivot point' which is typically a constant. In the case of an FFT computation, its value is equal to half of the FFT data buffer size.

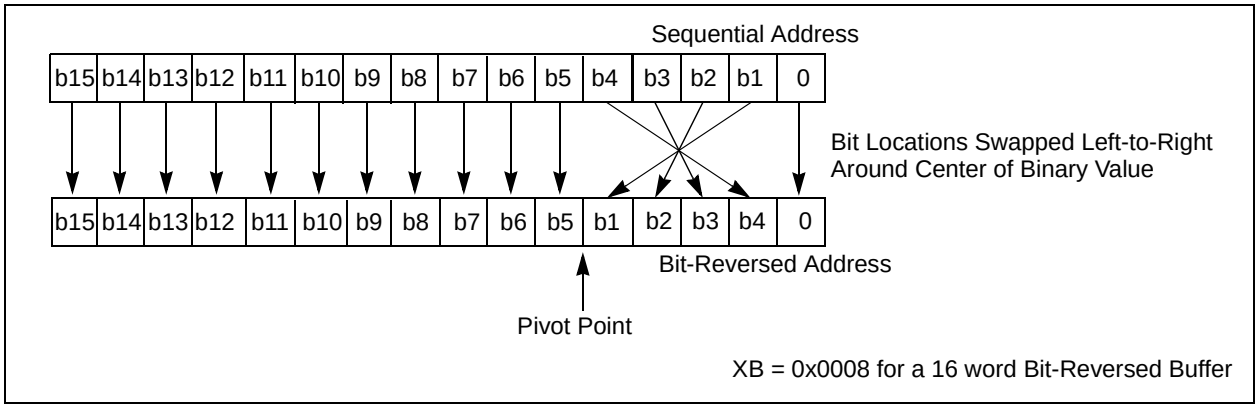
Note:	All Bit-Reversed EA calculations assume word sized data (LSb of every EA is always clear). The XB value is scaled accordingly to generate compatible (byte) addresses.

When enabled, Bit-Reversed Addressing will only be executed for register indirect with pre-increment or post-increment addressing and word sized data writes. It will not function for any other Addressing mode or for byte sized data, and normal addresses will be generated instead. When Bit-Reversed Addressing is active, the W Address Pointer will always be added to the address modifier (XB) and the offset associated with the register Indirect Addressing mode will be ignored. In addition, as word sized data is a requirement, the LSb of the EA is ignored (and always clear).

Note:	Modulo addressing and Bit-Reversed Addressing should not be enabled together. In the event that the user attempts to do this, Bit-Reversed Addressing will assume priority when active for the X WAGU, and X WAGU modulo addressing will be disabled. However, modulo addressing will continue to function in the X RAGU.

If Bit-Reversed Addressing has already been enabled by setting the BREN (XBREV<15>) bit, then a write to the XBREV register should not be immediately followed by an indirect read operation using the W register that has been designated as the bit-reversed pointer.

FIGURE 4-2: BIT-REVERSED ADDRESS EXAMPLE



5.1 Interrupt Priority

The user-assignable Interrupt Priority (IP<2:0>) bits for each individual interrupt source are located in the Least Significant 3 bits of each nibble, within the IPCx register(s). Bit 3 of each nibble is not used and is read as a '0'. These bits define the priority level assigned to a particular interrupt by the user.

Note:	The user selectable priority levels start at 0, as the lowest priority, and level 7, as the highest priority.

Since more than one interrupt request source may be assigned to a specific user specified priority level, a means is provided to assign priority within a given level. This method is called "Natural Order Priority" and is final.

Natural order priority is determined by the position of an interrupt in the vector table, and only affects interrupt operation when multiple interrupts with the same user-assigned priority become pending at the same time.

Table 5-1 lists the interrupt numbers and interrupt sources for the dsPIC DSC devices and their associated vector numbers.

Note 1:	The natural order priority scheme has 0 as the highest priority and 53 as the lowest priority.
2:	The natural order priority number is the same as the INT number.

The ability for the user to assign every interrupt to one of seven priority levels implies that the user can assign a very high overall priority level to an interrupt with a low natural order priority. The INT0 (external interrupt 0) may be assigned to priority level 1, thus giving it a very low effective priority.

TABLE 5-1: dsPIC30F1010/202X INTERRUPT VECTOR TABLE

INT Number	Vector Number	Interrupt Source
Highest Natural Order Priority		
0	8	INT0 – External Interrupt 0
1	9	IC1 – Input Capture 1
2	10	OC1 – Output Compare 1
3	11	T1 – Timer 1
4	12	Reserved
5	13	OC2 – Output Compare 2
6	14	T2 – Timer 2
7	15	T3 – Timer 3
8	16	SPI1
9	17	U1RX – UART1 Receiver
10	18	U1TX – UART1 Transmitter
11	19	ADC – ADC Convert Done
12	20	NVM – NVM Write Complete
13	21	SI2C – I^2C™ Slave Event
14	22	MI2C – I^2C Master Event
15	23	Reserved
16	24	INT1 – External Interrupt 1
17	25	INT2 – External Interrupt 2
18	26	PWM Special Event Trigger
19	27	PWM Gen#1
20	28	PWM Gen#2
21	29	PWM Gen#3
22	30	PWM Gen#4
23	31	Reserved
24	32	Reserved
25	33	Reserved
26	34	Reserved
27	35	CN – Input Change Notification
28	36	Reserved
29	37	Analog Comparator 1
30	38	Analog Comparator 2
31	39	Analog Comparator 3
32	40	Analog Comparator 4
33	41	Reserved
34	42	Reserved
35	43	Reserved
36	44	Reserved
37	45	ADC Pair 0 Conversion Done
38	46	ADC Pair 1 Conversion Done
39	47	ADC Pair 2 Conversion Done
40	48	ADC Pair 3 Conversion Done
41	49	ADC Pair 4 Conversion Done
42	50	ADC Pair 5 Conversion Done
43	51	Reserved
44	52	Reserved
45-53	53-61	Reserved
Lowest Natural Order Priority		

REGISTER 5-1: INTCON1: INTERRUPT CONTROL REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVBTE	COVTE
bit 15							bit 8

R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
SFTACERR	DIV0ERR	—	MATHERR	ADDRERR	STKERR	OSCFAIL	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **NSTDIS:** Interrupt Nesting Disable bit
1 = Interrupt nesting is disabled
0 = Interrupt nesting is enabled

bit 14 **OVAERR:** Accumulator A Overflow Trap Flag bit
1 = Trap was caused by overflow of Accumulator A
0 = Trap was not caused by overflow of Accumulator A

bit 13 **OVBERR:** Accumulator B Overflow Trap Flag bit
1 = Trap was caused by overflow of Accumulator B
0 = Trap was not caused by overflow of Accumulator B

bit 12 **COVAERR:** Accumulator A Catastrophic Overflow Trap Enable bit
1 = Trap was caused by catastrophic overflow of Accumulator A
0 = Trap was not caused by catastrophic overflow of Accumulator A

bit 11 **COVBERR:** Accumulator B Catastrophic Overflow Trap Enable bit
1 = Trap was caused by catastrophic overflow of Accumulator B
0 = Trap was not caused by catastrophic overflow of Accumulator B

bit 10 **OVATE:** Accumulator A Overflow Trap Enable bit
1 = Trap overflow of Accumulator A
0 = Trap disabled

bit 9 **OVBTE:** Accumulator B Overflow Trap Enable bit
1 = Trap overflow of Accumulator B
0 = Trap disabled

bit 8 **COVTE:** Catastrophic Overflow Trap Enable bit
1 = Trap on catastrophic overflow of Accumulator A or B enabled
0 = Trap disabled

bit 7 **SFTACERR:** Shift Accumulator Error Status bit
1 = Math error trap was caused by an invalid accumulator shift
0 = Math error trap was not caused by an invalid accumulator shift

bit 6 **DIV0ERR:** Arithmetic Error Status bit
1 = Math error trap was caused by a divided by zero
0 = Math error trap was not caused by an invalid accumulator shift

bit 5 **Unimplemented:** Read as ‘0’

bit 4 **MATHERR:** Arithmetic Error Status bit
1 = Overflow trap has occurred
0 = Overflow trap has not occurred

bit 3 **ADDRERR:** Address Error Trap Status bit
1 = Address error trap has occurred
0 = Address error trap has not occurred

6.2 Configuring Analog Port Pins

The use of the ADPCFG and TRIS registers control the operation of the A/D port pins. The port pins that are desired as analog inputs must have their corresponding TRIS bit set (input). If the TRIS bit is cleared (output), the digital output level (V_{OH} or V_{OL}) will be converted.

When reading the PORT register, all pins configured as analog input channel will read as cleared (a low level).

Pins configured as digital inputs will not convert an analog input. Analog levels on any pin that is defined as a digital input (including the ANx pins), may cause the input buffer to consume current that exceeds the device specifications.

6.2.1 I/O PORT WRITE/READ TIMING

One instruction cycle is required between a port direction change or port write operation and a read operation of the same port. Typically this instruction would be a NOP.

EXAMPLE 6-1: PORT WRITE/READ EXAMPLE

```
MOV 0xFF00, W0; Configure PORTB<15:8>
      ; as inputs
MOV W0, TRISBB; and PORTB<7:0> as outputs
NOP   ; Delay 1 cycle
BTSS PORTB, #13; Next Instruction
```

6.3 Input Change Notification

The input change notification function of the I/O ports allows the dsPIC30F1010/202X devices to generate interrupt requests to the processor in response to a change-of-state on selected input pins. This feature is capable of detecting input change-of-states even in Sleep mode, when the clocks are disabled. There are 8 external signals (CN0 through CN7) that can be selected (enabled) for generating an interrupt request on a change-of-state.

There are two control registers associated with the CN module. The CNEN1 register contain the CN interrupt enable (CNxIE) control bits for each of the CN input pins. Setting any of these bits enables a CN interrupt for the corresponding pins.

Each CN pin also has a weak pull-up connected to it. The pull-ups act as a current source that is connected to the pin and eliminate the need for external resistors when push button or keypad devices are connected. The pull-ups are enabled separately using the CNPU1 register, which contain the weak pull-up enable (CNxPUE) bits for each of the CN pins. Setting any of the control bits enables the weak pull-ups for the corresponding pins.

Note: Pull-ups on change notification pins should always be disabled whenever the port pin is configured as a digital output.

TABLE 8-1: TIMER1 REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
TMR1	0100	Timer 1 Register																uuuu uuuu uuuu uuuu
PR1	0102	Period Register 1																1111 1111 1111 1111
T1CON	0104	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS<1:0>		—	TSYNC	TCS	—	0000 0000 0000 0000

Legend: u = uninitialized bit

Note: Refer to the "*dsPIC30F Family Reference Manual*" (DS70046) for descriptions of register bit fields.

10.0 INPUT CAPTURE MODULE

Note: This data sheet summarizes features of this group of dsPIC30F devices and is not intended to be a complete reference source. For more information on the CPU, peripherals, register descriptions and general device functionality, refer to the "*dsPIC30F Family Reference Manual*" (DS70046).

This section describes the Input Capture module and associated operational modes. The features provided by this module are useful in applications requiring Frequency (Period) and Pulse measurement. Figure 10-1 depicts a block diagram of the Input Capture module. Input capture is useful for such modes as:

- Frequency/Period/Pulse Measurements
- Additional sources of External Interrupts

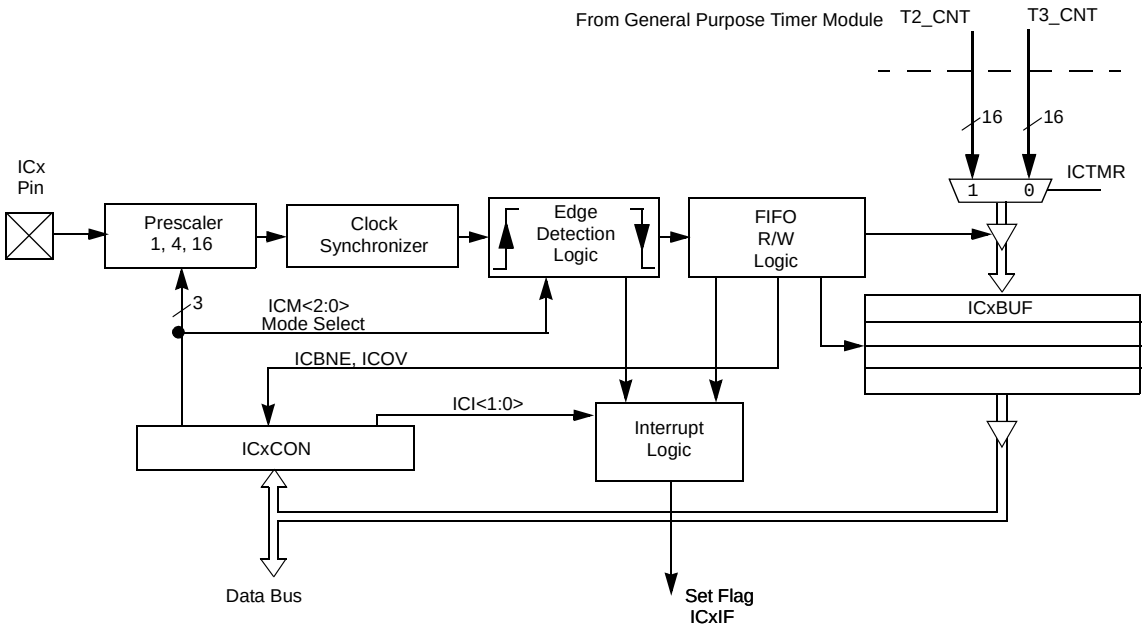
The key operational features of the Input Capture module are:

- Simple Capture Event mode
- Timer2 and Timer3 mode selection
- Interrupt on input capture event

These operating modes are determined by setting the appropriate bits in the ICxCON register (where x = 1,2,...,N). The dsPIC DSC devices contain up to 8 capture channels, (i.e., the maximum value of N is 8).

Note: The dsPIC30F1010 devices does not feature a Input Capture module. The dsPIC30F202X devices have one capture input – IC1. The naming of this capture channel is intentional and preserves software compatibility with other dsPIC DSC devices.

FIGURE 10-1: INPUT CAPTURE MODE BLOCK DIAGRAM



Note: Where 'x' is shown, reference is made to the registers or bits associated to the respective input capture channels 1 through N.

11.4.1 PWM PERIOD

The PWM period is specified by writing to the PRx register. The PWM period can be calculated using Equation 11-1.

EQUATION 11-1: PWM PERIOD

$$\text{PWM period} = [(\text{PRx}) + 1] \cdot 4 \cdot T_{OSC} \cdot (\text{TMRx prescale value})$$

PWM frequency is defined as 1/[PWM period].

When the selected TMRx is equal to its respective period register, PRx, the following four events occur on the next increment cycle:

- TMRx is cleared.
- The OCx pin is set.
  - Exception 1: If PWM duty cycle is 0x0000, the OCx pin will remain low.
  - Exception 2: If duty cycle is greater than PRx, the pin will remain high.
- The PWM duty cycle is latched from OCxRS into OCxR.
- The corresponding timer interrupt flag is set.

See Figure 11-1 for key PWM period comparisons. Timer3 is referred to in the figure for clarity.

11.4.2 PWM WITH FAULT PROTECTION INPUT PIN

When control bits OCM<2:0> (OCxCON<2:0>) = 111, Fault protection is enabled via the OCFLTA pin. If the a logic '0' is detected on the OCFLTA pin, the output pins are placed in a high-impedance state. The state remains until:

- the external Fault condition has been removed **and**
- the PWM mode is reenabled by writing to the appropriate control bits

As a result of the Fault condition, the OCxIF interrupt is asserted, and an interrupt will be generated, if enabled. Upon detection of the Fault condition, the OCFLTx bit in the OCxCON register is asserted high. This bit is a read-only bit and will be cleared once the external Fault condition has been removed, and the PWM mode is reenabled by writing the appropriate mode bits, OCM<2:0> in the OCxCON register.

11.5 Output Compare Operation During CPU Sleep Mode

When the CPU enters the Sleep mode, all internal clocks are stopped. Therefore, when the CPU enters the Sleep state, the output compare channel will drive the pin to the active state that was observed prior to entering the CPU Sleep state.

For example, if the pin was high when the CPU entered the Sleep state, the pin will remain high. Likewise, if the pin was low when the CPU entered the Sleep state, the pin will remain low. In either case, the output compare module will resume operation when the device wakes up.

11.6 Output Compare Operation During CPU Idle Mode

When the CPU enters the Idle mode, the output compare module can operate with full functionality.

The output compare channel will operate during the CPU Idle mode if the OCSIDL bit (OCxCON<13>) is at logic '0' and the selected time base (Timer2 or Timer3) is enabled and the TSIDL bit of the selected timer is set to logic '0'.

REGISTER 12-12: FCLCONx: PWM FAULT CURRENT-LIMIT CONTROL REGISTER (CONTINUED)

bit 6-3 **FLTSRC<3:0>:** Fault Control Signal Source Select for PWM Generator #X bits
0000 = Analog Comparator #1
0001 = Analog Comparator #2
0010 = Analog Comparator #3
0011 = Analog Comparator #4

0100 = Reserved
0101 = Reserved
0110 = Reserved
0111 = Reserved

1000 = Shared Fault #1 (SFLT1)
1001 = Shared Fault #2 (SFLT2)
1020 = Shared Fault #3 (SFLT3)
1011 = Shared Fault #4 (SFLT4)

1100 = Reserved
1101 = Independent Fault #2 (IFLT2)
1110 = Reserved
1111 = Independent Fault #4 (IFLT4)

bit 2 **FLTPOL:** Fault Polarity for PWM Generator #X bit
1 = The selected Fault source is low active
0 = The selected Fault source is high active

bit 1-0 **FLTMOD<1:0>:** Fault Mode for PWM Generator #x bits
00 = The selected Fault source forces PWMxH, PWMxL pins to FLTDAT values (latched condition)
01 = The selected Fault source forces PWMxH, PWMxL pins to FLTDAT values (cycle)
10 = Reserved
11 = Fault input is disabled

12.4 Module Functionality

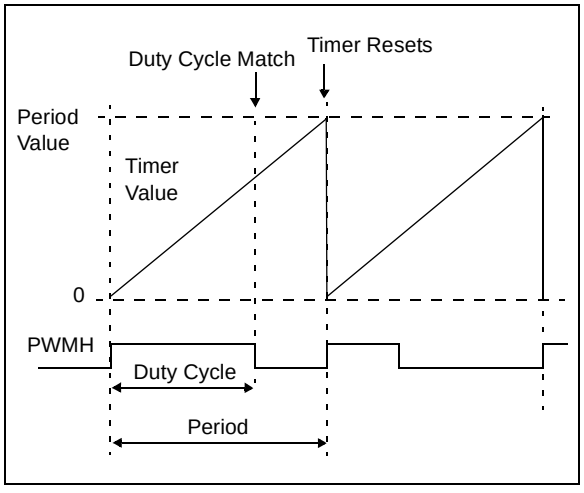
The PS PWM module is a very high-speed design that provides capabilities not found in other PWM generators. The module supports these PWM modes:

- Standard Edge-Aligned PWM mode
- Complementary PWM mode
- Push-Pull PWM mode
- Multi-Phase PWM mode
- Variable Phase PWM mode
- Current-Limit PWM mode
- Constant Off-time PWM mode
- Current Reset PWM mode
- Independent Time Base PWM mode

12.4.1 STANDARD EDGE-ALIGNED PWM MODE

Standard Edge-Aligned mode (Figure 12-3) is the basic PWM mode used by many power converter topologies such as “Buck”, “Boost” and “Forward”. To create the edge-aligned PWM, a timer/counter circuit counts upward from zero to a specified maximum value for the Period. Another register contains the value for Duty Cycle, which is constantly compared to the timer (Period) value. While the timer/counter value is less than or equal to the duty cycle value, the PWM output signal is asserted. When the timer value exceeds the duty cycle value, the PWM signal is deasserted. When the timer is greater than the period value, the timer is reset, and the process repeats.

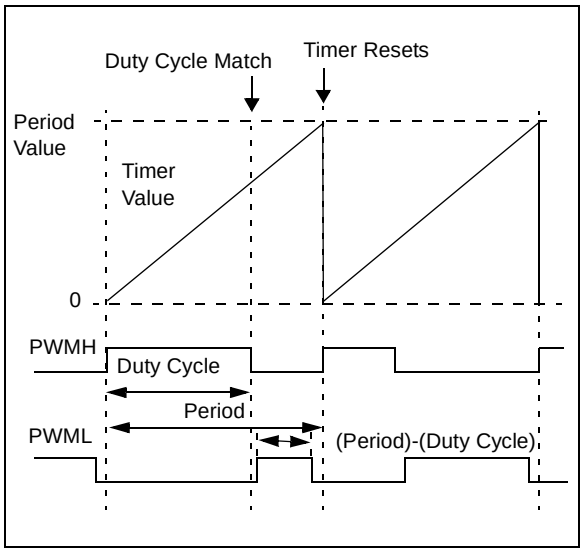
FIGURE 12-3: EDGE-ALIGNED PWM



12.4.2 COMPLEMENTARY PWM MODE

Complementary PWM is generated in a manner similar to standard Edge-Aligned PWM. Complementary mode provides a second PWM output signal on the PWML pin that is the complement of the primary PWM signal (PWMH). Complementary mode PWM is shown in Figure 12-4.

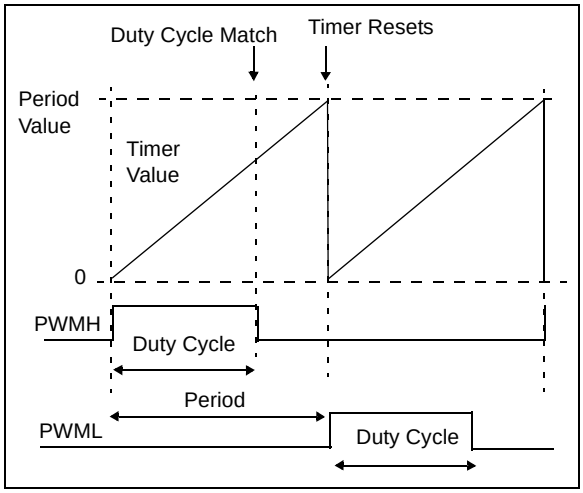
FIGURE 12-4: COMPLEMENTARY PWM



12.4.3 PUSH-PULL PWM MODE

The Push-Pull mode shown in Figure 12-5 is a version of the standard Edge-Aligned PWM mode where the active PWM signal is alternately outputted on one of two PWM pins. There is no complementary PWM output available. This mode is useful in transformer-based power converters. Transformer-based circuits must avoid any direct currents that will cause their cores to saturate. The Push-Pull mode ensures that the duty cycle of the two phases is identical, thus yielding a net DC bias of zero.

FIGURE 12-5: PUSH-PULL PWM



16.0 10-BIT 2 Msps ANALOG-TO-DIGITAL CONVERTER (ADC) MODULE

The dsPIC30F1010/202X devices provide high-speed successive approximation analog to digital conversions to support applications such as AC/DC and DC/DC power converters.

16.1 Features

- 10-bit resolution
- Uni-polar Inputs
- Up to 12 input channels
- ±1 LSB accuracy
- Single supply operation
- 2000 ksps conversion rate at 5V
- 1000 ksps conversion rate at 3.0V
- Low power CMOS technology

16.2 Description

This ADC module is designed for applications that require low latency between the request for conversion and the resultant output data. Typical applications include:

- AC/DC power supplies
- DC/DC converters
- Power factor correction

This ADC works with the Power Supply PWM module in power control applications that require high-frequency control loops. This module can sample and convert two analog inputs in one microsecond. The one microsecond conversion delay reduces the “phase lag” between measurement and control system response.

Up to 4 inputs may be sampled at a time, and up to 12 inputs may request conversion at a time. If multiple inputs request conversion, the ADC will convert them in a sequential manner starting with the lowest order input.

This ADC design provides each pair of analog inputs (AN1,AN0), (AN3,AN2), ... , the ability to specify its own trigger source out of a maximum of sixteen different trigger sources. This capability allows this ADC to sample and convert analog inputs that are associated with PWM generators operating on independent time bases.

There is no operation during Sleep mode. The user applications typically require synchronization between analog data sampling and PWM output to the application circuit. The very high speed operation of this ADC module allows “data on demand”.

In addition, several hardware features have been added to the peripheral interface to improve real-time performance in a typical DSP based application.

1. Result alignment options
2. Automated sampling
3. External conversion start control

A block diagram of the ADC module is shown in Figure 16-1.

16.3 Module Functionality

The 10-bit 2 Msps ADC is designed to support power conversion applications when used with the Power Supply PWM module. The 10-bit 2 Msps ADC samples up to N ($N \leq 12$) inputs at a time and then converts two sampled inputs at a time. The quantity of sample and hold circuits is determined by a device’s requirements. The10-Bit 2 Msps ADC produces two 10-bit conversion results in 1 microsecond.

The ADC module supports up to 12 analog inputs. The sampled inputs are connected, via multiplexers, to the converter.

The analog reference voltage is defined as the device supply voltage (AV_{DD}/AV_{SS}).

The ADC module uses these Control and Status registers:

- A/D Control Register (ADCON)
- A/D Status Register (ADSTAT)
- A/D Base Register (ADBASE)
- A/D Port Configuration Register (ADPCFG)
- A/D Convert Pair Control Register 0 (ADCPC0)
- A/D Convert Pair Control Register 1 (ADCPC1)
- A/D Convert Pair Control Register 2 (ADCPC2)

The ADCON register controls the operation of the ADC module. The ADSTAT register displays the status of the conversion processes. The ADPCFG registers configure the port pins as analog inputs or as digital I/O. The CPC registers control the triggering of the ADC conversions. (See Register 16-1 through Register 16-7 for detailed bit configurations.)

Note: A unique feature of the ADC module is its ability to sample inputs in an asynchronous manner. Individual sample and hold circuits can be triggered independently of each other.

Note: The PLL must be enabled for the ADC module to function. This is achieved by using the FNOSC<1:0> bits in the FOSCSEL Configuration register.

17.0 SMPS COMPARATOR MODULE

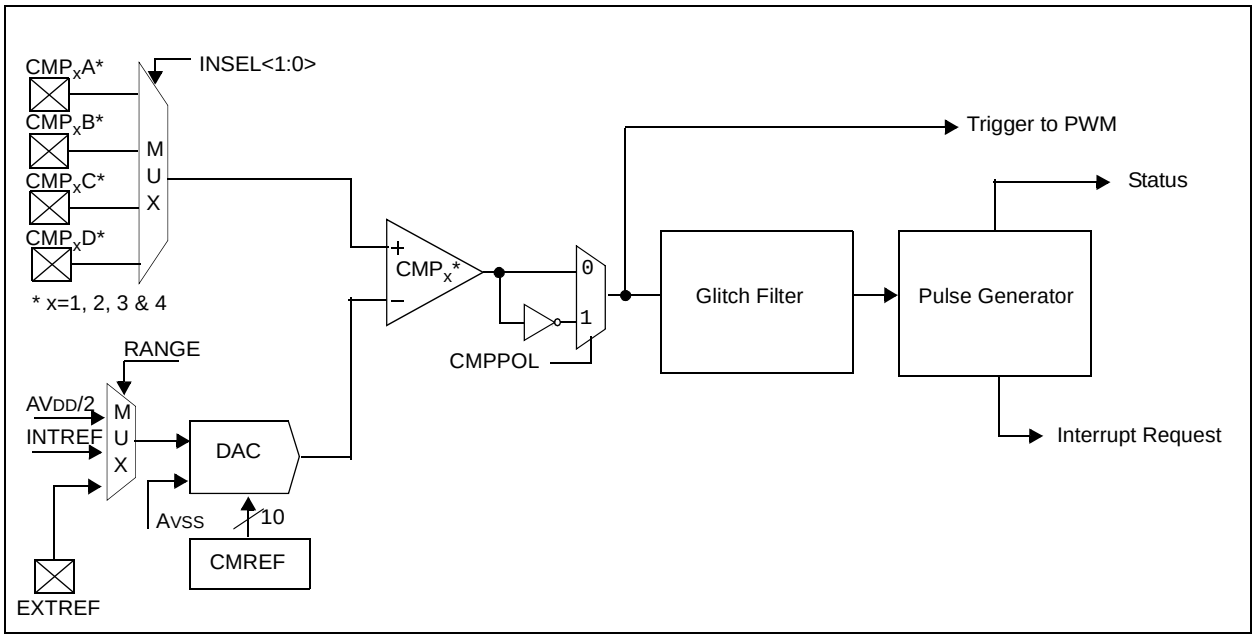
Note: This data sheet summarizes features of this group of dsPIC30F devices and is not intended to be a complete reference source. For more information on the CPU, peripherals, register descriptions and general device functionality, refer to the "*dsPIC30F Family Reference Manual*" (DS70046).

The dsPIC30F SMPS Comparator module monitors current and/or voltage transients that may be too fast for the CPU and ADC to capture.

17.1 Features Overview

- 16 comparator inputs
- 10-bit DAC provides reference
- Programmable output polarity
- Interrupt generation capability
- Selectable Input sources
- DAC has three ranges of operation:
  - AVDD/2
  - Internal Reference 1.2V 1%
  - External Reference < (AVDD - 1.6V)
- ADC sample and convert trigger capability
- Can be disabled to reduce power consumption
- Functional support for PWM Module:
  - PWM Duty Cycle Control
  - PWM Period Control
  - PWM Fault Detect

FIGURE 17-1: COMPARATOR MODULE BLOCK DIAGRAM



17.2 Module Applications

This module provides a means for the SMPS dsPIC DSC devices to monitor voltage and currents in a power conversion application. The ability to detect transient conditions and stimulate the dsPIC DSC processor and/or peripherals without requiring the processor and ADC to constantly monitor voltages or currents frees the dsPIC DSC to perform other tasks.

The Comparator module has a high-speed comparator and an associated 10-bit DAC that provides a programmable reference voltage to one input of the comparator. The polarity of the comparator output is user programmable. The output of the module can be used in the following modes:

- Generate an interrupt
- Trigger an ADC sample and convert process
- Truncate the PWM signal (current limit)
- Truncate the PWM period (current minimum)
- Disable the PWM outputs (Fault-latch)

The output of the Comparator module may be used in multiple modes at the same time, such as: (1) generate an interrupt, (2) have the ADC take a sample and convert it and (3) truncate the PWM output in response to a voltage being detected beyond its expected value.

The Comparator module can also be used to wake-up the system from Sleep or Idle mode when the analog input voltage exceeds the programmed threshold voltage.

18.0 SYSTEM INTEGRATION

Note: This data sheet summarizes features of this group of dsPIC30F devices and is not intended to be a complete reference source. For more information on the CPU, peripherals, register descriptions and general device functionality, refer to the "*dsPIC30F Family Reference Manual*" (DS70046).
For more information on the device instruction set and programming, refer to the "*dsPIC30F/33F Programmer's Reference Manual*" (DS70157).

There are several features intended to maximize system reliability, minimize cost through elimination of external components, provide power-saving operating modes and offer code protection:

- Oscillator Selection
- Reset:
  - Power-on Reset (POR)
  - Power-up Timer (PWRT)
  - Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT)
- Power-Saving modes (Sleep and Idle)
- Code Protection
- Unit ID Locations
- In-Circuit Serial Programming (ICSP) programming capability

dsPIC30F devices have a Watchdog Timer, which can be permanently enabled via the Configuration bits or can be software controlled. It runs off its own RC oscillator for added reliability. There are two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in Reset until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a delay on power-up only, designed to keep the part in Reset mode while the power supply stabilizes. With these two timers on-chip, most applications need no external Reset circuitry.

Sleep mode is designed to offer a very low-current Power-Down mode. The user can wake-up from Sleep mode through external Reset, Watchdog Timer Wake-up or through an interrupt. Several oscillator options are also made available to allow the part to fit a wide variety of applications. In the Idle mode, the clock sources are still active, but the CPU is shut off. The RC oscillator option saves system cost, while the LP crystal option saves power.

18.1 Oscillator System Overview

The dsPIC30F oscillator system has the following modules and features:

- Various external and internal oscillator options as clock sources
- An on-chip PLL to boost internal operating frequency
- A clock switching mechanism between various clock sources
- Programmable clock postscaler for system power savings
- A Fail-Safe Clock Monitor (FSCM) that detects clock failure and takes fail-safe measures
- Clock Control register OSCCON
- Configuration bits for main oscillator selection

Configuration bits determine the clock source upon Power-on Reset (POR). Thereafter, the clock source can be changed between permissible clock sources. The OSCCON register controls the clock switching and reflects system clock related status bits.

Note: 32 kHz crystal operation is not enabled on dsPIC30F1010/202X devices.

A simplified diagram of the oscillator system is shown in Figure 18-1.

18.2 Oscillator Control Registers

The oscillators are controlled with these registers:

- OSCCON: Oscillator Control Register
- OSCTUN2: Oscillator Tuning Register 2
- LFSR: Linear Feedback Shift Register
- FOSCSEL: Oscillator Selection Configuration Bits
- FOSC: Oscillator Selection Configuration Bits

TABLE 19-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax		Description	# of words	# of cycles	Status Flags Affected
52	NEG	NEG	Acc	Negate Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
		NEG	f	f = $\overline{f}$ + 1	1	1	C,DC,N,OV,Z
		NEG	f,WREG	WREG = $\overline{f}$ + 1	1	1	C,DC,N,OV,Z
		NEG	Ws,Wd	Wd = $\overline{Ws}$ + 1	1	1	C,DC,N,OV,Z
53	NOP	NOP		No Operation	1	1	None
		NOPR		No Operation	1	1	None
54	POP	POP	f	Pop f from Top-of-Stack (TOS)	1	1	None
		POP	Wdo	Pop from Top-of-Stack (TOS) to Wdo	1	1	None
		POP.D	Wnd	Pop from Top-of-Stack (TOS) to W(nd):W(nd + 1)	1	2	None
		POP.S		Pop Shadow Registers	1	1	All
55	PUSH	PUSH	f	Push f to Top-of-Stack (TOS)	1	1	None
		PUSH	Wso	Push Wso to Top-of-Stack (TOS)	1	1	None
		PUSH.D	Wns	Push W(ns):W(ns + 1) to Top-of-Stack (TOS)	1	2	None
		PUSH.S		Push Shadow Registers	1	1	None
56	PWRSAV	PWRSAV	#lit1	Go into Sleep or Idle mode	1	1	WDTO,Sleep
57	RCALL	RCALL	Expr	Relative Call	1	2	None
		RCALL	Wn	Computed Call	1	2	None
58	REPEAT	REPEAT	#lit14	Repeat Next Instruction lit14 + 1 times	1	1	None
		REPEAT	Wn	Repeat Next Instruction (Wn) + 1 times	1	1	None
59	RESET	RESET		Software device Reset	1	1	None
60	RETFIE	RETFIE		Return from interrupt	1	3 (2)	None
61	RETLW	RETLW	#lit10,Wn	Return with literal in Wn	1	3 (2)	None
62	RETURN	RETURN		Return from Subroutine	1	3 (2)	None
63	RLC	RLC	f	f = Rotate Left through Carry f	1	1	C,N,Z
		RLC	f,WREG	WREG = Rotate Left through Carry f	1	1	C,N,Z
		RLC	Ws,Wd	Wd = Rotate Left through Carry Ws	1	1	C,N,Z
64	RLNC	RLNC	f	f = Rotate Left (No Carry) f	1	1	N,Z
		RLNC	f,WREG	WREG = Rotate Left (No Carry) f	1	1	N,Z
		RLNC	Ws,Wd	Wd = Rotate Left (No Carry) Ws	1	1	N,Z
65	RRC	RRC	f	f = Rotate Right through Carry f	1	1	C,N,Z
		RRC	f,WREG	WREG = Rotate Right through Carry f	1	1	C,N,Z
		RRC	Ws,Wd	Wd = Rotate Right through Carry Ws	1	1	C,N,Z
66	RRNC	RRNC	f	f = Rotate Right (No Carry) f	1	1	N,Z
		RRNC	f,WREG	WREG = Rotate Right (No Carry) f	1	1	N,Z
		RRNC	Ws,Wd	Wd = Rotate Right (No Carry) Ws	1	1	N,Z
67	SAC	SAC	Acc,#Slit4,Wdo	Store Accumulator	1	1	None
		SAC.R	Acc,#Slit4,Wdo	Store Rounded Accumulator	1	1	None
68	SE	SE	Ws,Wnd	Wnd = sign extended Ws	1	1	C,N,Z
69	SETM	SETM	f	f = 0xFFFF	1	1	None
		SETM	WREG	WREG = 0xFFFF	1	1	None
		SETM	Ws	Ws = 0xFFFF	1	1	None
70	SFTAC	SFTAC	Acc,Wn	Arithmetic Shift Accumulator by (Wn)	1	1	OA,OB,OAB, SA,SB,SAB
		SFTAC	Acc,#Slit6	Arithmetic Shift Accumulator by Slit6	1	1	OA,OB,OAB, SA,SB,SAB
71	SL	SL	f	f = Left Shift f	1	1	C,N,OV,Z
		SL	f,WREG	WREG = Left Shift f	1	1	C,N,OV,Z
		SL	Ws,Wd	Wd = Left Shift Ws	1	1	C,N,OV,Z
		SL	Wb,Wns,Wnd	Wnd = Left Shift Wb by Wns	1	1	N,Z
		SL	Wb,#lit5,Wnd	Wnd = Left Shift Wb by lit5	1	1	N,Z

20.11 Demonstration/Development Boards, Evaluation Kits and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

20.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent® and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika®

TABLE 21-21: TIMER2 EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions: 3.3V and 5.0V (±10%) (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**		**Min**	**Typ**	**Max**	**Units**	**Conditions**
TB10	TTXH	T2CK High Time	Synchronous, no prescaler	0.5 TCY + 20	—	—	ns	Must also meet Parameter TB15
			Synchronous, with prescaler	10	—	—	ns	
TB11	TTXL	T2CK Low Time	Synchronous, no prescaler	0.5 TCY + 20	—	—	ns	Must also meet Parameter TB15
			Synchronous, with prescaler	10	—	—	ns	
TB15	TTXP	T2CK Input Period	Synchronous, no prescaler	TCY + 10	—	—	ns	N = Prescale value (1, 8, 64, 256)
			Synchronous, with prescaler	Greater of: 20 ns or (TCY + 40)/N	—	—	—	
TB20	TCKEXTMRL	Delay from External T2CK Clock Edge to Timer Increment		0.5 TCY	—	1.5 TCY	—	

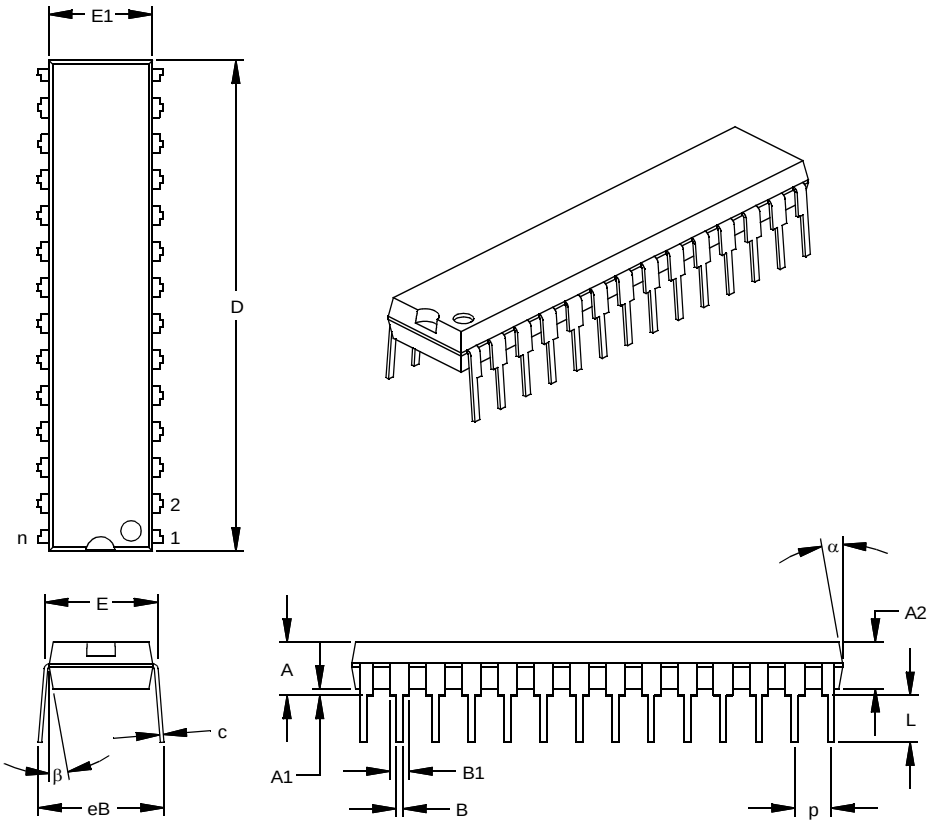
TABLE 21-22: TIMER3 EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions: 3.3V and 5.0V (±10%) (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**		**Min**	**Typ**	**Max**	**Units**	**Conditions**
TC10	TTXH	T3CK High Time	Synchronous	0.5 TCY + 20	—	—	ns	Must also meet Parameter TC15
TC11	TTXL	T3CK Low Time	Synchronous	0.5 TCY + 20	—	—	ns	Must also meet Parameter TC15
TC15	TTXP	T3CK Input Period	Synchronous, no prescaler	TCY + 10	—	—	ns	N = Prescale value (1, 8, 64, 256)
			Synchronous, with prescaler	Greater of: 20 ns or (TCY + 40)/N	—	—	—	
TC20	TCKEXTMRL	Delay from External T3CK Clock Edge to Timer Increment		0.5 TCY	—	1.5 TCY	—	

NOTES:

28-Lead Skinny Plastic Dual In-line (SP) – 300 mil Body (PDIP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		28			28	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.150	.160	3.56	3.81	4.06
Molded Package Thickness	A2	.125	.130	.135	3.18	3.30	3.43
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.310	.325	7.62	7.87	8.26
Molded Package Width	E1	.275	.285	.295	6.99	7.24	7.49
Overall Length	D	1.345	1.365	1.385	34.16	34.67	35.18
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.040	.053	.065	1.02	1.33	1.65
Lower Lead Width	B	.016	.019	.022	0.41	0.48	0.56
Overall Row Spacing §	eB	.320	.350	.430	8.13	8.89	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

***** Controlling Parameter
§ Significant Characteristic
Notes:
Dimension D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MO-095
Drawing No. C04-070