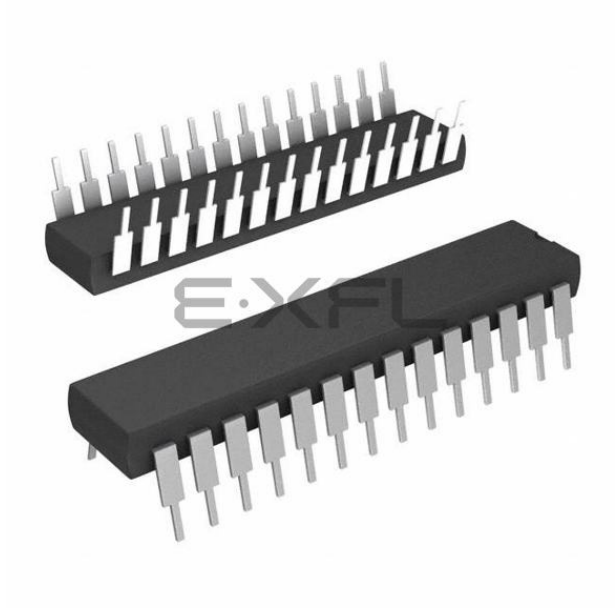

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Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	21
Program Memory Size	12KB (4K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
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Supplier Device Package	28-SPDIP
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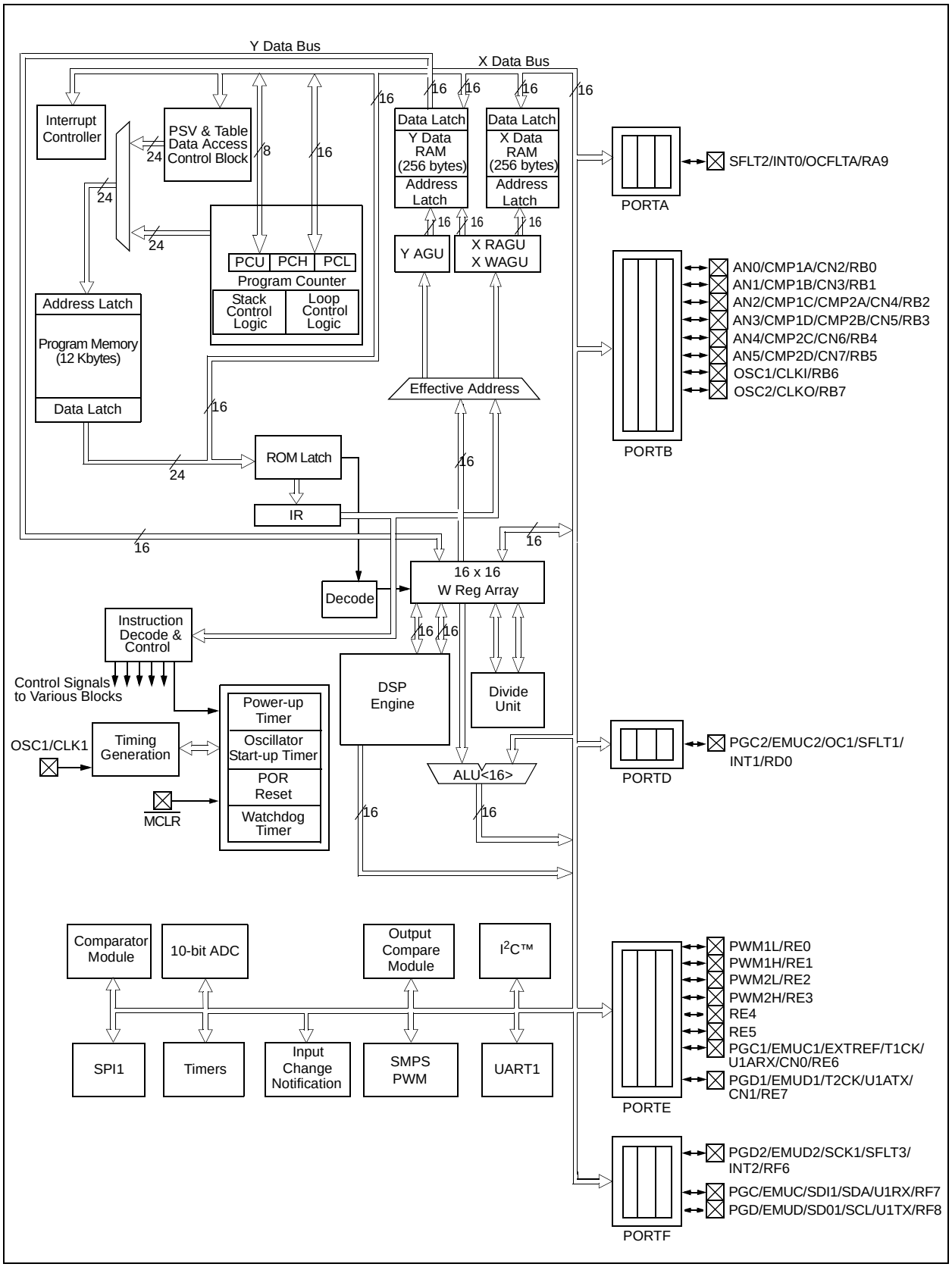
FIGURE 1-1: dsPIC30F1010 BLOCK DIAGRAM



2.2 Programmer's Model

The programmer's model is shown in Figure 2-1 and consists of 16x16-bit working registers (W0 through W15), 2x40-bit accumulators (ACCA and ACCB), STATUS register (SR), Data Table Page register (TBLPAG), Program Space Visibility Page register (PSVPAG), DO and REPEAT registers (DOSTART, DOEND, DCOUNT and RCOUNT), and Program Counter (PC). The working registers can act as data, address or offset registers. All registers are memory mapped. W0 acts as the W register for file register addressing.

Some of these registers have a shadow register associated with each of them, as shown in Figure 2-1. The shadow register is used as a temporary holding register and can transfer its contents to or from its host register upon the occurrence of an event. None of the shadow registers are accessible directly. The following rules apply for transfer of registers into and out of shadows.

- `PUSH.S` and `POP.S`
  W0, W1, W2, W3, SR (DC, N, OV, Z and C bits only) are transferred.
- `DO` instruction
  DOSTART, DOEND, DCOUNT shadows are pushed on loop start, and popped on loop end.

When a byte operation is performed on a working register, only the Least Significant Byte (LSB) of the target register is affected. However, a benefit of memory mapped working registers is that both the Least and Most Significant Bytes (MSBs) can be manipulated through byte wide data memory space accesses.

2.2.1 SOFTWARE STACK POINTER/ FRAME POINTER

The dsPIC® DSC devices contain a software stack. W15 is the dedicated software Stack Pointer (SP), and will be automatically modified by exception processing and subroutine calls and returns. However, W15 can be referenced by any instruction in the same manner as all other W registers. This simplifies the reading, writing and manipulation of the Stack Pointer (e.g., creating stack frames).

Note:	In order to protect against misaligned stack accesses, W15<0> is always clear.

W15 is initialized to 0x0800 during a Reset. The user may reprogram the SP during initialization to any location within data space.

W14 has been dedicated as a Stack Frame Pointer as defined by the `LNK` and `ULNK` instructions. However, W14 can be referenced by any instruction in the same manner as all other W registers.

2.2.2 STATUS REGISTER

The dsPIC DSC core has a 16-bit STATUS Register (SR), the LSB of which is referred to as the SR Low Byte (SRL) and the MSB as the SR High Byte (SRH). See Figure 2-1 for SR layout.

SRL contains all the MCU ALU operation status flags (including the Z bit), as well as the CPU Interrupt Priority Level Status bits, IPL<2:0>, and the REPEAT active Status bit, RA. During exception processing, SRL is concatenated with the MSB of the PC to form a complete word value, which is then stacked.

The upper byte of the STATUS register contains the DSP Adder/Subtracter status bits, the DO Loop Active bit (DA) and the Digit Carry (DC) Status bit.

2.2.3 PROGRAM COUNTER

The Program Counter is 23 bits wide. Bit 0 is always clear. Therefore, the PC can address up to 4M instruction words.

3.0 MEMORY ORGANIZATION

Note: This data sheet summarizes features of this group of dsPIC30F devices and is not intended to be a complete reference source. For more information on the CPU, peripherals, register descriptions and general device functionality, refer to the "*dsPIC30F Family Reference Manual*" (DS70046). For more information on the device instruction set and programming, refer to the "*dsPIC30F/33F Programmer's Reference Manual*" (DS70157).

3.1 Program Address Space

The program address space is 4M instruction words. It is addressable by a 24-bit value from either the 23-bit PC, table instruction Effective Address (EA), or data space EA, when program space is mapped into data space, as defined by Table 3-1. Note that the program space address is incremented by two between successive program words, in order to provide compatibility with data space addressing.

User program space access is restricted to the lower 4M instruction word address range (0x000000 to 0x7FFFFE), for all accesses other than TBLRD/TBLWT, which use TBLPAG<7> to determine user or configuration space access. In Table 3-1, Read/Write instructions, bit 23 allows access to the Device ID, the User ID and the Configuration bits. Otherwise, bit 23 is always clear.

Note: The address map shown in Figure 3-1 is conceptual, and the actual memory configuration may vary across individual devices depending on available memory.

FIGURE 3-1: PROGRAM SPACE MEMORY MAP FOR dsPIC30F1010/202X

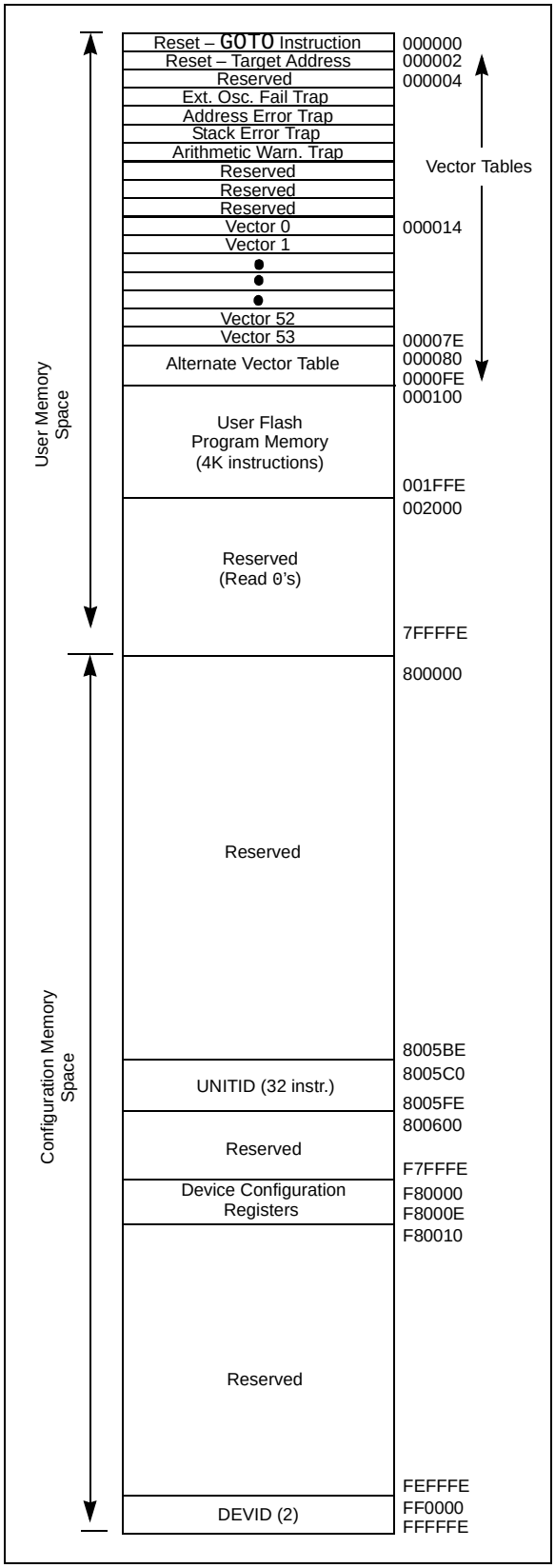
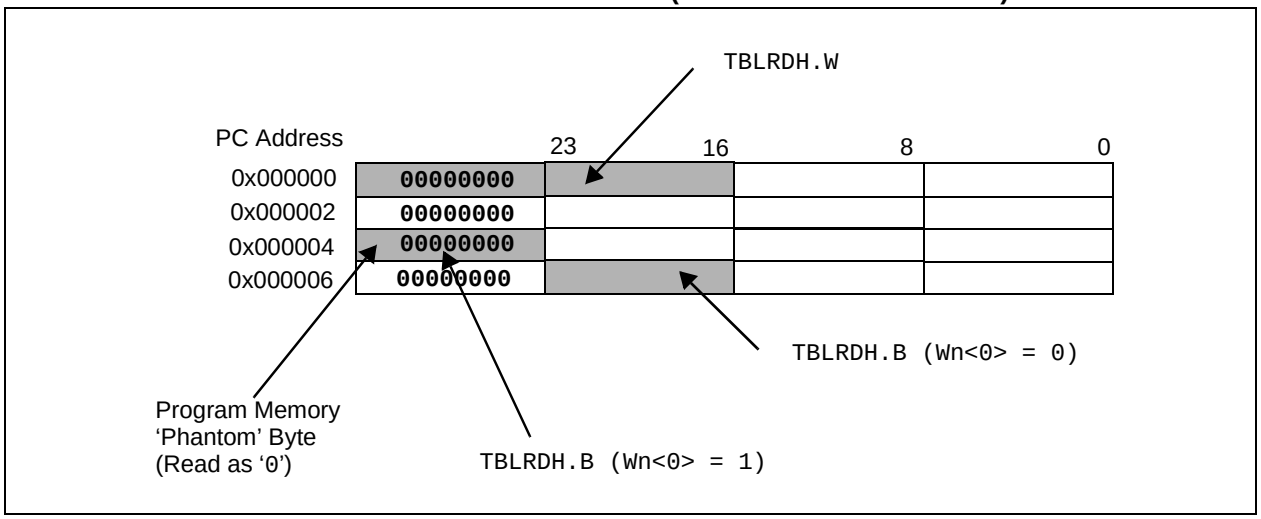


FIGURE 3-4: PROGRAM DATA TABLE ACCESS (MOST SIGNIFICANT BYTE)



3.1.2 DATA ACCESS FROM PROGRAM MEMORY USING PROGRAM SPACE VISIBILITY

The upper 32 Kbytes of data space may optionally be mapped into any 16K word program space page. This provides transparent access of stored constant data from X data space, without the need to use special instructions (i.e., TBLRDL/H, TBLWTL/H instructions).

Program space access through the data space occurs if the MSb of the data space EA is set and program space visibility is enabled, by setting the PSV bit in the Core Control register (CORCON). The functions of CORCON are discussed in **Section 2.4 "DSP Engine"**.

Data accesses to this area add an additional cycle to the instruction being executed, since two program memory fetches are required.

Note that the upper half of addressable data space is always part of the X data space. Therefore, when a DSP operation uses program space mapping to access this memory region, Y data space should typically contain state (variable) data for DSP operations, whereas X data space should typically contain coefficient (constant) data.

Although each data space address, 0x8000 and higher, maps directly into a corresponding program memory address (see Figure 3-5), only the lower 16-bits of the 24-bit program word are used to contain the data. The upper 8 bits should be programmed to force an illegal instruction to maintain machine robustness. Refer to the "*dsPIC30F/33F Programmer's Reference Manual*" (DS70157) for details on instruction encoding.

Note that by incrementing the PC by 2 for each program memory word, the Least Significant 15 bits of data space addresses directly map to the Least Significant 15 bits in the corresponding program space addresses. The remaining bits are provided by the Program Space Visibility Page register, PSVPAG<7:0>, as shown in Figure 3-5.

Note:	PSV access is temporarily disabled during Table Reads/Writes.

For instructions that use PSV which are executed outside a REPEAT loop:

- The following instructions will require one instruction cycle in addition to the specified execution time:
  - MAC class of instructions with data operand prefetch
  - MOV instructions
  - MOV.D instructions
- All other instructions will require two instruction cycles in addition to the specified execution time of the instruction.

For instructions that use PSV which are executed inside a REPEAT loop:

- The following instances will require two instruction cycles in addition to the specified execution time of the instruction:
  - Execution in the first iteration
  - Execution in the last iteration
  - Execution prior to exiting the loop due to an interrupt
  - Execution upon re-entering the loop after an interrupt is serviced
- Any other iteration of the REPEAT loop will allow the instruction, accessing data using PSV, to execute in a single cycle.

REGISTER 5-2: INTCON2: INTERRUPT CONTROL REGISTER 2

R/W-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0
ALTIVT	DISI	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	INT2EP	INT1EP	INT0EP
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **ALTIVT:** Enable Alternate Interrupt Vector Table bit
1 = Use alternate vector table
0 = Use standard (default) vector table

bit 14 **DISI:** DISI Instruction Status bit
1 = DISI instruction is active
0 = DISI instruction is not active

bit 13-3 **Unimplemented:** Read as ‘0’

bit 2 **INT2EP:** External Interrupt 2 Edge Detect Polarity Select bit
1 = Interrupt on negative edge
0 = Interrupt on positive edge

bit 1 **INT1EP:** External Interrupt 1 Edge Detect Polarity Select bit
1 = Interrupt on negative edge
0 = Interrupt on positive edge

bit 0 **INT0EP:** External Interrupt 0 Edge Detect Polarity Select bit
1 = Interrupt on negative edge
0 = Interrupt on positive edge

TABLE 6-1: dsPIC30F1010/2020 PORT REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
TRISA	02C0	—	—	—	—	—	—	TRISA9	—	—	—	—	—	—	—	—	—	0000 0010 0000 0000
PORTA	02C2	—	—	—	—	—	—	RA9	—	—	—	—	—	—	—	—	—	0000 0000 0000 0000
LATA	02C4	—	—	—	—	—	—	LAT9	—	—	—	—	—	—	—	—	—	0000 0000 0000 0000
TRISB	02C6	—	—	—	—	—	—	—	—	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	0000 0000 0011 1111
PORTB	02C8	—	—	—	—	—	—	—	—	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	0000 0000 0000 0000
LATB	02CA	—	—	—	—	—	—	—	—	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	0000 0000 0000 0000
TRISD	02D2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRISD0	0000 0000 0000 0001
PORTD	02D4	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RD0	0000 0000 0000 0000
LATD	02D6	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	LATD0	0000 0000 0000 0000
TRISE	02D8	—	—	—	—	—	—	—	—	TRSE7	TRSE6	TRISE5	TRISE4	TRISE3	TRISE2	TRISE1	TRISE0	0000 0000 1111 1111
PORTE	02DA	—	—	—	—	—	—	—	—	RE7	RE6	RE5	RE4	RE3	RE2	RE1	RE0	0000 0000 0000 0000
LATE	02DC	—	—	—	—	—	—	—	—	LATE7	LATE6	LATE5	LATE4	LATE3	LATE2	LATE1	LATE0	0000 0000 0000 0000
TRISF	02DE	—	—	—	—	—	—	—	TRISF8	TRISF7	TRISF6	—	—	—	—	—	—	0000 0001 1100 0000
PORTF	02E0	—	—	—	—	—	—	—	RF8	RF7	RF6	—	—	—	—	—	—	0000 0000 0000 0000
LATF	02E2	—	—	—	—	—	—	—	LATF8	LATF7	LATF6	—	—	—	—	—	—	0000 0000 0000 0000

Note: Refer to the "*dsPIC30F Family Reference Manual*" (DS70046) for descriptions of register bit fields.

REGISTER 12-2: PTPER: PRIMARY TIME BASE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTPER <15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
PTPER <7:3>					—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-3 Primary Time Base (PTMR) Period Value bits

bit 2-0 **Unimplemented:** Read as ‘0’

REGISTER 12-3: SEVTCMP: PWM SPECIAL EVENT COMPARE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SEVTCMP <15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
SEVTCMP <7:3>					—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

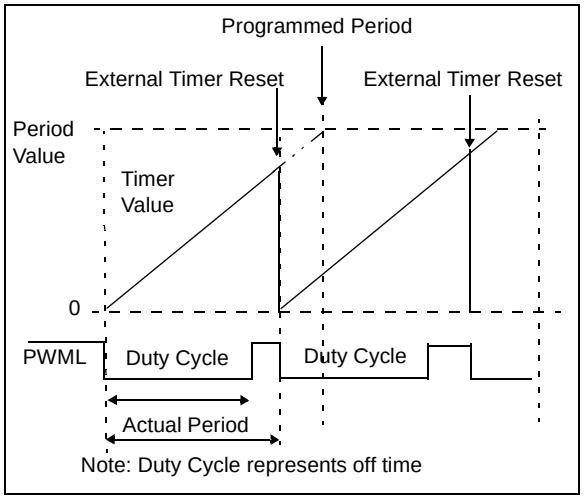
bit 15-3 Special Event Compare Count Value bits

bit 2-0 **Unimplemented:** Read as ‘0’

12.4.7 CONSTANT OFF-TIME PWM

Constant Off-Time mode is shown in Figure 12-9. Constant Off-Time PWM is a variable-frequency mode where the actual PWM period is less than or equal to the specified period value. The PWM time base is externally reset some time after the PWM signal duty cycle value has been reached, and the PWM signal has been deasserted. This mode is implemented by enabling the On-Time PWM mode (Current Reset mode) and using the complementary output.

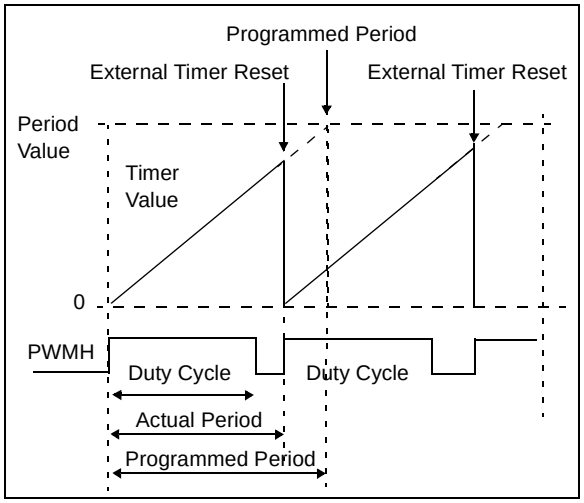
FIGURE 12-9: CONSTANT OFF-TIME PWM



12.4.8 CURRENT RESET PWM MODE

Current Reset PWM is shown in Figure 12-10. Current Reset PWM uses a Variable-Frequency mode where the actual PWM period is less than or equal to the specified period value. The PWM time base is externally reset some time after the PWM signal duty cycle value has been reached and the PWM signal has been deasserted. Current Reset PWM is a constant on-time PWM mode.

FIGURE 12-10: CURRENT RESET PWM

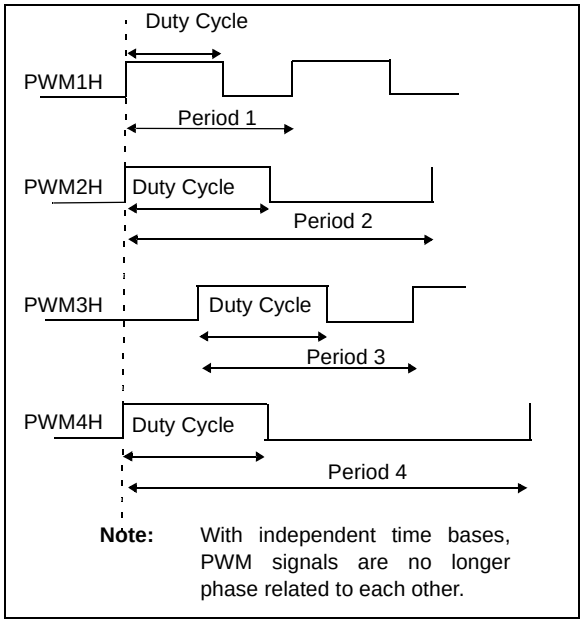


Typically, in the converter application, an energy storage inductor is charged with current while the PWM signal is asserted, and the inductor current is discharged by the load when the PWM signal is deasserted. In this application of current reset PWM, an external current measurement circuit determines when the inductor is discharged, and then generates a signal that the PWM module uses to reset the time base counter. In Current Reset mode, complementary outputs are available.

12.4.9 INDEPENDENT TIME BASE PWM

Independent Time Base PWM, as shown in Figure 12-11, is often used when the dsPIC DSC is controlling different power converter subcircuits such as the Power Factor Correction circuit, which may use 100 kHz PWM, and the full-bridge forward converter section may use 250 kHz PWM.

FIGURE 12-11: INDEPENDENT TIME BASE PWM



The FLTLEBEN and CLLEBEN bits enable the application of the blanking period to the selected Fault and current-limit inputs.

The LEB duration @ 30 MIPS = (LEB<9:3> + 1)/120 MHz.

There is a blanking period offset of 8.4 nsec. Therefore a LEB<9:3> value of zero yields an effective blanking period of 8.4 ns.

If a current-limit or Fault inputs are active at the end of the previous PWM cycle, and they are still active at the start of the new PWM cycle and the dead time is non-zero, the Fault or current limit will be detected regardless of the LEB counter configuration.

12.23 PWM Fault Pins

Each PWM generator can select its own Fault input source from a selection of up to 12 Fault/current-limit pins. In the FCLCONx registers, each PWM generator has control bits that specify the source for its Fault input signal. These are the FLTSRC<3:0> bits. Additionally, each PWM generator has a FLTIEN bit in the PWMCONx register that enables the generation of Fault interrupt requests. Each PWM generator has an associated Fault Polarity bit (FLTPOL) in the FCLCONx register that selects the active level of the selected Fault input.

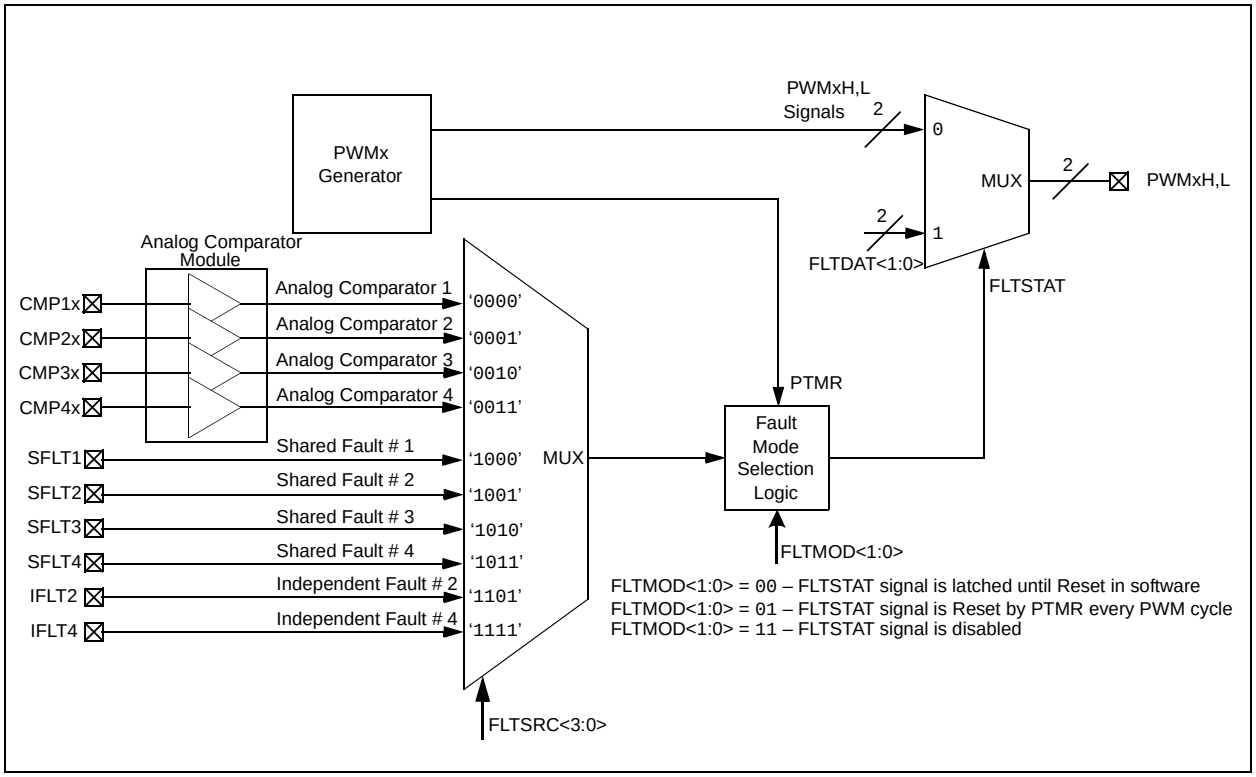
The Fault pins actually serve two different purposes. First is generation of Fault overrides for the PWM outputs. The action of overriding the PWM outputs and generating an interrupt is performed asynchronously in hardware so that Fault events can be managed quickly. Second, the Fault pin inputs can be used to implement either Current-Limit PWM mode or Current Force mode.

PWM Fault condition states are available on the FLTSTAT bit in the PWMCONx registers. The FLTSTAT bits displays the Fault IRQ latch if the FIE bit is set. If Fault interrupts are not enabled, then the FSTATx bits display the status of the selected FLTx input in positive logic format. When the Fault input pins are not used in association with a PWM generator, these pins become general purpose I/O or interrupt input pins.

The FLTx pins are normally active high. The FLTPOL bit in FCLCONx registers, if set to one, invert the selected Fault input signal so that it is an active low.

The Fault pins are also readable through the PORT I/O logic when the PWM module is enabled. This allows the user to poll the state of the Fault pins in software. Figure 12-20 is a diagram of the PWM Fault control logic.

FIGURE 12-20: PWM FAULT CONTROL LOGIC DIAGRAM



16.18 Module Power-Down Modes

The module has two internal power modes.

When the ADON bit is '1', the module is in Active mode and is fully powered and functional.

When ADON is '0', the module is in Off mode. The state machine for the module is reset, as are all of the pending conversion requests.

To return to the Active mode from Off mode, the user must wait for the bias generators to stabilize. The stabilization time is specified in the electrical specs.

16.19 Effects of a Reset

A device Reset forces all registers to their Reset state. This forces the ADC module to be turned off, and any conversion and sampling sequence is aborted. The value that is in the ADCBUFx register is not modified.

The ADCBUFx registers contain unknown data after a Power-on Reset.

16.20 Configuring Analog Port Pins

The use of the ADPCFG and TRIS registers control the operation of the A/D port pins.

The port pins that are desired as analog inputs should have their corresponding TRIS bit set (input). If the TRIS bit is cleared (output), the digital output level (V_{OH} or V_{OL}) will be converted.

Port pins that are desired as analog inputs must have the corresponding ADPCFG bit clear. This will configure the port to disable the digital input buffer. Analog levels on pins where ADPCFG<n> = 1, may cause the digital input buffer to consume excessive current.

If a pin is not configured as an analog input ADPCFG<n> = 1, the analog input is forced to AVss, and conversions of that input do not yield meaningful results.

When reading the PORT register, all pins configured as analog input ADPCFG<n> = 0 will read '0'.

The A/D operation is independent of the state of the input selection bits and the TRIS bits.

16.21 Output Formats

The A/D converts 10 bits. The data buffer RAM is 16 bits wide. The ADC data can be read in one of two different formats, as shown in Figure 16-5. The FORM bit selects the format. Each of the output formats translates to a 16-bit result on the data bus.

18.6 INTERNAL FAST RC OSCILLATOR (FRC)

FRC is a fast, precise frequency internal RC oscillator. The FRC oscillator is designed to run at a frequency of 6.4/9.7/14.55 MHz (<±2% accuracy). The FRC oscillator option is intended to be accurate enough to provide the clock frequency necessary to maintain baud rate tolerance for serial data transmissions. The user has the ability to tune the FRC frequency by +-3%.

The FRC oscillator is powered:

a) Any time the EC or HS Oscillator modes are NOT selected.
b) When the fail-safe clock monitor is enabled and a clock fail is detected, forcing a switch to FRC.

18.6.1 FREQUENCY RANGE SELECTION

The FRC module has a “Gear Shift” control signal that selects low range (9.7 MHz for industrial temperature rated parts and 6.4 MHz for extended temperature rated parts) or high range (14.55 MHz for industrial temperture rated parts and 9.7 MHz for extended temperature rated parts) frequency of operation. This feature enables a dsPIC DSC device to operate up to a maiximum speed of 20 MIPS at 3.3V or up to a maximum speed of 30 MIPS at 5.0V and remain with system specifications.

18.6.2 NOMINAL FREQUENCY VALUES

The FRC module is calibrated to a nominal 9.7 MHz for industrial temperature rated parts and 6.4 MHz for extended temperature rated parts in low range and 14.55 MHz for industrial temperture rated parts and 9.7 MHz for extended temperature rated parts in high range This feature enables a user to “tune” the dsPIC DSC device frequency of operation by +-3% and still remain within system specifications.

18.6.3 FRC FREQUENCY USER TUNING

The FRC is calibrated at the factory to give a nominal 6.4/9.7/14.55 MHz. The TUN<3:0> field in the OSCTUN register is available to the user for trimming the FRC oscillator frequency in applications.

The 4-bit tuning control signals are supplied by the OSCTUN or the OSCTUN2 registers depending on the TSEQEN bit in the OSCCON register.

The tuning range of the 14.55 MHz oscillator is ±0.45 MHz (±3%) nominal.

The base frequency can be tuned in the user's application. This frequency tuning capability allows the user to deviate from the factory calibrated frequency. The user can tune the frequency by writing to the OSCTUN register TUN<3:0> bits.

18.6.4 CLOCK DITHERING LOGIC

In power conversion applications, the primary electrical noise emission that the designers want to reduce is caused by the power transistors switching at the PWM frequency. By changing the system clock frequency of the SMPS dsPIC DSC, the resultant PWM frequency will change and the peak EMI will be reduced at the noise is spread over a wider frequency range.
Typically, the range of frequency variation is few percent. The dsPIC30F1010/202X can provide two ways to vary system clock frequency on a PWM cycle basis. These are Frequency Sequencing mode and Pseudo Random Clock Dithering mode. Table 18-8 shows the implementation details of both these methods.

18.6.5 FREQUENCY SEQUENCING MODE

The Frequency Sequencing mode enables the PWM module to select a sequence of eight different FRC TUN values to vary the system frequency with each rollover of the primary PWM time base. The OSCTUN and the OSCTUN2 registers allow the user to specify eight sequential tune values if the TSEQEN bit is set in the OSCCON register. If the TSEQEN bit is zero, then only the TUN bits affect the FRC frequency.

A 4-bit wide multiplexer with eight sets of inputs selects the tuning value from the TUN and the TSEQx bit fields. The multiplexer is controlled by the ROLL<5:3> counter in the PWM module. The ROLL<5:3> counter increments every time the primary time base rolls over after reaching the period value.

18.6.6 PSEUDO RANDOM CLOCK DITHERING MODE

The Pseudo Random Clock Dither (PRCD) logic is implemented with a 15-bit LFSR (Linear Feedback Shift Register), which is a shift register with a few exclusive OR gates. The lower four bits of the LFSR provides the FRC TUNE bits. The PRCD feature is enabled by setting the PRCDEN bit in the OSCCON register. The LSFR is “clocked” (enabled to clock) once every time the ROLL<3> bit changes state, which occurs once every 8 PWM cycles.

18.6.7 FAIL-SAFE CLOCK MONITOR

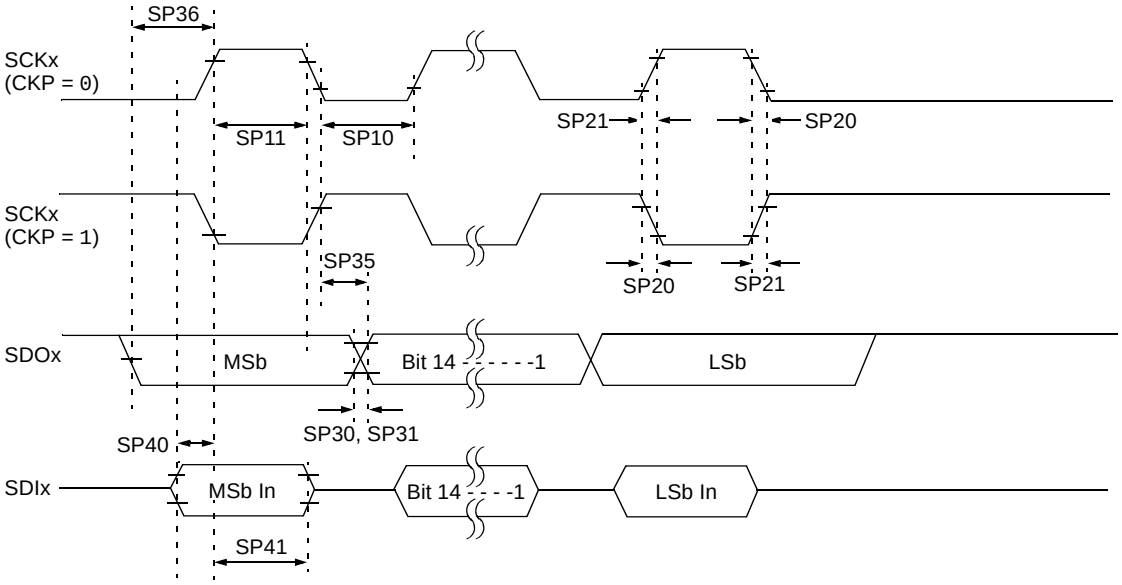
The Fail-Safe Clock Monitor (FSCM) allows the device to continue to operate even in the event of an oscillator failure. The FSCM function is enabled by appropriately programming the FCKSM Configuration bits (Clock Switch and Monitor Selection bits) in the FOSC Configuration register.

In the event of an oscillator failure, the FSCM will generate a clock failure trap event and will switch the system clock over to the FRC oscillator. The user will then have the option to either attempt to restart the oscillator or execute a controlled shutdown. The user may decide to treat the trap as a warm Reset by sim-

TABLE 19-1: SYMBOLS USED IN OPCODE DESCRIPTIONS (CONTINUED)

Field	Description
Wb	Base W register ∈ {W0..W15}
Wd	Destination W register ∈ { Wd, [Wd], [Wd++], [Wd--], [++Wd], [--Wd] }
Wdo	Destination W register ∈ { Wnd, [Wnd], [Wnd++], [Wnd--], [++Wnd], [--Wnd], [Wnd+Wb] }
Wm,Wn	Dividend, Divisor working register pair (direct addressing)
Wm*Wm	Multiplicand and Multiplier working register pair for Square instructions ∈ {W4 * W4,W5 * W5,W6 * W6,W7 * W7}
Wm*Wn	Multiplicand and Multiplier working register pair for DSP instructions ∈ {W4 * W5,W4 * W6,W4 * W7,W5 * W6,W5 * W7,W6 * W7}
Wn	One of 16 working registers ∈ {W0..W15}
Wnd	One of 16 destination working registers ∈ {W0..W15}
Wns	One of 16 source working registers ∈ {W0..W15}
WREG	W0 (working register used in file register instructions)
Ws	Source W register ∈ { Ws, [Ws], [Ws++], [Ws--], [++Ws], [--Ws] }
Wso	Source W register ∈ { Wns, [Wns], [Wns++], [Wns--], [++Wns], [--Wns], [Wns+Wb] }
Wx	X data space prefetch address register for DSP instructions ∈ {[W8] + = 6, [W8] + = 4, [W8] + = 2, [W8], [W8] – = 6, [W8] – = 4, [W8] – = 2, [W9] + = 6, [W9] + = 4, [W9] + = 2, [W9], [W9] – = 6, [W9] – = 4, [W9] – = 2, [W9 + W12],none}
Wxd	X data space prefetch destination register for DSP instructions ∈ {W4..W7}
Wy	Y data space prefetch address register for DSP instructions ∈ {[W10] + = 6, [W10] + = 4, [W10] + = 2, [W10], [W10] - = 6, [W10] - = 4, [W10] - = 2, [W11] + = 6, [W11] + = 4, [W11] + = 2, [W11], [W11] – = 6, [W11] – = 4, [W11] – = 2, [W11 + W12], none}
Wyd	Y data space prefetch destination register for DSP instructions ∈ {W4..W7}

FIGURE 21-13: SPIx MODULE MASTER MODE (CKE = 1) TIMING CHARACTERISTICS



Note: Refer to Figure 21-1 for load conditions.

TABLE 21-28: SPIx MODULE MASTER MODE (CKE = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.3V and 5.0V (±10%) (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic(1)**	**Min**	**Typ(2)**	**Max**	**Units**	**Conditions**
SP10	TscL	SCKx Output Low Time(3)	TCY/2	—	—	ns	
SP11	TscH	SCKx Output High Time(3)	TCY/2	—	—	ns	
SP20	TscF	SCKx Output Fall Time(4)	—	—	—	ns	See Parameter D032
SP21	TscR	SCKx Output Rise Time(4)	—	—	—	ns	See Parameter D031
SP30	TdoF	SDOx Data Output Fall Time(4)	—	—	—	ns	See Parameter D032
SP31	TdoR	SDOx Data Output Rise Time(4)	—	—	—	ns	See Parameter D031
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	—	30	ns	
SP36	TdoV2sc, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	20	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	20	—	—	ns	

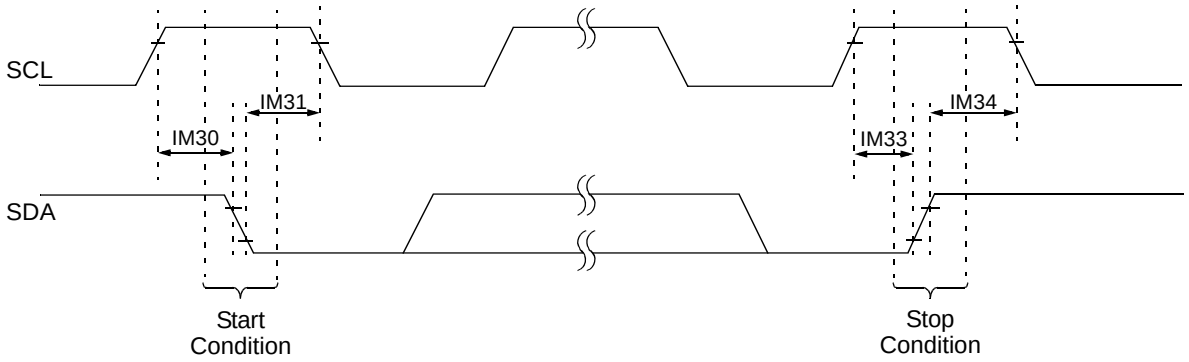
Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ" column is at 5V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCKx is 100 ns. Therefore, the clock generated in Master mode must not violate this specification.

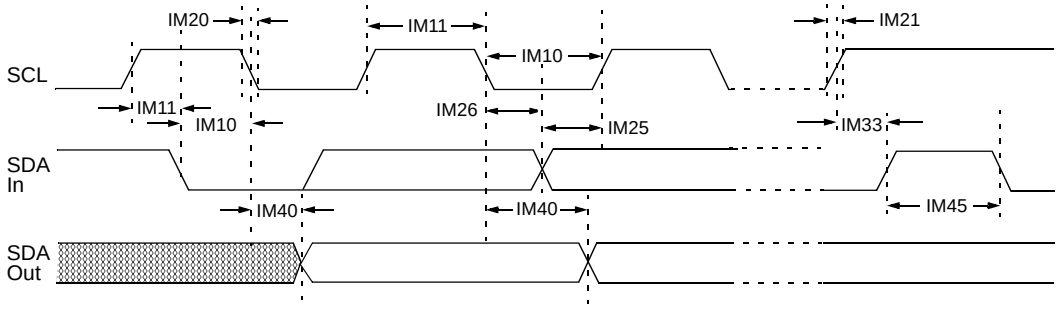
4: Assumes 50 pF load on all SPIx pins.

FIGURE 21-16: I²C™ BUS START/STOP BITS TIMING CHARACTERISTICS (MASTER MODE)



Note: Refer to Figure 21-1 for load conditions.

FIGURE 21-17: I²C™ BUS DATA TIMING CHARACTERISTICS (MASTER MODE)



Note: Refer to Figure 21-1 for load conditions.

TABLE 21-33: 10-BIT HIGH-SPEED A/D MODULE SPECIFICATIONS

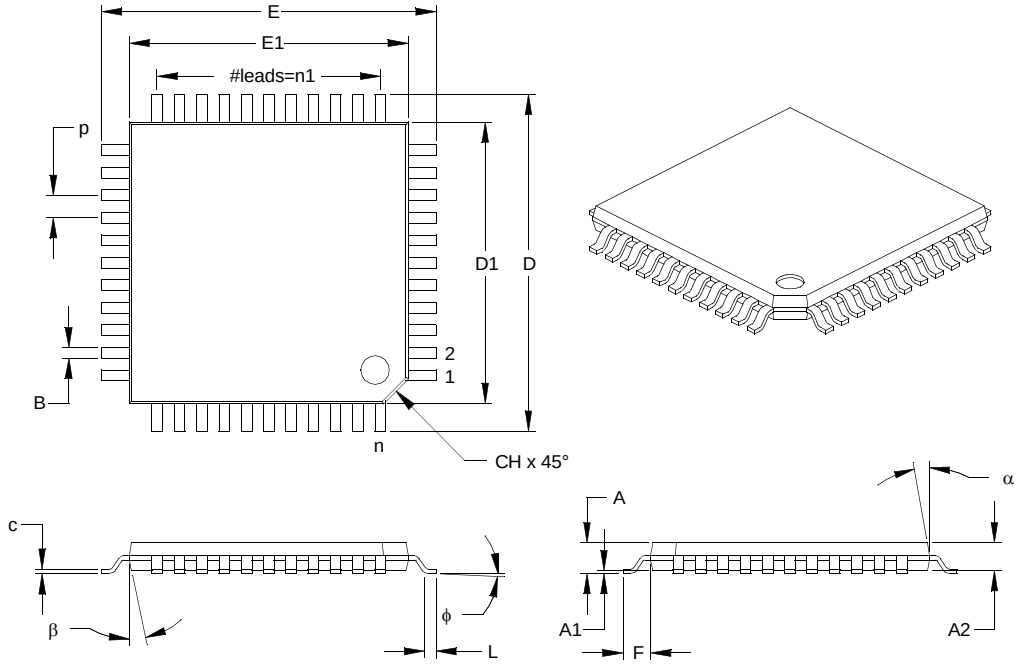
AC CHARACTERISTICS			Standard Operating Conditions: 3.3V and 5.0V (±10%) (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ**	**Max.**	**Units**	**Conditions**
Device Supply							
AD01	AVDD	Module VDD Supply	Greater of: VDD – 0.3 or 2.7		Lesser of: VDD + 0.3 or 5.5	V	
AD02	AVSS	Module VSS Supply	Vss – 0.3		VSS + 0.3	V	
Analog Input							
AD10	VINH-VINL	Full-Scale Input Span	VSS		VDD	V	
AD11	VIN	Absolute Input Voltage	AVSS – 0.3		AVDD + 0.3	V	
AD12	—	Leakage Current	—	±0.001	±0.244	µA	VINL = AVSS = 0V, AVDD = 5V, Source Impedance = 1 kΩ
AD13	—	Leakage Current	—	±0.001	±0.244	µA	VINL = AVSS = 0V, AVDD = 3.3V, Source Impedance = 1 kΩ
AD17	RIN	Recommended Impedance of Analog Voltage Source	—		1K	Ω	
DC Accuracy							
AD20	Nr	Resolution	10 data bits			bits	
AD21	INL	Integral Nonlinearity	—	±0.5	< ±1	LSb	VINL = AVSS = 0V, AVDD = 5V
AD21A	INL	Integral Nonlinearity	—	±0.5	< ±1	LSb	VINL = AVSS = 0V, AVDD = 3.3V
AD22	DNL	Differential Nonlinearity	—	±0.5	< ±1	LSb	VINL = AVSS = 0V, AVDD = 5V
AD22A	DNL	Differential Nonlinearity	—	±0.5	< ±1	LSb	VINL = AVSS = 0V, AVDD = 3.3V
AD23	GERR	Gain Error	—	±0.75	<±4.0	LSb	VINL = AVSS = 0V, AVDD = 5V
AD23A	GERR	Gain Error	—	±0.75	<±3.0	LSb	VINL = AVSS = 0V, AVDD = 3.3V

Note 1: Because the sample caps will eventually lose charge, clock rates below 10 kHz can affect linearity performance, especially at elevated temperatures.

2: The A/D conversion result never decreases with an increase in the input voltage, and has no missing codes.

44-Lead Plastic Thin Quad Flatpack (PT) 10x10x1 mm Body, 1.0/0.10 mm Lead Form (TQFP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		44			44	
Pitch	p		.031			0.80	
Pins per Side	n1		11			11	
Overall Height	A	.039	.043	.047	1.00	1.10	1.20
Molded Package Thickness	A2	.037	.039	.041	0.95	1.00	1.05
Standoff	A1	.002	.004	.006	0.05	0.10	0.15
Foot Length	L	.018	.024	.030	0.45	0.60	0.75
Footprint (Reference)	F		.039 REF.			1.00 REF.	
Foot Angle	ϕ	0	3.5	7	0	3.5	7
Overall Width	E	.463	.472	.482	11.75	12.00	12.25
Overall Length	D	.463	.472	.482	11.75	12.00	12.25
Molded Package Width	E1	.390	.394	.398	9.90	10.00	10.10
Molded Package Length	D1	.390	.394	.398	9.90	10.00	10.10
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.012	.015	.017	0.30	0.38	0.44
Pin 1 Corner Chamfer	CH	.025	.035	.045	0.64	0.89	1.14
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

***** Controlling Parameter

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

REF: Reference Dimension, usually without tolerance, for information purposes only.

See ASME Y14.5M

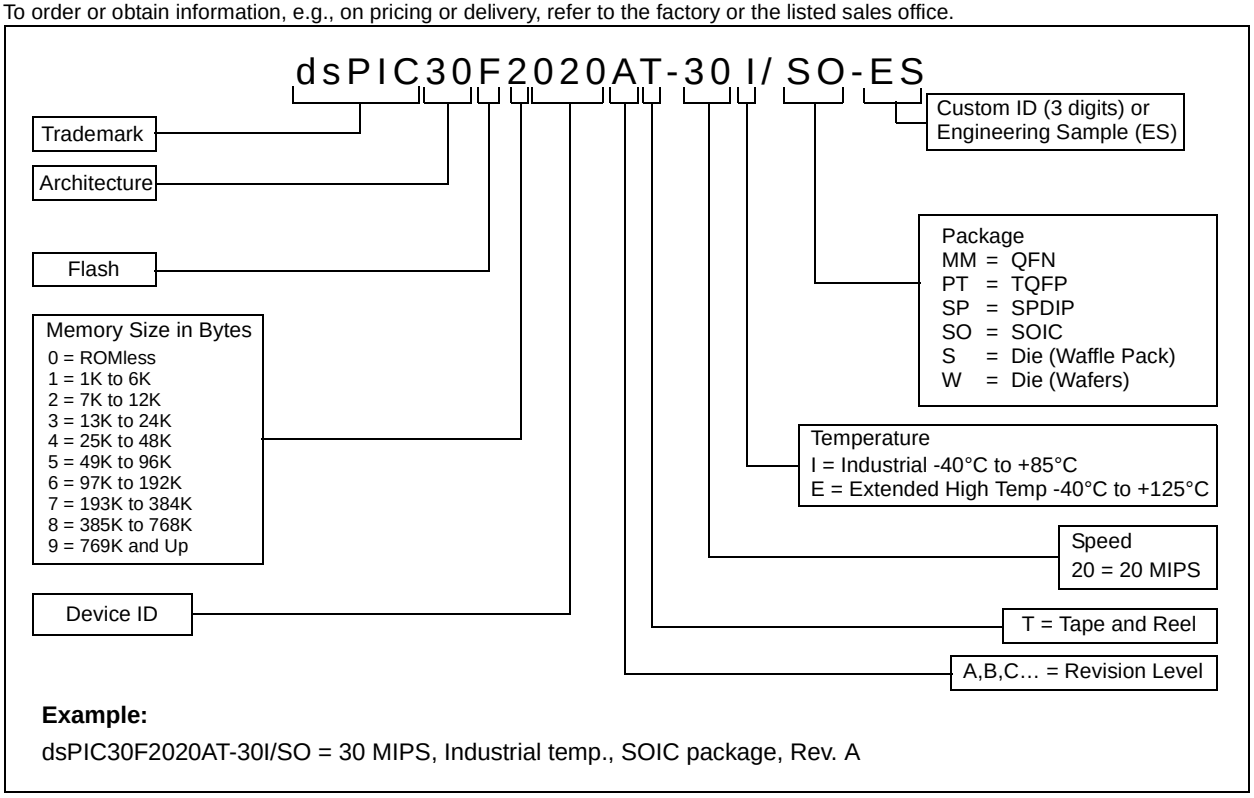
JEDEC Equivalent: MS-026

Drawing No. C04-076

Revised 07-22-05

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



Example:

dsPIC30F2020AT-30I/SO = 30 MIPS, Industrial temp., SOIC package, Rev. A

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