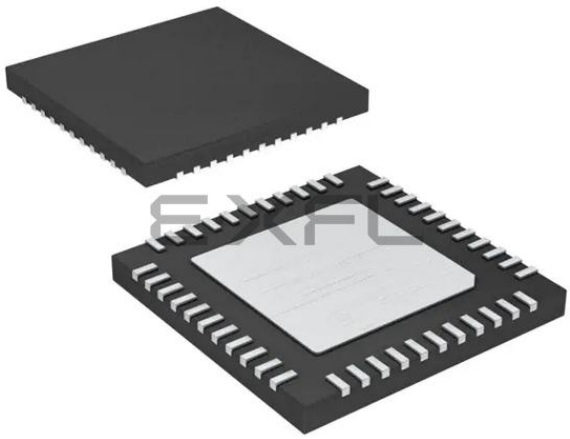

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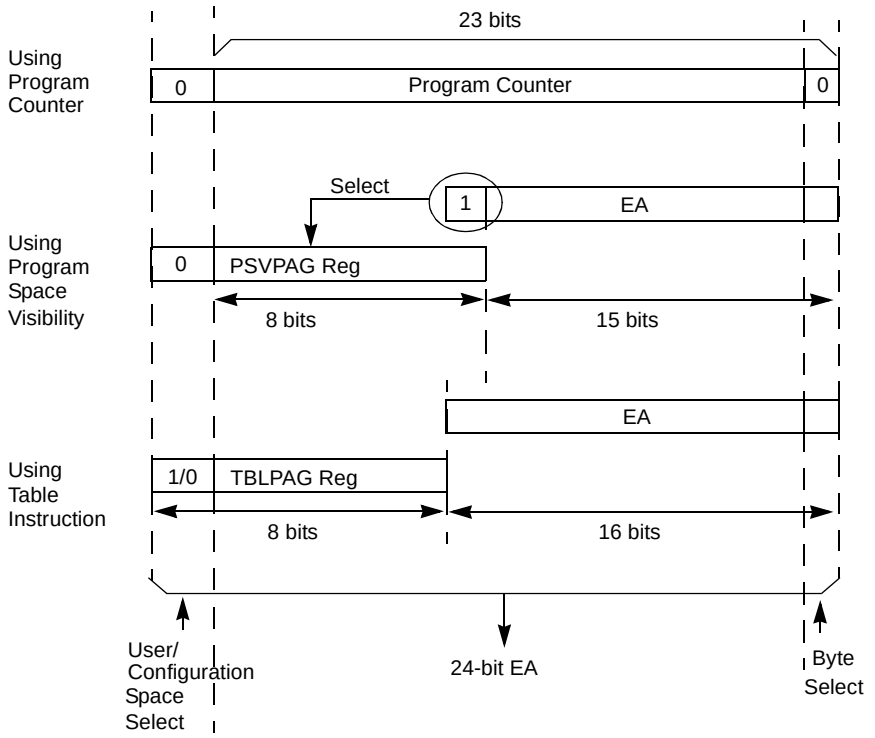
Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	20 MIPS
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	35
Program Memory Size	12KB (4K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic30f2023-20e-ml

TABLE 3-1: PROGRAM SPACE ADDRESS CONSTRUCTION

Access Type	Access Space	Program Space Address				
		<23>	<22:16>	<15>	<14:1>	<0>
Instruction Access	User	0	PC<22:1>			0
TBLRD/TBLWT	User (TBLPAG<7> = 0)	TBLPAG<7:0>		Data EA <15:0>		
TBLRD/TBLWT	Configuration (TBLPAG<7> = 1)	TBLPAG<7:0>		Data EA <15:0>		
Program Space Visibility	User	0	PSVPAG<7:0>		Data EA <14:0>	

FIGURE 3-2: DATA ACCESS FROM PROGRAM SPACE ADDRESS GENERATION



Note: Program Space Visibility cannot be used to access bits <23:16> of a word in program memory.

5.0 INTERRUPTS

Note: This data sheet summarizes features of this group of dsPIC30F devices and is not intended to be a complete reference source. For more information on the CPU, peripherals, register descriptions and general device functionality, refer to the "*dsPIC30F Family Reference Manual*" (DS70046). For more information on the device instruction set and programming, refer to the "*dsPIC30F/33F Programmer's Reference Manual*" (DS70157).

The dsPIC30F1010/202X device has up to 35 interrupt sources and 4 processor exceptions (traps), which must be arbitrated based on a priority scheme.

The CPU is responsible for reading the Interrupt Vector Table (IVT) and transferring the address contained in the interrupt vector to the Program Counter (PC). The interrupt vector is transferred from the program data bus into the Program Counter, via a 24-bit wide multiplexer on the input of the Program Counter.

The Interrupt Vector Table and Alternate Interrupt Vector Table (AIVT) are placed near the beginning of program memory (0x000004). The IVT and AIVT are shown in Figure 5-1.

The interrupt controller is responsible for preprocessing the interrupts and processor exceptions, prior to their being presented to the processor core. The peripheral interrupts and traps are enabled, prioritized and controlled using centralized special function registers:

- IFS0<15:0>, IFS1<15:0>, IFS2<15:0>
  All interrupt request flags are maintained in these three registers. The flags are set by their respective peripherals or external signals, and they are cleared via software.
- IEC0<15:0>, IEC1<15:0>, IEC2<15:0>
  All interrupt enable control bits are maintained in these three registers. These control bits are used to individually enable interrupts from the peripherals or external signals.
- IPC0<15:0>... IPC11<7:0>
  The user-assignable priority level associated with each of these interrupts is held centrally in these twelve registers.
- IPL<3:0> The current CPU priority level is explicitly stored in the IPL bits. IPL<3> is present in the CORCON register, whereas IPL<2:0> are present in the STATUS Register (SR) in the processor core.
- INTCON1<15:0>, INTCON2<15:0>
  Global interrupt control functions are derived from these two registers. INTCON1 contains the control and status flags for the processor exceptions. The INTCON2 register controls the external interrupt request signal behavior and the use of the alternate vector table.
- The INTTREG register contains the associated interrupt vector number and the new CPU interrupt priority level, which are latched into vector number (VECNUM<6:0>) and Interrupt level (ILR<3:0>) bit fields in the INTTREG register. The new interrupt priority level is the priority of the pending interrupt.

Note: Interrupt flag bits get set when an Interrupt condition occurs, regardless of the state of its corresponding enable bit. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

All interrupt sources can be user assigned to one of 7 priority levels, 1 through 7, via the IPCx registers. Each interrupt source is associated with an interrupt vector, as shown in Figure 5-1. Levels 7 and 1 represent the highest and lowest maskable priorities, respectively.

Note: Assigning a priority level of 0 to an interrupt source is equivalent to disabling that interrupt.

If the NSTDIS bit (INTCON1<15>) is set, nesting of interrupts is prevented. Thus, if an interrupt is currently being serviced, processing of a new interrupt is prevented, even if the new interrupt is of higher priority than the one currently being serviced.

Note: The IPL bits become read-only whenever the NSTDIS bit has been set to '1'.

Certain interrupts have specialized control bits for features like edge or level triggered interrupts, interrupt-on-change, etc. Control of these features remains within the peripheral module that generates the interrupt.

The `DISI` instruction can be used to disable the processing of interrupts of priorities 6 and lower for a certain number of instructions, during which the DISI bit (INTCON2<14>) remains set.

When an interrupt is serviced, the PC is loaded with the address stored in the vector location in Program Memory that corresponds to the interrupt. There are 63 different vectors within the IVT (refer to Figure 5-1). These vectors are contained in locations 0x000004 through 0x0000FE of program memory (refer to Figure 5-1). These locations contain 24-bit addresses, and, in order to preserve robustness, an address error trap will take place should the PC attempt to fetch any of these words during normal execution. This prevents execution of random data as a result of accidentally decrementing a PC into vector space, accidentally mapping a data space address into vector space, or the PC rolling over to 0x000000 after reaching the end of implemented program memory space. Execution of a `GOTO` instruction to this vector space will also generate an address error trap.

REGISTER 5-18: IPC9: INTERRUPT PRIORITY CONTROL REGISTER 9

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	ADCP2IP<2:0>			—	ADCP1IP<2:0>		
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	ADCP0IP<2:0>			—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **ADCP2IP<2:0>:** ADC Pair 2 Conversion Done Interrupt Priority bits
111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as ‘0’

bit 10-8 **ADCP1IP<2:0>:** ADC Pair 1 Conversion Done Interrupt Priority bits
111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **ADCP0IP<2:0>:** ADC Pair 0 Conversion Done Interrupt Priority bits
111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

bit 3-0 **Unimplemented:** Read as ‘0’

7.6.3 LOADING WRITE LATCHES

Example 7-2 shows a sequence of instructions that can be used to load the 96 bytes of write latches. 32 TBLWTL and 32 TBLWTH instructions are needed to load the write latches selected by the table pointer.

EXAMPLE 7-2: LOADING WRITE LATCHES

```
; Set up a pointer to the first program memory location to be written
; program memory selected, and writes enabled
       MOV     #0x0000,W0                      ;
       MOV     W0,TBLPAG                       ; Initialize PM Page Boundary SFR
       MOV     #0x6000,W0                      ; An example program memory address
; Perform the TBLWT instructions to write the latches
; 0th_program_word
       MOV     #LOW_WORD_0,W2                  ;
       MOV     #HIGH_BYTE_0,W3                 ;
       TBLWTL  W2,[W0]                         ; Write PM low word into program latch
       TBLWTH  W3,[W0++]                       ; Write PM high byte into program latch
; 1st_program_word
       MOV     #LOW_WORD_1,W2                  ;
       MOV     #HIGH_BYTE_1,W3                 ;
       TBLWTL  W2,[W0]                         ; Write PM low word into program latch
       TBLWTH  W3,[W0++]                       ; Write PM high byte into program latch
;  2nd_program_word
       MOV     #LOW_WORD_2,W2                  ;
       MOV     #HIGH_BYTE_2,W3                 ;
       TBLWTL  W2, [W0]                        ; Write PM low word into program latch
       TBLWTH  W3, [W0++]                      ; Write PM high byte into program latch
       •
       •
       •
; 31st_program_word
       MOV     #LOW_WORD_31,W2                 ;
       MOV     #HIGH_BYTE_31,W3                ;
       TBLWTL  W2, [W0]                        ; Write PM low word into program latch
       TBLWTH  W3, [W0++]                      ; Write PM high byte into program latch
```

Note: In Example 7-2, the contents of the upper byte of W3 have no effect.

7.6.4 INITIATING THE PROGRAMMING SEQUENCE

For protection, the write initiate sequence for NVMKEY must be used to allow any erase or program operation to proceed. After the programming command has been executed, the user must wait for the programming time until programming is complete. The two instructions following the start of the programming sequence should be NOPs.

EXAMPLE 7-3: INITIATING A PROGRAMMING SEQUENCE

```
       DISI    #5                      ; Block all interrupts with priority <7
                                       ; for next 5 instructions
       MOV     #0x55,W0
       MOV     W0,NVMKEY               ; Write the 0x55 key
       MOV     #0xAA,W1                ;
       MOV     W1,NVMKEY               ; Write the 0xAA key
       BSET    NVMCON,#WR              ; Start the erase sequence
       NOP                             ; Insert two NOPs after the erase
       NOP                             ; command is asserted
```

11.4.1 PWM PERIOD

The PWM period is specified by writing to the PRx register. The PWM period can be calculated using Equation 11-1.

EQUATION 11-1: PWM PERIOD

$$\text{PWM period} = [(\text{PRx}) + 1] \cdot 4 \cdot T_{OSC} \cdot (\text{TMRx prescale value})$$

PWM frequency is defined as 1/[PWM period].

When the selected TMRx is equal to its respective period register, PRx, the following four events occur on the next increment cycle:

- TMRx is cleared.
- The OCx pin is set.
  - Exception 1: If PWM duty cycle is 0x0000, the OCx pin will remain low.
  - Exception 2: If duty cycle is greater than PRx, the pin will remain high.
- The PWM duty cycle is latched from OCxRS into OCxR.
- The corresponding timer interrupt flag is set.

See Figure 11-1 for key PWM period comparisons. Timer3 is referred to in the figure for clarity.

11.4.2 PWM WITH FAULT PROTECTION INPUT PIN

When control bits OCM<2:0> (OCxCON<2:0>) = 111, Fault protection is enabled via the OCFLTA pin. If the a logic '0' is detected on the OCFLTA pin, the output pins are placed in a high-impedance state. The state remains until:

- the external Fault condition has been removed **and**
- the PWM mode is reenabled by writing to the appropriate control bits

As a result of the Fault condition, the OCxIF interrupt is asserted, and an interrupt will be generated, if enabled. Upon detection of the Fault condition, the OCFLTx bit in the OCxCON register is asserted high. This bit is a read-only bit and will be cleared once the external Fault condition has been removed, and the PWM mode is reenabled by writing the appropriate mode bits, OCM<2:0> in the OCxCON register.

11.5 Output Compare Operation During CPU Sleep Mode

When the CPU enters the Sleep mode, all internal clocks are stopped. Therefore, when the CPU enters the Sleep state, the output compare channel will drive the pin to the active state that was observed prior to entering the CPU Sleep state.

For example, if the pin was high when the CPU entered the Sleep state, the pin will remain high. Likewise, if the pin was low when the CPU entered the Sleep state, the pin will remain low. In either case, the output compare module will resume operation when the device wakes up.

11.6 Output Compare Operation During CPU Idle Mode

When the CPU enters the Idle mode, the output compare module can operate with full functionality.

The output compare channel will operate during the CPU Idle mode if the OCSIDL bit (OCxCON<13>) is at logic '0' and the selected time base (Timer2 or Timer3) is enabled and the TSIDL bit of the selected timer is set to logic '0'.

12.36 EXTERNAL SYNCHRONIZATION FEATURES

In large power conversion systems, it is often desirable to be able to synchronize multiple power controllers to ensure that “beat frequencies” are not generated within the system, or as a means to ensure “quiet” periods during which current and voltage measurements can be made.

dsPIC30F202X devices (excluding 28-pin packages) have input and/or output pins that provide the capability to either synchronize the SMPS dsPIC DSC device with an external device or have external devices synchronized to the SMPS dsPIC DSC. These synchronizing features are enabled via the SYNCIEN and SYNCOEN bits in the PTCON control register in the PWM module.

The SYNCPOL bit in the PTCON register selects whether the rising edge or the falling edge of the SYNCI signal is the active edge. The SYNCPOL bit in the PTCON register also selects whether the SYNCO output pulse is low active or high active.

The SYNCSRC<2:0> bits in the PTCON register specify the source for the SYNCI signal.

If the SYNCI feature is enabled, the primary time base counter is reset when an active SYNCI edge is detected. If the SYNCO feature is enabled, an output pulse is generated when the primary time base counter rolls over at the end of a PWM cycle.

The recommended SYNCI pulse width should be more than 100 nsec. The expected SYNCO output pulse width will be approximately 100 nsec.

When using the SYNCI feature, it is recommended that the user program the period register with a period value that is slightly longer than the expected period of the external synchronization input signal. This provides protection in case the SYNCI signal is not received due to noise or external component failure. With a reasonable period value programmed into the PTPER register, the local power conversion process should remain operational even if the global synchronization signal is not received.

12.37 CPU LOAD STAGGERING

The SMPS dsPIC DSC has the ability to stagger the individual trigger comparison operations. This feature helps to level the processor’s workload to minimize situations where the processor is overloaded.

Assume a situation where there are four PWM channels controlling four independent voltage outputs. Assume further that each PWM generator is operating at 1000 kHz (1 µsec period) and each control loop is operating at 125 kHz (8 µsec).

The TRGDIV<2:0> bits in each TRGCONx register will be set to ‘111’, which selects that every 8th trigger comparison match will generate a trigger signal to the ADC to capture data and begin a conversion process.

If the stagger-in-time feature did not exist, all of the requests from all of the PWM trigger registers might occur at the same time. If this “pile-up” were to happen, some data sample might become stale (outdated) by the time the data for all four channels can be processed.

With the stagger-in-time feature, the trigger signals are spaced out over time (during succeeding PWM periods) so that all of the data is processed in an orderly manner.

The ROLL counter is a counter connected to the primary time base counter. The ROLL counter is incremented each time the primary time base counter reaches terminal count (period rollover).

The stagger-in-time feature is controlled by the TRGSTRT<5:0> bits in the TRGCONx registers. The TRGSTRT<5:0> bits specify the count value of the ROLL counter that must be matched before an individual trigger comparison module in each of the PWM generators can begin to count the trigger comparison events as specified by the TRGDIV<2:0> bits in the PWMCONx registers.

So, in our example with the four PWM generators, the first PWM’s TRGSTRT<5:0> bits would be ‘000’, the second PWM’s TRGSTRT bits would be set to ‘010’, the third PWM’s TRGSTRT bits would be set to ‘100’ and the fourth PWM’s TRGSTRT bits would be set to ‘110’. Therefore, over a total of eight PWM cycles, the four separate control loops could be run each with their own 2-µsec time period.

12.38 EXTERNAL TRIGGER BLANKING

Using the LEB<9:3> bits in the LEBCONx registers, the PWM module has the capability to blank (ignore) the external current and Fault inputs for a period of 0 to 1024 nsec. This feature is useful if power transistor turn-on induced transients make current sensing difficult at the start of a PWM cycle.

REGISTER 13-2: SPIxCON1: SPIx CONTROL REGISTER 1

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	DISSCK	DISSDO	MODE16	SMP	CKE(1)
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SSEN	CKP	MSTEN	SPRE<2:0>			PPRE<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12 **DISSCK:** Disable SCKx pin bit (SPI Master modes only)
1 = Internal SPI clock is disabled, pin functions as I/O
0 = Internal SPI clock is enabled

bit 11 **DISSDO:** Disable SDOx pin bit
1 = SDOx pin is not used by module; pin functions as I/O
0 = SDOx pin is controlled by the module

bit 10 **MODE16:** Word/Byte Communication Select bit
1 = Communication is word-wide (16 bits)
0 = Communication is byte-wide (8 bits)

bit 9 **SMP:** SPIx Data Input Sample Phase bit
Master mode:
1 = Input data sampled at end of data output time
0 = Input data sampled at middle of data output time
Slave mode:
SMP must be cleared when SPIx is used in Slave mode.

bit 8 **CKE:** SPIx Clock Edge Select bit(1)
1 = Serial output data changes on transition from active clock state to Idle clock state (see bit 6)
0 = Serial output data changes on transition from Idle clock state to active clock state (see bit 6)

bit 7 **SSEN:** Slave Select Enable bit (Slave mode)
1 = $\overline{SSx}$ pin used for Slave mode
0 = $\overline{SSx}$ pin not used by module. Pin controlled by port function.

bit 6 **CKP:** Clock Polarity Select bit
1 = Idle state for clock is a high level; active state is a low level
0 = Idle state for clock is a low level; active state is a high level

bit 5 **MSTEN:** Master Mode Enable bit
1 = Master mode
0 = Slave mode

bit 4-2 **SPRE<2:0>:** Secondary Prescale bits (Master mode)
111 = Secondary prescale 1:1
110 = Secondary prescale 2:1
...
000 = Secondary prescale 8:1

bit 1-0 **PPRE<1:0>:** Primary Prescale bits (Master mode)
11 = Primary prescale 1:1
10 = Primary prescale 4:1
01 = Primary prescale 16:1
00 = Primary prescale 64:1

Note 1: The CKE bit is not used in the Framed SPI modes. The user should program this bit to '0' for the Framed SPI modes (FRMEN = 1).

REGISTER 13-3: SPIxCON2: SPIx CONTROL REGISTER 2

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
FRMEN	SPIFSD	FRMPOL	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	U-0
—	—	—	—	—	—	FRMDLY	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **FRMEN**: Framed SPIx Support bit
1 = Framed SPIx support enabled ($\overline{SS}$x pin used as frame sync pulse input/output)
0 = Framed SPIx support disabled

bit 14 **SPIFSD**: Frame Sync Pulse Direction Control bit
1 = Frame sync pulse input (slave)
0 = Frame sync pulse output (master)

bit 13 **FRMPOL**: Frame Sync Pulse Polarity bit
1 = Frame sync pulse is active-high
0 = Frame sync pulse is active-low

bit 12-2 **Unimplemented:** Read as ‘0’

bit 1 **FRMDLY**: Frame Sync Pulse Edge Select bit
1 = Frame sync pulse coincides with first bit clock
0 = Frame sync pulse precedes first bit clock

bit 0 **Unimplemented:** This bit must not be set to ‘1’ by the user application.

14.2 I²C Module Addresses

The I2CADD register contains the Slave mode addresses. The register is a 10-bit register.

If the A10M bit (I2CCON<10>) is '0', the address is interpreted by the module as a 7-bit address. When an address is received, it is compared to the 7 Least Significant bits of the I2CADD register.

If the A10M bit is '1', the address is assumed to be a 10-bit address. When an address is received, it will be compared with the binary value '1 1 1 1 0 A9 A8' (where A9, A8 are two Most Significant bits of I2CADD). If that value matches, the next address will be compared with the Least Significant 8 bits of I2CADD, as specified in the 10-bit addressing protocol.

14.3 I²C 7-bit Slave Mode Operation

Once enabled (I2CEN = 1), the slave module will wait for a Start bit to occur (i.e., the I²C module is 'Idle'). Following the detection of a Start bit, 8 bits are shifted into I2CRSR and the address is compared against I2CADD. In 7-bit mode (A10M = 0), bits I2CADD<6:0> are compared against I2CRSR<7:1> and I2CRSR<0> is the R_W bit. All incoming bits are sampled on the rising edge of SCL.

If an address match occurs, an acknowledgement will be sent, and the slave event interrupt flag (SI2CIF) is set on the falling edge of the ninth (ACK) bit. The address match does not affect the contents of the I2CRCV buffer or the RBF bit.

14.3.1 SLAVE TRANSMISSION

If the R_W bit received is a '1', then the serial port will go into Transmit mode. It will send ACK on the ninth bit and then hold SCL to '0' until the CPU responds by writing to I2CTRN. SCL is released by setting the SCLREL bit, and 8 bits of data are shifted out. Data bits are shifted out on the falling edge of SCL, such that SDA is valid during SCL high (see timing diagram). The interrupt pulse is sent on the falling edge of the ninth clock pulse, regardless of the status of the ACK received from the master.

14.3.2 SLAVE RECEPTION

If the R_W bit received is a '0' during an address match, then Receive mode is initiated. Incoming bits are sampled on the rising edge of SCL. After 8 bits are received, if I2CRCV is not full or I2COV is not set, I2CRSR is transferred to I2CRCV. ACK is sent on the ninth clock.

If the RBF flag is set, indicating that I2CRCV is still holding data from a previous operation (RBF = 1), then ACK is not sent; however, the interrupt pulse is generated. In the case of an overflow, the contents of the I2CRSR are not loaded into the I2CRCV.

Note:	The I2CRCV will be loaded if the I2COV bit = 1 and the RBF flag = 0. In this case, a read of the I2CRCV was performed, but the user did not clear the state of the I2COV bit before the next receive occurred. The acknowledgement is not sent (ACK = 1) and the I2CRCV is updated.

14.4 I²C 10-bit Slave Mode Operation

In 10-bit mode, the basic receive and transmit operations are the same as in the 7-bit mode. However, the criteria for address match is more complex.

The I²C specification dictates that a slave must be addressed for a write operation, with two address bytes following a Start bit.

The A10M bit is a control bit that signifies that the address in I2CADD is a 10-bit address rather than a 7-bit address. The address detection protocol for the first byte of a message address is identical for 7-bit and 10-bit messages, but the bits being compared are different.

I2CADD holds the entire 10-bit address. Upon receiving an address following a Start bit, I2CRSR <7:3> is compared against a literal '11110' (the default 10-bit address) and I2CRSR<2:1> are compared against I2CADD<9:8>. If a match occurs and if R_W = 0, the interrupt pulse is sent. The ADD10 bit will be cleared to indicate a partial address match. If a match fails or R_W = 1, the ADD10 bit is cleared and the module returns to the Idle state.

The low byte of the address is then received and compared with I2CADD<7:0>. If an address match occurs, the interrupt pulse is generated and the ADD10 bit is set, indicating a complete 10-bit address match. If an address match did not occur, the ADD10 bit is cleared and the module returns to the Idle state.

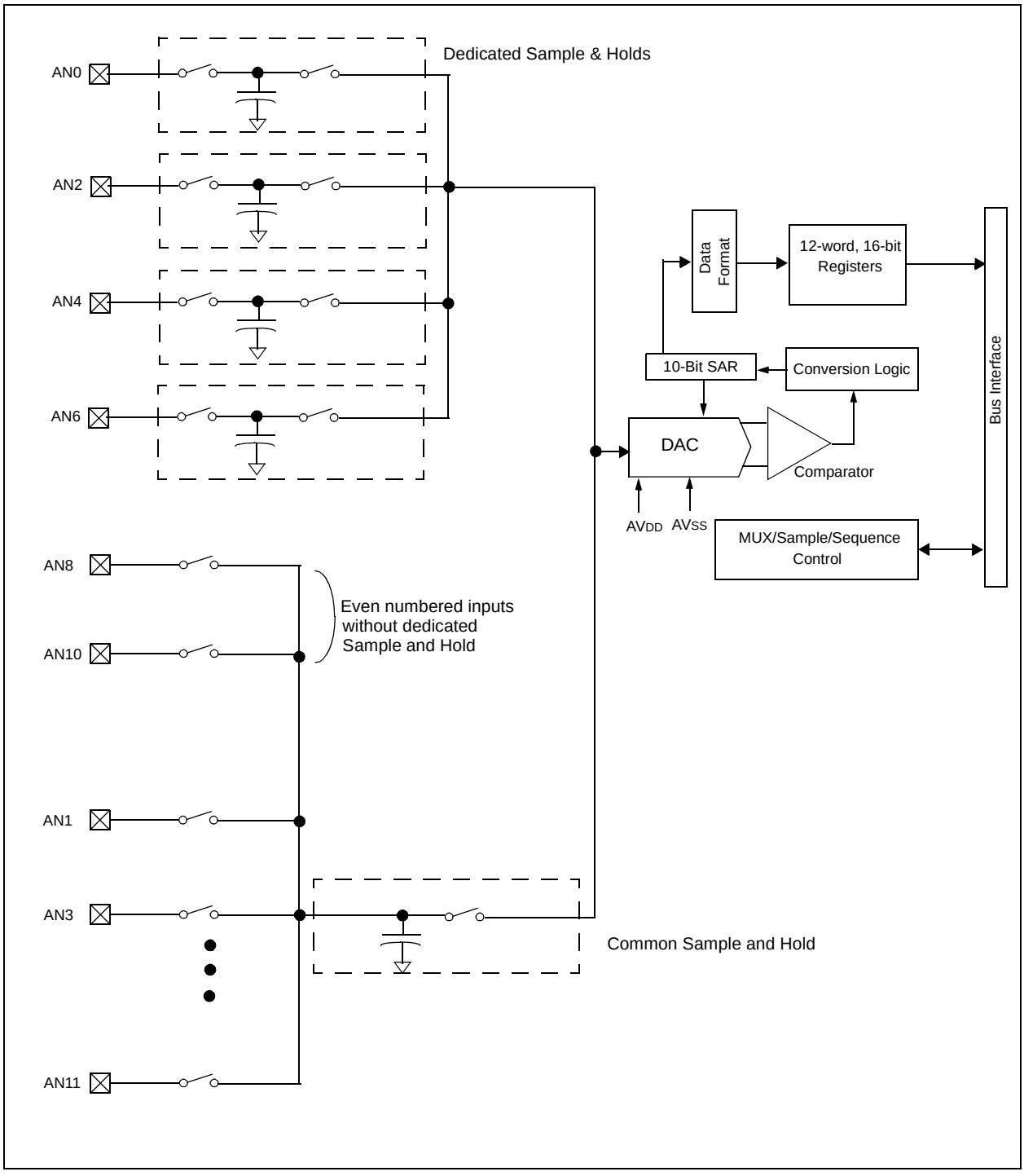
14.4.1 10-BIT MODE SLAVE TRANSMISSION

Once a slave is addressed in this fashion, with the full 10-bit address (we will refer to this state as "PRIOR_ADDR_MATCH"), the master can begin sending data bytes for a slave reception operation.

14.4.2 10-BIT MODE SLAVE RECEPTION

Once addressed, the master can generate a Repeated Start, reset the high byte of the address and set the R_W bit without generating a Stop bit, thus initiating a slave transmit operation.

FIGURE 16-1: ADC BLOCK DIAGRAM



REGISTER 16-3: A/D BASE REGISTER (ADBASE)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADBASE<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
ADBASE<7:1>							—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-1 **ADC Base Register:** This register contains the base address of the user's ADC Interrupt Service Routine jump table. This register, when read, contains the sum of the ADBASE register contents and the encoded value of the PxRDY Status bits.

The encoder logic provides the bit number of the highest priority PxRDY bits where P0RDY is the highest priority, and P5RDY is lowest priority.

Note: The encoding results are shifted left two bits so bits 1-0 of the result are always zero.

bit 0 **Unimplemented:** Read as '0'

Note: As an alternative to using the ADBASE Register, the ADCP0-5 ADC Pair Conversion Complete Interrupts (Interrupts 37-42) can be used to invoke A to D conversion completion routines for individual ADC input pairs. Refer to **Section 16.9 "Individual Pair Interrupts"**.

REGISTER 16-4: A/D PORT CONFIGURATION REGISTER (ADPCFG)

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	PCFG11	PCFG10	PCFG9	PCFG8
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PCFG7	PCFG6	PCFG5	PCFG4	PCFG3	PCFG2	PCFG1	PCFG0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **Unimplemented:** Read as '0'

bit 11-0 **PCFG<11:0>:** A/D Port Configuration Control bits

1 = Port pin in Digital mode, port read input enabled, A/D input multiplexor connected to AVSS

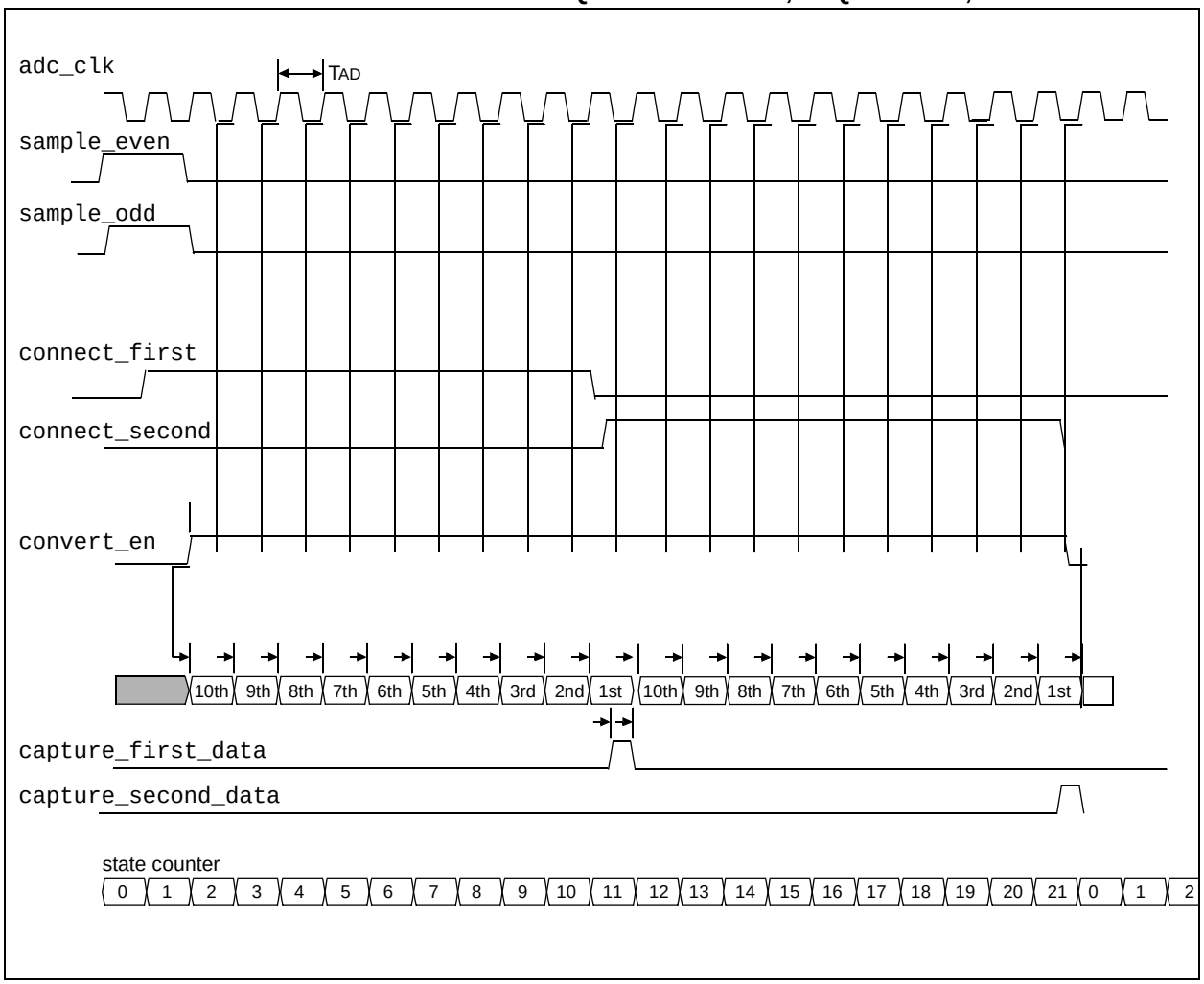
0 = Port pin in Analog mode, port read input disabled, A/D samples pin voltage

16.17 A/D Sample and Convert Timing

The sample and hold circuits assigned to the input pins have their own timing logic that is triggered when an external sample and convert request (from PWM or TMR) is made. The sample and hold circuits have a fixed two clock data sample period. When the sample has been acquired, then the ADC control logic is notified of a pending request, then the conversion is performed as the conversion resources become available.

The ADC module always converts pairs of analog input channels, so a typical conversion process requires 24 clock cycles.

FIGURE 16-3: DETAILED CONVERSION SEQUENCE TIMINGS, SEQSAMP = 0, NOT BUSY



REGISTER 18-2: OSCTUN: OSCILLATOR TUNING REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TSEQ3<3:0>				TSEQ2<3:0>			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TSEQ1<3:0>				TUN<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-12 **TSEQ3<3:0>:** Tune Sequence Value #3 bits
When PWM ROLL<2:0> = 011, this field is used to tune the FRC instead of TUN<3:0>

bit 11-8 **TSEQ2<3:0>:** Tune Sequence Value #2 bits
When PWM ROLL<2:0> = 010, this field is used to tune the FRC instead of TUN<3:0>

bit 7-4 **TSEQ1<3:0>:** Tune Sequence Value #1 bits
When PWM ROLL<2:0> = 001, this field is used to tune the FRC instead of TUN<3:0>

bit 3-0 **TUN<3:0>:** Specifies the user tuning capability for the internal fast RC oscillator . If the TSEQEN bit in the OSCCON register is set, this field, along with bits TSEQ1-TSEQ7, will sequentially tune the FRC oscillator.

0111 = Maximum frequency
0110 =
0101 =
0100 =
0011 =
0010 =
0001 =
0000 = Center frequency, oscillator is running at calibrated frequency
1111 =
1110 =
1101 =
1100 =
1011 =
1010 =
1001 =
1000 = Minimum frequency

TABLE 18-7: FWDT AND FPOR BIT DESCRIPTIONS FOR dsPIC30F1010/202X

Bit Field	Register	Description
FWDTEN	FWDT	Watchdog Timer Enable bit 1 = Watchdog Timer always enabled. (LPRC oscillator cannot be disabled. Clearing the SWDTEN bit in the RCON register will have no effect.) 0 = Watchdog Timer enabled/disabled by user software (LPRC can be disabled by clearing the SWDTEN bit in the RCON register)
WWDTEN	FWDT	Watchdog Timer Window Enable bit 1 = Watchdog Timer in Non-Window mode 0 = Watchdog Timer in Window mode
WDTPRE	FWDT	Watchdog Timer Prescaler bit 1 = 1:128 0 = 1:32
WDTPOST<3:0>	FWDT	Watchdog Timer Postscaler bits 1111 = 1:32, 768 1110 = 1:16, 384 . . . 0001 = 1:2 0000 = 1:1
FPWRT<2:0>	FPOR	Power-on Reset Timer Value Select bits 111 = PWRT = 128 ms 110 = PWRT = 64 ms 101 = PWRT = 32 ms 100 = PWRT = 16 ms 011 = PWRT = 8 ms 010 = PWRT = 4 ms 001 = PWRT = 2 ms 000 = PWRT = Disabled

18.11 In-Circuit Debugger

When MPLAB® ICD 2 is selected as a debugger, the in-circuit debugging functionality is enabled. This function allows simple debugging functions when used with MPLAB IDE. When the device has this feature enabled, some of the resources are not available for general use. These resources include the first 80 bytes of data RAM and two I/O pins.

One of four pairs of Debug I/O pins may be selected by the user using configuration options in MPLAB IDE. These pin pairs are named EMUD/EMUC, EMUD1/EMUC1 and EMUD2/EMUC2.

In each case, the selected EMUD pin is the Emulation/Debug Data line, and the EMUC pin is the Emulation/Debug Clock line. These pins will interface to the MPLAB ICD 2 module available from Microchip. The selected pair of Debug I/O pins is used by MPLAB ICD 2 to send commands and receive responses, as well as to send and receive data. To use the in-circuit debugging function of the device, the design must implement ICSP connections to $\overline{MCLR}$, VDD, VSS, PGC, PGD and the selected EMUDx/EMUCx pin pair.

This gives rise to two possibilities:

1. If EMUD/EMUC is selected as the debug I/O pin pair, then only a 5-pin interface is required, as the EMUD and EMUC pin functions are multiplexed with the PGD and PGC pin functions in all dsPIC30F devices.
2. If EMUD1/EMUC1 or EMUD2/EMUC2 is selected as the debug I/O pin pair, then a 7-pin interface is required, as the EMUDx/EMUCx pin functions (x = 1 or 2) are not multiplexed with the PGD and PGC pin functions.

TABLE 21-2: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min	Typ	Max	Unit
dsPIC30F1010/202X-30I					
Operating Junction Temperature Range	T_J	-40	—	+125	°C
Operating Ambient Temperature Range	T_A	-40	—	+85	°C
dsPIC30F1010/202X-20E					
Operating Junction Temperature Range	T_J	-40	—	+150	°C
Operating Ambient Temperature Range	T_A	-40	—	+125	°C
Power Dissipation: Internal Chip Power Dissipation: $P_{INT} = V_{DD} \times (I_{DD} - \sum I_{OH})$ I/O Pin Power Dissipation: $P_{I/O} = \sum (\{V_{DD} - V_{OH}\} \times I_{OH}) + \sum (V_{OL} \times I_{OL})$	P_D	$P_{INT} + P_{I/O}$			W
Maximum Allowed Power Dissipation	P_{DMAX}	$(T_J - T_A)/\theta_{JA}$			W

TABLE 21-3: THERMAL PACKAGING CHARACTERISTICS

Characteristic	Symbol	Typ	Max	Unit	Notes
Package Thermal Resistance, 28-pin SOIC (SO)	θ_{JA}	48.3	—	°C/W	**1, 2**
Package Thermal Resistance, 28-pin QFN	θ_{JA}	33.7	—	°C/W	**1, 2**
Package Thermal Resistance, 28-pin SPDIP (SP)	θ_{JA}	42	—	°C/W	**1, 2**
Package Thermal Resistance, 44-pin QFN	θ_{JA}	28	—	°C/W	**1, 2**
Package Thermal Resistance, 44-pin TQFP	θ_{JA}	39.3	—	°C/W	**1, 2**

Note 1: Junction to ambient thermal resistance, Theta-ja (θ_{JA}) numbers are achieved by package simulations.

2: Depending on operating conditions, air flow may be required for improved thermal performance.

TABLE 21-4: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS

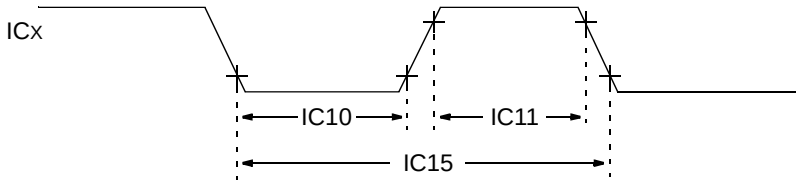
DC CHARACTERISTICS			**Standard Operating Conditions: 3.3V and 5.0V (±10%) (unless otherwise stated)** Operating temperature -40°C ≤ T_A ≤ +85°C for Industrial -40°C ≤ T_A ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Operating Voltage(2)							
DC10	V_{DD}	**Supply Voltage**	3.0	—	5.5	V	Industrial temperature
DC11	V_{DD}	**Supply Voltage**	3.0	—	5.5	V	Extended temperature
DC12	V_{DR}	**RAM Data Retention Voltage(3)**	—	1.5	—	V	
DC16	V_{POR}	**V_{DD} Start Voltage** to Ensure Internal Power-on Reset signal	—	V_{SS}	—	V	
DC17	S_{VDD}	**V_{DD} Rise Rate** to Ensure Internal Power-on Reset signal	0.05	—	—	V/ms	0-5V in 0.1 sec, 0-3.3V in 60 ms

Note 1: Data in "Typ" column is at 5V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: These parameters are characterized but not tested in manufacturing.

3: This is the limit to which V_{DD} can be lowered without losing RAM data.

FIGURE 21-7: INPUT CAPTURE x (ICx) TIMING CHARACTERISTICS



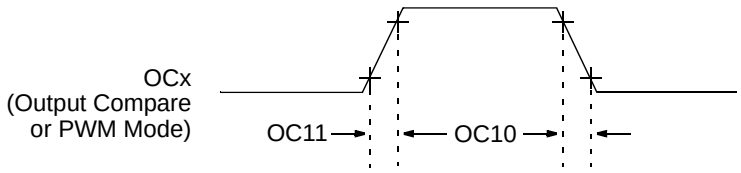
Note: Refer to Figure 21-1 for load conditions.

TABLE 21-23: INPUT CAPTURE x TIMING REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions: 3.3V and 5.0V (±10%) (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Param No.	**Symbol**	**Characteristic(1)**		**Min**	**Max**	**Units**	**Conditions**
IC10	TccL	ICx Input Low Time	No Prescaler	0.5 TCY + 20	—	ns	
			With Prescaler	10	—	ns	
IC11	TccH	ICx Input High Time	No Prescaler	0.5 TCY + 20	—	ns	
			With Prescaler	10	—	ns	
IC15	TccP	ICx Input Period		(2 TCY + 40)/N	—	ns	N = Prescale value (1, 4, 16)

Note 1: These parameters are characterized but not tested in manufacturing.

FIGURE 21-8: OUTPUT COMPARE x (OCx) MODULE TIMING CHARACTERISTICS



Note: Refer to Figure 21-1 for load conditions.

TABLE 21-24: OUTPUT COMPARE x MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.3V and 5.0V (±10%) (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic(1)**	**Min**	**Typ(2)**	**Max**	**Units**	**Conditions**
OC10	TccF	OCx Output Fall Time	—	—	—	ns	See Parameter D032
OC11	TccR	OCx Output Rise Time	—	—	—	ns	See Parameter D031

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ" column is at 5V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

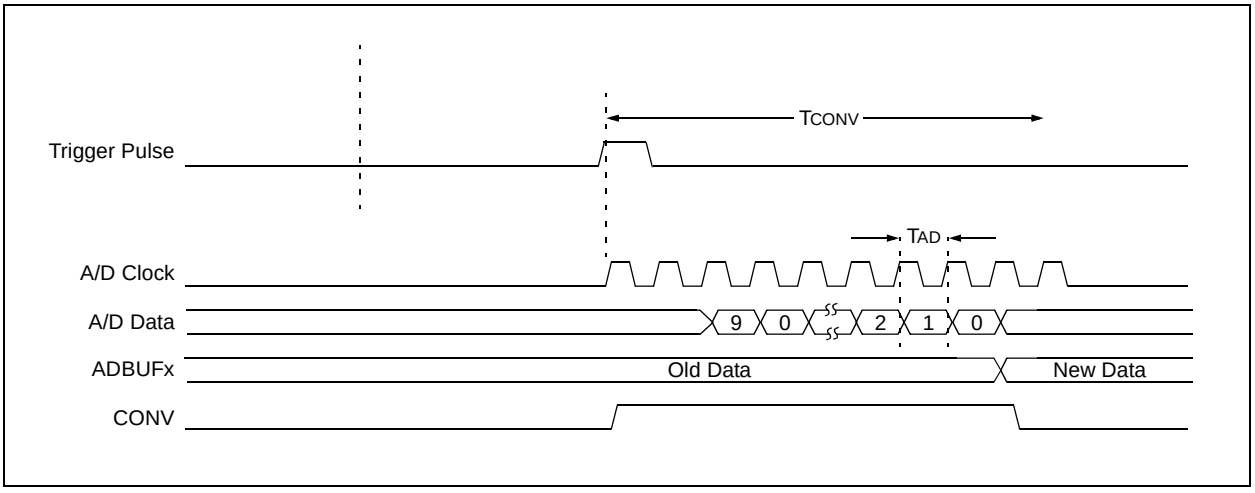
TABLE 21-33: 10-BIT HIGH-SPEED A/D MODULE SPECIFICATIONS (CONTINUED)

AC CHARACTERISTICS			Standard Operating Conditions: 3.3V and 5.0V (±10%) (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ**	**Max.**	**Units**	**Conditions**
AD24	EOFF	Offset Error	—	±0.75	<±2.0	LSb	VINL = AVSS = VSS = 0V, AVDD = VDD = 5V
AD24A	EOFF	Offset Error	—	±0.75	<±2.0	LSb	VINL = AVSS = VSS = 0V, AVDD = VDD = 3.3V
AD25	—	Monotonicity(2)	—	—	—	—	Guaranteed
Dynamic Performance							
AD30	THD	Total Harmonic Distortion	-77	-73	-68	dB	
AD31	SINAD	Signal to Noise and Distortion	—	58	—	dB	
AD32	SFDR	Spurious Free Dynamic Range	—	-73	—	dB	
AD33	FNYQ	Input Signal Bandwidth	—	—	0.5	MHz	
AD34	ENOB	Effective Number of Bits	—	9.4	—	bits	

Note 1: Because the sample caps will eventually lose charge, clock rates below 10 kHz can affect linearity performance, especially at elevated temperatures.

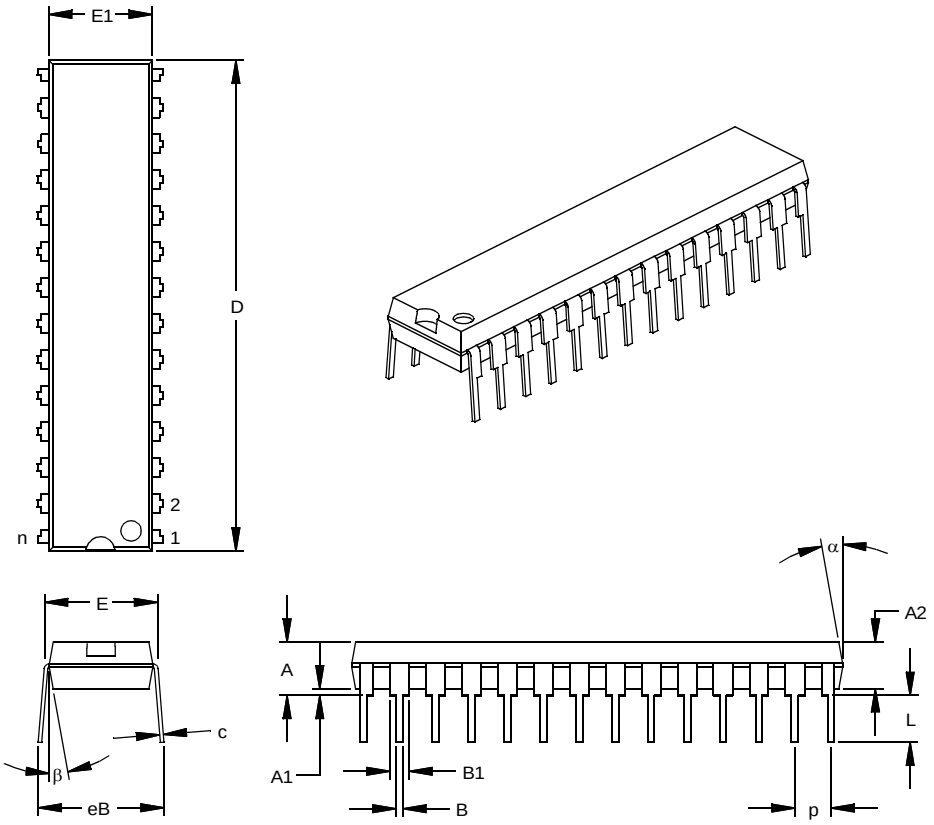
2: The A/D conversion result never decreases with an increase in the input voltage, and has no missing codes.

FIGURE 21-20: A/D CONVERSION TIMING PER INPUT



28-Lead Skinny Plastic Dual In-line (SP) – 300 mil Body (PDIP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

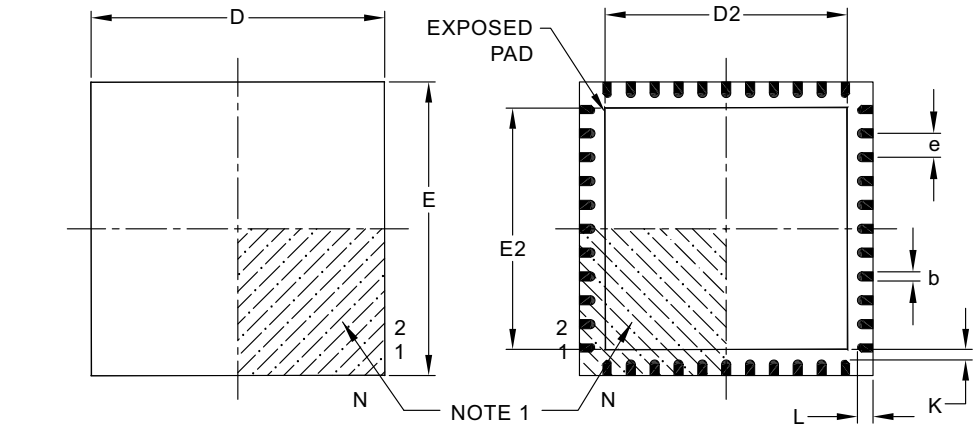


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		28			28	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.150	.160	3.56	3.81	4.06
Molded Package Thickness	A2	.125	.130	.135	3.18	3.30	3.43
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.310	.325	7.62	7.87	8.26
Molded Package Width	E1	.275	.285	.295	6.99	7.24	7.49
Overall Length	D	1.345	1.365	1.385	34.16	34.67	35.18
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.040	.053	.065	1.02	1.33	1.65
Lower Lead Width	B	.016	.019	.022	0.41	0.48	0.56
Overall Row Spacing §	eB	.320	.350	.430	8.13	8.89	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

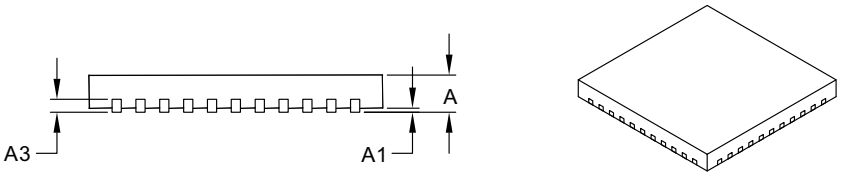
***** Controlling Parameter
§ Significant Characteristic
Notes:
Dimension D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MO-095
Drawing No. C04-070

44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body (QFN)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW **BOTTOM VIEW**



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		44	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		8.00 BSC	
Exposed Pad Width	E2	6.30	6.45	6.80
Overall Length	D		8.00 BSC	
Exposed Pad Length	D2	6.30	6.45	6.80
Contact Width	b	0.25	0.30	0.38
Contact Length §	L	0.30	0.40	0.50
Contact-to-Exposed Pad §	K	0.20	—	—

Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

□ □ □ □ Microchip Technology Drawing No. C04–103, Sept. 8, 2006

NOTES: