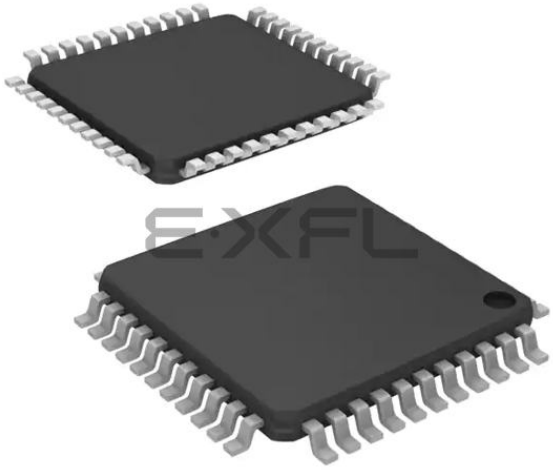

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Product Status	Active
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Core Size	16-Bit
Speed	20 MIPS
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	35
Program Memory Size	12KB (4K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic30f2023-20e-pt

Analog Features:

ADC

- 10-bit resolution
- 2000 Ksps conversion rate
- Up to 12 input channels
- “Conversion pairing” allows simultaneous conversion of two inputs (i.e., current and voltage) with a single trigger
- PWM control loop:
  - Up to six conversion pairs available
  - Each conversion pair has up to four PWM and seven other selectable trigger sources
- Interrupt hardware supports up to 1M interrupts per second

COMPARATOR

- Four Analog Comparators:
  - 20 ns response time
  - 10-bit DAC reference generator
  - Programmable output polarity
  - Selectable input source
  - ADC sample and convert capable
- PWM module interface
  - PWM Duty Cycle Control
  - PWM Period Control
  - PWM Fault Detect
- Special Event Trigger
- PWM-generated ADC Trigger

Special Microcontroller Features:

- Enhanced Flash program memory:
  - 10,000 erase/write cycle (min.) for industrial temperature range, 100k (typical)
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- Detects clock failure and switches to on-chip low power RC oscillator
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  - Sleep, Idle and Alternate Clock modes

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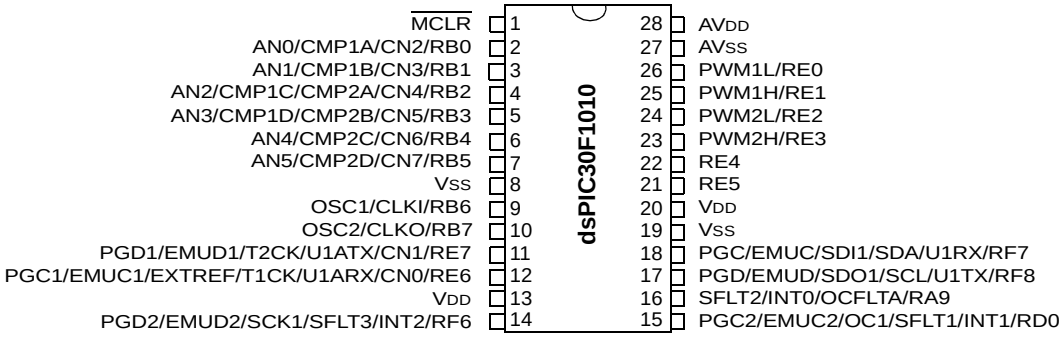
dsPIC30F SWITCH MODE POWER SUPPLY FAMILY

Product	Pins	Packaging	Program Memory (Bytes)	Data SRAM (Bytes)	Timers	Capture	Compare	UART	SPI	I^2C™	PWM	ADCs	S & H	A/D Inputs	Analog Comparators	GPIO
dsPIC30F1010	28	SDIP	6K	256	2	0	1	1	1	1	2x2	1	3	6 ch	2	21
dsPIC30F1010	28	SOIC	6K	256	2	0	1	1	1	1	2x2	1	3	6 ch	2	21
dsPIC30F1010	28	QFN-S	6K	256	2	0	1	1	1	1	2x2	1	3	6 ch	2	21
dsPIC30F2020	28	SDIP	12K	512	3	1	2	1	1	1	4x2	1	5	8 ch	4	21
dsPIC30F2020	28	SOIC	12K	512	3	1	2	1	1	1	4x2	1	5	8 ch	4	21
dsPIC30F2020	28	QFN-S	12K	512	3	1	2	1	1	1	4x2	1	5	8 ch	4	21
dsPIC30F2023	44	QFN	12K	512	3	1	2	1	1	1	4x2	1	5	12 ch	4	35
dsPIC30F2023	44	TQFP	12K	512	3	1	2	1	1	1	4x2	1	5	12 ch	4	35

Pin Diagrams

28-Pin SDIP and SOIC



28-Pin QFN-S

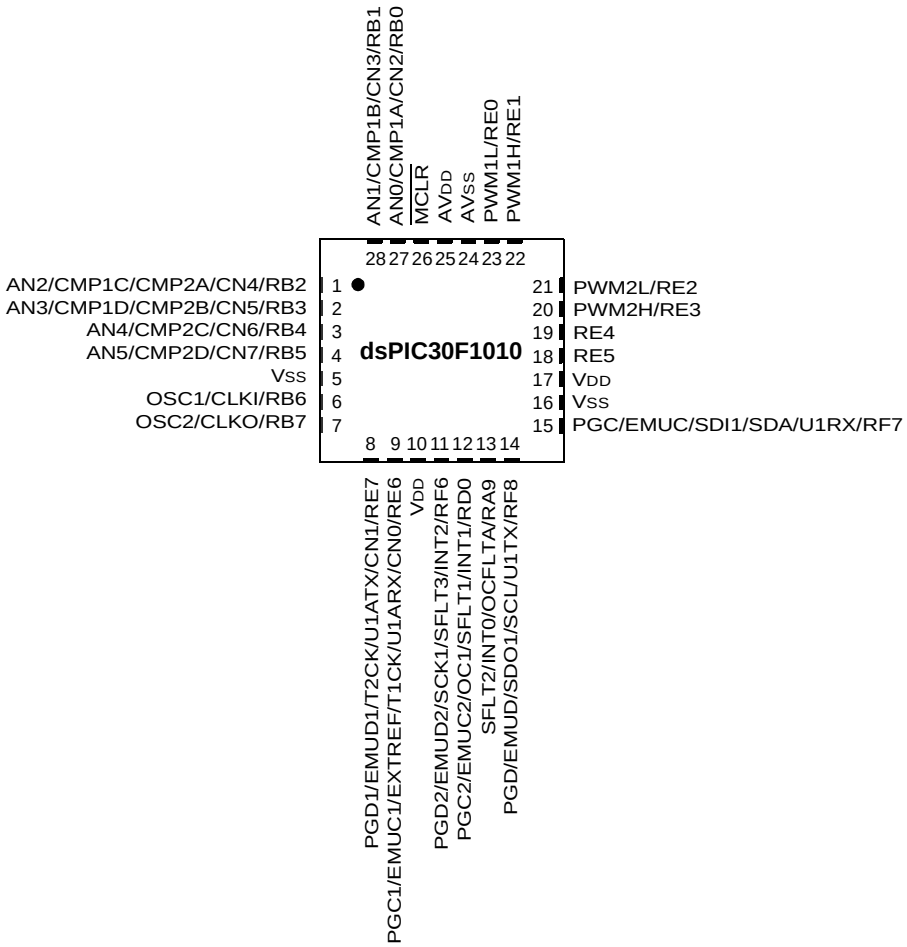


TABLE 4-2: BIT-REVERSED ADDRESS SEQUENCE (16-ENTRY)

Normal Address					Bit-Reversed Address				
A3	A2	A1	A0	Decimal	A3	A2	A1	A0	Decimal
0	0	0	0	0	0	0	0	0	0
0	0	0	1	1	1	0	0	0	8
0	0	1	0	2	0	1	0	0	4
0	0	1	1	3	1	1	0	0	12
0	1	0	0	4	0	0	1	0	2
0	1	0	1	5	1	0	1	0	10
0	1	1	0	6	0	1	1	0	6
0	1	1	1	7	1	1	1	0	14
1	0	0	0	8	0	0	0	1	1
1	0	0	1	9	1	0	0	1	9
1	0	1	0	10	0	1	0	1	5
1	0	1	1	11	1	1	0	1	13
1	1	0	0	12	0	0	1	1	3
1	1	0	1	13	1	0	1	1	11
1	1	1	0	14	0	1	1	1	7
1	1	1	1	15	1	1	1	1	15

TABLE 4-3: BIT-REVERSED ADDRESS MODIFIER VALUES FOR XBREV REGISTER

Buffer Size (Words)	XB<14:0> Bit-Reversed Address Modifier Value(1)
32768	0x4000
16384	0x2000
8192	0x1000
4096	0x0800
2048	0x0400
1024	0x0200
512	0x0100
256	0x0080
128	0x0040
64	0x0020
32	0x0010
16	0x0008
8	0x0004
4	0x0002
2	0x0001

Note 1: Modifier values greater than 256 words exceed the data memory available on the dsPIC30F1010/202X device

REGISTER 5-4: IFS1: INTERRUPT FLAG STATUS REGISTER 1

R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0	U-0	U-0
AC3IF	AC2IF	AC1IF	—	CNIF	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	PWM4IF	PWM3IF	PWM2IF	PWM1IF	PSEMIF	INT2IF	INT1IF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **AC3IF:** Analog Comparator #3 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 14 **AC2IF:** Analog Comparator #2 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 13 **AC1IF:** Analog Comparator #1 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 12 **Unimplemented:** Read as '0'

bit 11 **CNIF:** Input Change Notification Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 10-7 **Unimplemented:** Read as '0'

bit 6 **PWM4IF:** Pulse Width Modulation Generator #4 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 5 **PWM3IF:** Pulse Width Modulation Generator #3 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 4 **PWM2IF:** Pulse Width Modulation Generator #2 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 3 **PWM1IF:** Pulse Width Modulation Generator #1 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 2 **PSEMIF:** PWM Special Event Match Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 1 **INT2IF:** External Interrupt 2 Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 0 **INT1IF:** External Interrupt 1 Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

TABLE 6-2: dsPIC30F2023 PORT REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
TRISA	02C0	—	—	—	—	TRISA11	TRISA10	TRIS9	TRISA8	—	—	—	—	—	—	—	—	0000 1111 0000 0000
PORTA	02C2	—	—	—	—	RA11	RA10	RA9	RA8	—	—	—	—	—	—	—	—	0000 0000 0000 0000
LATA	02C4	—	—	—	—	LATA11	LATA10	LATA9	LATA8	—	—	—	—	—	—	—	—	0000 0000 0000 0000
TRISB	02C6	—	—	—	—	TRISB11	TRISB10	TRISB9	TRISB8	TRISB7	TRIS6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	0000 1111 1111 1111
PORTB	02C8	—	—	—	—	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	0000 0000 0000 0000
LATB	02CA	—	—	—	—	LATB11	LATB10	LATB9	LATB8	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	0000 0000 0000 0000
TRISD	02D2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRISD1	TRISD0	0000 0000 0000 0011
PORTD	02D4	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RD1	RD0	0000 0000 0000 0000
LATD	02D6	—	—	—	—	—	—	—	—	—	—	—	—	—	—	LATD1	LATD0	0000 0000 0000 0000
TRISE	02D8	—	—	—	—	—	—	—	—	TRSE7	TRSE6	TRISE5	TRISE4	TRISE3	TRISE2	TRISE1	TRISE0	0000 0000 1111 1111
PORTE	02DA	—	—	—	—	—	—	—	—	RE7	RE6	RE5	RE4	RE3	RE2	RE1	RE0	0000 0000 0000 0000
LATE	02DC	—	—	—	—	—	—	—	—	LATE7	LATE6	LATE5	LATE4	LATE3	LATE2	LATE1	LATE0	0000 0000 0000 0000
TRISF	02DE	TRISF15	TRISF14	—	—	—	—	—	TRISF8	TRISF7	TRISF6	—	—	TRISF3	TRISF2	—	—	1100 0001 1100 1100
PORTF	02E0	RF15	RF14	—	—	—	—	—	RF8	RF7	RF6	—	—	RF3	RF2	—	—	0000 0000 0000 0000
LATF	02E2	LATF15	LATF14	—	—	—	—	—	LATF8	LATF7	LATF6	—	—	LATF3	LATF2	—	—	0000 0000 0000 0000
TRISG	02E4	—	—	—	—	—	—	—	—	—	—	—	—	TRISG3	TRISG2	—	—	0000 0000 0000 1100
PORTG	02E6	—	—	—	—	—	—	—	—	—	—	—	—	RG3	RG2	—	—	0000 0000 0000 0000
LATG	02E8	—	—	—	—	—	—	—	—	—	—	—	—	LATG3	LATG2	—	—	0000 0000 0000 0000

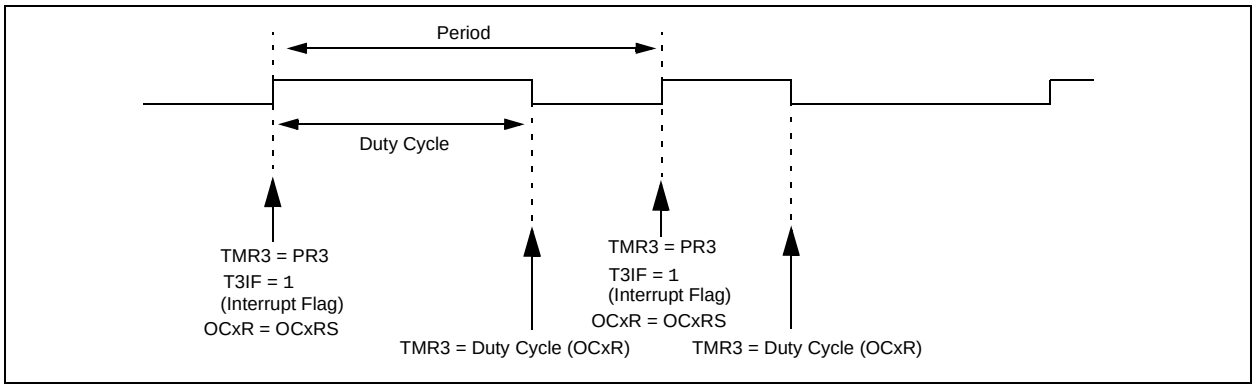
Note: Refer to the "*dsPIC30F Family Reference Manual*" (DS70046) for descriptions of register bit fields.

TABLE 6-3: dsPIC30F1010/202X INPUT CHANGE NOTIFICATION REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
CNEN1	0060	—	—	—	—	—	—	—	—	CN7IE	CN6IE	CN5IE	CN4IE	CN3IE	CN2IE	CN1IE	CN0IE	0000 0000 0000 0000
CNPU1	0064	—	—	—	—	—	—	—	—	CN7PUE	CN6PUE	CN5PUE	CN4PUE	CN3PUE	CN2PUE	CN1PUE	CN0PUE	0000 0000 0000 0000

Note: Refer to the "*dsPIC30F Family Reference Manual*" (DS70046) for descriptions of register bit fields.

FIGURE 11-1: PWM OUTPUT TIMING



11.7 Output Compare Interrupts

The output compare channels have the ability to generate an interrupt on a compare match, for whichever Match mode has been selected.

For all modes except the PWM mode, when a compare event occurs, the respective interrupt flag (OCxIF) is asserted and an interrupt will be generated, if enabled. The OCxIF bit is located in the corresponding IFS STATUS register, and must be cleared in software. The interrupt is enabled via the respective compare interrupt enable (OCxIE) bit, located in the corresponding IEC Control register.

For the PWM mode, when an event occurs, the respective timer interrupt flag (T2IF or T3IF) is asserted and an interrupt will be generated, if enabled. The IF bit is located in the IFS0 STATUS register, and must be cleared in software. The interrupt is enabled via the respective timer interrupt enable bit (T2IE or T3IE), located in the IEC0 Control register. The output compare interrupt flag is never set during the PWM mode of operation.

12.14 Dead-Time Generation

Dead time refers to a programmable period of time, specified by the Dead-Time Register (DTR) or the ALT-DTR register, which prevent a PWM output from being asserted until its complementary PWM signal has been deasserted for the specified time. Figure 12-15 shows the insertion of dead time in a complementary pair of PWM outputs. Figure 12-16 shows the four dead-time units that each have their own dead-time value.

Dead-time generation can be provided when any of the PWM I/O pin pairs are operating in any output mode.

Many power-converter circuits require dead time because the power transistors cannot switch instantaneously. To prevent current “shoot-through” some amount of time must be provided between the turn-off event of one PWM output in a complementary pair and the turn-on event of the other transistor.

The PWM module can also provide negative dead time. Negative dead time is the forced overlap of the PWMH and PWML signals. There are certain converter techniques that require a limited amount of
current “shoot-through”.

The dead-time feature can be disabled for each PWM generator. The dead-time functionality is controlled by the DTC<1:0> bits in the PWMCON register.

Note:	If zero dead time is required, the dead time feature must be explicitly disabled in the DTC<1:0> bit in the PWMCON register

FIGURE 12-15: DEAD-TIME INSERTION FOR COMPLEMENTARY PWM

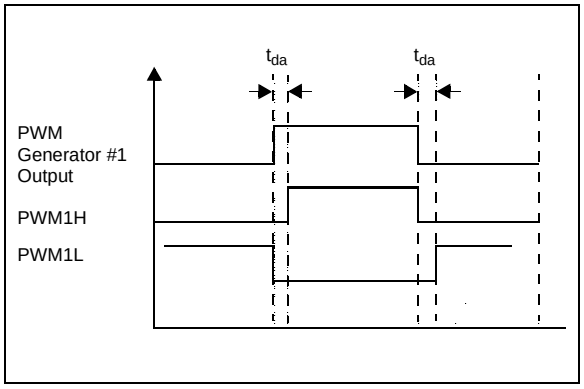
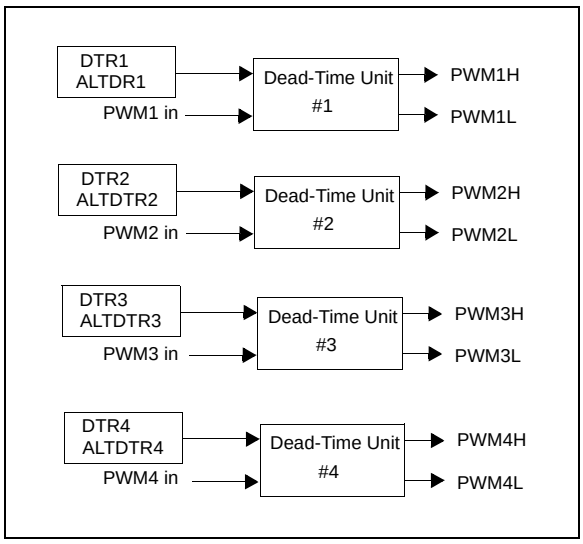


FIGURE 12-16: DEAD-TIME CONTROL UNITS BLOCK DIAGRAM



12.14.1 DEAD-TIME GENERATORS

Each complementary output pair for the PWM module has 12-bit down counters to produce the dead-time insertion. Each dead-time unit has a rising and falling edge detector connected to the duty cycle comparison output.

Depending on whether the edge is rising or falling, one of the transitions on the complementary outputs is delayed until the associated timer counts down to zero. A timing diagram indicating the dead-time insertion for one pair of PWM outputs is shown in Figure 12-15.

12.14.2 ALTERNATE DEAD-TIME SOURCE

The alternate dead time refers to the dead time specified by the ALTDTR register that is applied to the complementary PWM output. Figure 12-17 shows a dual dead-time insertion using the ALTDTR register.

12.24 PWM Current-Limit Pins

Each PWM generator can select its own current-limit input source from up to12 current-limit/Fault pins. In the FCLCONx registers, each PWM generator has control bits (CLSRC<3:0>) that specify the source for its current-limit input signal. Additionally, each PWM generator has a CLIEN bit in the PWMCONx register that enables the generation of current-limit interrupt requests. Each PWM generator has an associated Fault polarity bit CLPOL in the FCLCONx register. Figure 12-21 is a diagram of the PWM Current-Limit control logic.

The current-limit pins actually serve two different purposes. They can be used to implement either Current-Limit PWM mode or Current Reset PWM mode.

1. When the CLIEN bit is set in the PWMCONx registers, the PWMxH,L outputs are forced to the values specified by the CLDAT<1:0> bits in the IOCONx register, if the selected current-limit input signal is asserted.
2. When the CLMOD bit is zero AND the XPRES bit in the PWMCONx register is '01' AND the PWM generator is in Independent Time Base mode (ITB = 1), then a current-limit signal resets the time base for the affected PWM generator. This behavior is called Current Reset mode, which is used in some Power Factor Correction (PFC) applications.

12.24.1 CURRENT-LIMIT INTERRUPTS

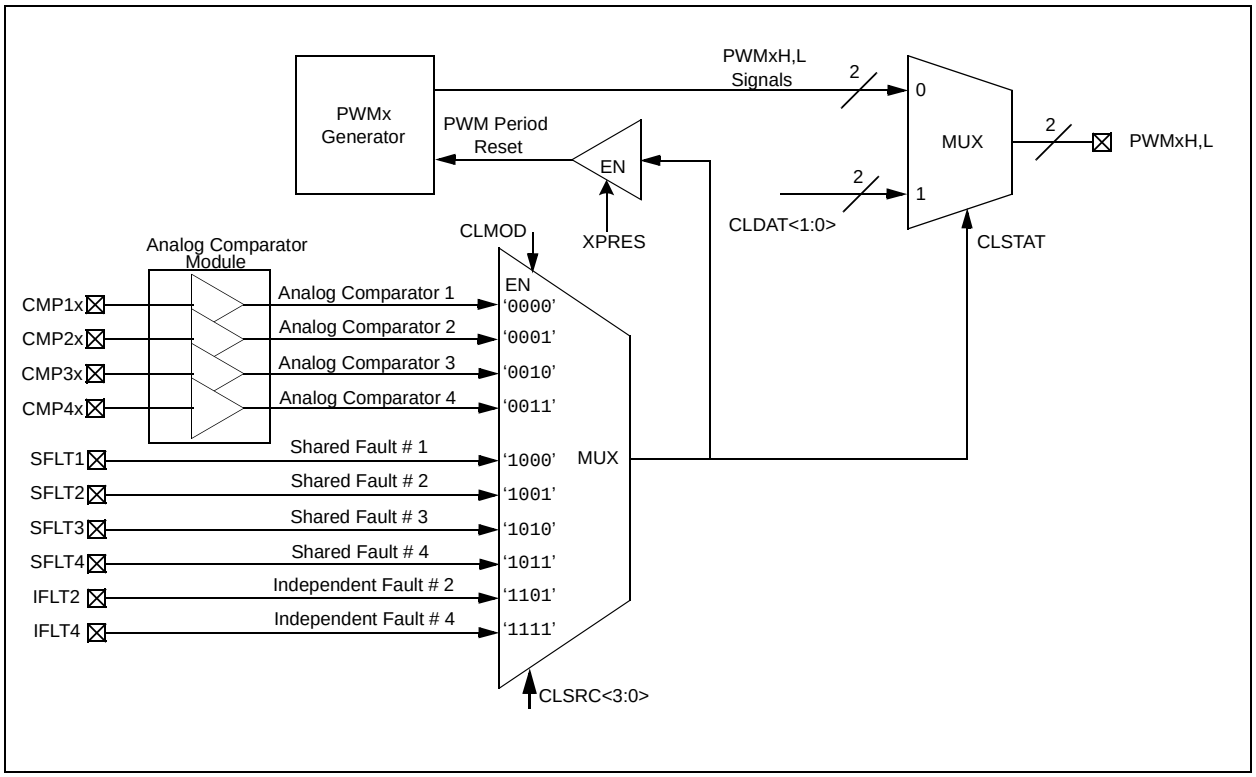
The state of the PWM current-limit conditions is available on the CLSTAT bits in the PWMCONx registers. The CLSTAT bits display the current-limit IRQ flag if the CLIEN bit is set. If current-limit interrupts are not enabled, then the CLSTAT bits display the status of the selected current-limit inputs in positive logic format. When the current-limit input pin associated with a PWM generator is not used, these pins become general purpose I/O or interrupt input pins.

The current-limit pins are normally active high. If set to '1', the CLPOL bit in FCLCONx registers inverts the selected current-limit input signal to active high.

The interrupts generated by the selected current-limit signals are combined to create a single interrupt request signal to the interrupt controller, which has its own interrupt vector, interrupt flag bit, interrupt enable bit and interrupt priority bits associated with it.

The Fault pins are also readable through the PORT I/O logic when the PWM module is enabled. This allows the user to poll the state of the Fault pins in software.

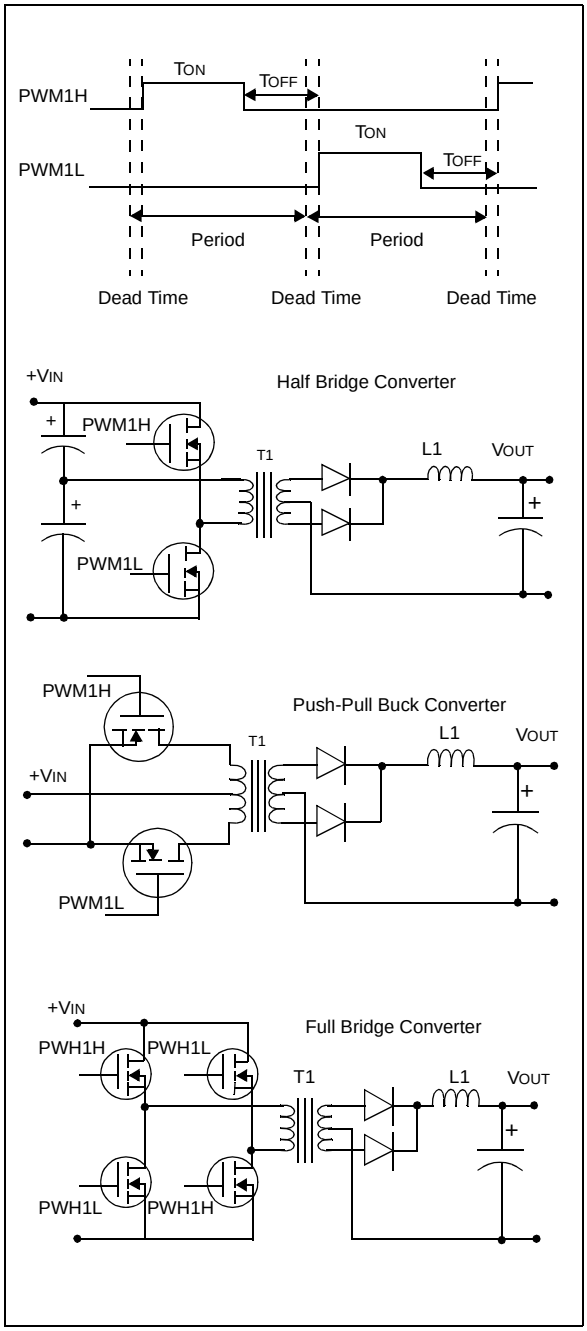
FIGURE 12-21: PWM CURRENT-LIMIT CONTROL LOGIC DIAGRAM



12.34.3 APPLICATION OF PUSH-PULL PWM MODE

Push-Pull PWM mode is typically used in transformer coupled circuits to ensure that no net DC currents flow through the transformer. Push-Pull mode ensures that the same duty cycle PWM pulse is applied to the transformer windings in alternate directions, as shown in Figure 12-24.

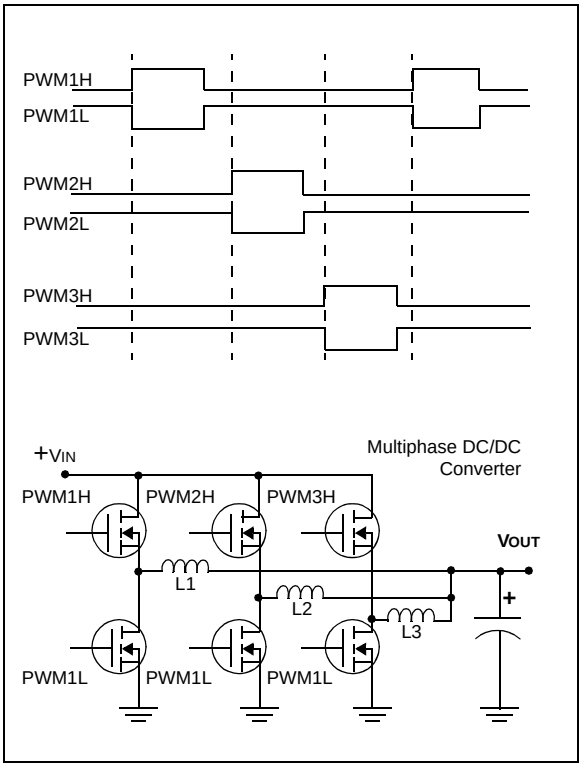
FIGURE 12-24: APPLICATIONS OF PUSH-PULL PWM MODE



12.34.4 APPLICATION OF MULTI-PHASE PWM MODE

Multi-Phase PWM mode is often used in DC/DC converters that must handle very fast load current transients and fit into tight spaces. A multi-phase converter is essentially a parallel array of buck converters that are operated slightly out of phase of each other, as shown in Figure 12-25. The multiple phases create an effective switching speed equal to the sum of the individual converters. If a single phase is operating with a 333 KHz PWM frequency, then the effective switching frequency for the circuit is 1 MHz. This high switching frequency greatly reduces output capacitor size requirements and improves load transient response.

FIGURE 12-25: APPLICATIONS OF MULTI-PHASE PWM MODE



REGISTER 16-6: A/D CONVERT PAIR CONTROL REGISTER 1 (ADCPC1) (CONTINUED)

bit 4-0 **TRGSRC2<4:0>:** Trigger 2 Source Selection bits
Selects trigger source for conversion of analog channels: AN5 and AN4
00000 = No conversion enabled
00001 = Individual software trigger selected
00010 = Global software trigger selected
00011 = PWM Special Event Trigger selected
00100 = PWM generator #1 trigger selected
00101 = PWM generator #2 trigger selected
00110 = PWM generator #3 trigger selected
00111 = PWM generator #4 trigger selected
01100 = Timer #1 period match
01101 = Timer #2 period match
01110 = PWM GEN #1 current-limit ADC trigger
01111 = PWM GEN #2 current-limit ADC trigger
10000 = PWM GEN #3 current-limit ADC trigger
10001 = PWM GEN #4 current-limit ADC trigger
10110 = PWM GEN #1 fault ADC trigger
10111 = PWM GEN #2 fault ADC trigger
11000 = PWM GEN #3 fault ADC trigger
11001 = PWM GEN #4 fault ADC trigger

REGISTER 16-7: A/D CONVERT PAIR CONTROL REGISTER 2 (ADCPC2)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IRQEN5	PEND5	SWTRG5	TRGSRC5<4:0>				
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IRQEN4	PEND4	SWTRG4	TRGSRC4<4:0>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **IRQEN5:** Interrupt Request Enable 5 bit
1 = Enable IRQ generation when requested conversion of channels AN11 and AN10 is completed
0 = IRQ is not generated

bit 14 **PEND5:** Pending Conversion Status 5 bit
1 = Conversion of channels AN11 and AN10 is pending. Set when selected trigger is asserted
0 = Conversion is complete

bit 13 **SWTRG5:** Software Trigger 5 bit
1 = Start conversion of AN11 and AN10 (if selected by TRGSRC bits). If other conversions are in progress, then conversion will be performed when the conversion resources are available. This bit will be reset when the PEND bit is set.

bit 12-8 **TRGSRC5<4:0>:** Trigger Source Selection 5 bits
Selects trigger source for conversion of analog channels A11 and A10.
00000 = No conversion enabled
00001 = Individual software trigger selected
00010 = Global software trigger selected
00011 = PWM Special Event Trigger selected
00100 = PWM generator #1 trigger selected
00101 = PWM generator #2 trigger selected
00110 = PWM generator #3 trigger selected
00111 = PWM generator #4 trigger selected
01100 = Timer #1 period match
01101 = Timer #2 period match
01110 = PWM GEN #1 current-limit ADC trigger
01111 = PWM GEN #2 current-limit ADC trigger
10000 = PWM GEN #3 current-limit ADC trigger
10001 = PWM GEN #4 current-limit ADC trigger
10110 = PWM GEN #1 fault ADC trigger
10111 = PWM GEN #2 fault ADC trigger
11000 = PWM GEN #3 fault ADC trigger
11001 = PWM GEN #4 fault ADC trigger

bit 7 **IRQEN4:** Interrupt Request Enable 4 bit
1 = Enable IRQ generation when requested conversion of channels AN9 and AN8 is completed
0 = IRQ is not generated

bit 6 **PEND4:** Pending Conversion Status 4 bit
1 = Conversion of channels AN9 and AN8 is pending. Set when selected trigger is asserted.
0 = Conversion is complete

bit 5 **SWTRG4:** Software Trigger 4 bit
1 = Start conversion of AN9 and AN8 (if selected by TRGSRC bits). If other conversions are in progress, then conversion will be performed when the conversion resources are available. This bit will be reset when the PEND bit is set.

18.3.1 INITIAL CLOCK SOURCE SELECTION

While coming out of a Power-on Reset, the device selects its clock source based on:

a) FNOSC<1:0> Configuration bits that select one of three oscillator groups (HS, EC or FRC)

b) POSCMD1<1:0> Configuration bits that select the Primary Oscillator Mode

c) OSCIOFNC selects if the OSC2 pin is an I/O or clock output

The selection is as shown in Table 18-1.

TABLE 18-1: CONFIGURATION BIT VALUES FOR CLOCK SELECTION

Oscillator Mode	Oscillator Source	FNOSC<1:0>		POSCMD<1:0>		OSCIOFNC	OSC2 Function	OSC1 Function
		Bit 1	Bit 0	Bit 1	Bit 0			
HS w/PLL 32x	PLL	1	1	1	0	N/A	CLKO(1)	CLKI
FRC w/PLL 32x	PLL	0	1	1	1	1	CLKO	I/O
FRC w/PLL 32x	PLL	0	1	1	1	0	I/O	I/O
EC w/PLL 32x	PLL	1	1	0	0	1	CLKO	CLKI
EC w/PLL 32x	PLL	1	1	0	0	0	I/O	CLKI
EC(2)	External	1	0	0	0	1	CLKO	CLKI
EC(2)	External	1	0	0	0	0	I/O	CLKI
HS(2)	External	1	0	1	0	N/A	CLKO(1)	CLKI
FRC(2)	Internal RC	0	0	1	1	0	I/O	I/O
FRC(2)	Internal RC	0	0	1	1	1	CLKO	I/O

Note 1: CLKO is not recommended to drive external circuits.

2: This mode is not recommended for some applications; disabling 32x PLL will not allow operation of high-speed ADC and PWM.

18.3.2 OSCILLATOR START-UP TIMER (OST)

In order to ensure that a crystal oscillator (or ceramic resonator) has started and stabilized, an Oscillator Start-up Timer is included. It is a simple 10-bit counter that counts 1024 TOSC cycles before releasing the oscillator clock to the rest of the system. The time-out period is designated as TOST. The TOST time is involved every time the oscillator has to restart (i.e., on POR and wake-up from Sleep). The Oscillator Start-up Timer is applied to the HS Oscillator mode (upon wake-up from Sleep and POR) for the primary oscillator.

18.3.3 PHASE LOCKED LOOP (PLL)

The PLL multiplies the clock, which is generated by the primary oscillator. The PLL is selectable to have a gain of x32 only. Input and output frequency ranges are summarized in Table 18-2.

TABLE 18-2: PLL FREQUENCY RANGE

FIN	PLL Multiplier	FOUT
6.4 MHz	x32	205 MHz
9.7 MHz	x32	310 MHz
14.55 MHz	x32	466 MHz

The PLL features a lock output, which is asserted when the PLL enters a phase locked state. Should the loop fall out of lock (e.g., due to noise), the lock signal will be rescinded. The state of this signal is reflected in the read-only LOCK bit in the OSCCON register.

20.6 MPLAB X SIM Software Simulator

The MPLAB X SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB X SIM Software Simulator fully supports symbolic debugging using the MPLAB XC Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

20.7 MPLAB REAL ICE In-Circuit Emulator System

The MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs all 8, 16 and 32-bit MCU, and DSC devices with the easy-to-use, powerful graphical user interface of the MPLAB X IDE.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ-11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB X IDE. MPLAB REAL ICE offers significant advantages over competitive emulators including full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, logic probes, a ruggedized probe interface and long (up to three meters) interconnection cables.

20.8 MPLAB ICD 3 In-Circuit Debugger System

The MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost-effective, high-speed hardware debugger/programmer for Microchip Flash DSC and MCU devices. It debugs and programs PIC Flash microcontrollers and dsPIC DSCs with the powerful, yet easy-to-use graphical user interface of the MPLAB IDE.

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

20.9 PICkit 3 In-Circuit Debugger/ Programmer

The MPLAB PICkit 3 allows debugging and programming of PIC and dsPIC Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB IDE. The MPLAB PICkit 3 is connected to the design engineer's PC using a full-speed USB interface and can be connected to the target via a Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the Reset line to implement in-circuit debugging and In-Circuit Serial Programming™ (ICSP™).

20.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at V_{DDMIN} and V_{DDMAX} for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages, and a modular, detachable socket assembly to support various package types. The ICSP cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices, and incorporates an MMC card for file storage and data applications.

TABLE 21-5: DC CHARACTERISTICS: OPERATING CURRENT (I_{DD})

DC CHARACTERISTICS			Standard Operating Conditions: 3.3V and 5.0V (±10%) (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Parameter No.	**Typical(1)**	**Max**	**Units**	**Conditions**		
Operating Current (I_{DD})(2)						
DC20a	13	16	mA	+25°C	3.3V	FRC 3.2 MIPS, PLL disabled
DC20b	14	16	mA	+85°C		
DC20c	14	17	mA	+125°C		
DC20d	22	26	mA	+25°C	5V	
DC20e	22	26	mA	+85°C		
DC20f	22	27	mA	+125°C		
DC22a	19	22	mA	+25°C	3.3V	FRC, 4.9 MIPS, PLL disabled
DC22b	19	23	mA	+85°C		
DC22c	19	23	mA	+125°C		
DC22d	30	36	mA	+25°C	5V	
DC22e	30	37	mA	+85°C		
DC22f	31	37	mA	+125°C		
DC23a	27	33	mA	+25°C	3.3V	FRC, 7.3 MIPS, PLL disabled
DC23b	28	33	mA	+85°C		
DC23c	28	34	mA	+125°C		
DC23d	44	53	mA	+25°C	5V	
DC23e	45	53	mA	+85°C		
DC23f	45	54	mA	+125°C		
DC24a	66	79	mA	+25°C	3.3V	FRC 13 MIPS, PLL enabled
DC24b	67	80	mA	+85°C		
DC24c	68	81	mA	+125°C		
DC24d	108	129	mA	+25°C	5V	
DC24e	109	130	mA	+85°C		
DC24f	110	131	mA	+125°C		
DC26a	98	118	mA	+25°C	3.3V	FRC 20 MIPS, PLL enabled
DC26b	99	118	mA	+85°C		
DC26d	159	191	mA	+25°C	5V	
DC26e	160	192	mA	+85°C		
DC26f	161	193	mA	+125°C		
DC27d	222	267	mA	+25°C	5V	FRC, 30 MIPS, PLL enabled
DC27e	223	267	mA	+85°C		

Note 1: Data in "Typical" column is at 5V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature also have an impact on the current consumption. The test conditions for all I_{DD} measurements are as follows:
- All I/O pins are configured as Outputs and pulled to V_{SS}.
- $\overline{MCLR}$ = V_{DD}, WDT and FSCM are disabled.
- CPU, SRAM, Program Memory and Data Memory are operational.
- No peripheral modules are operating.

TABLE 21-12: EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.3V and 5.0V (±10%) (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
OS10	FIN	External CLKI Frequency(2) (External clocks allowed only in EC mode)	6 6	— —	15.00 15.00	MHz MHz	EC EC with 32x PLL
		Oscillator Frequency(2)	6 6	— —	15.00 15.00	MHz MHz	HS FRC internal
OS20	TOSC	TOSC = 1/FOSC(3)	16.5	—	DC	ns	
OS25	TCY	Instruction Cycle Time(2,4)	33	—	DC	ns	
OS30	TosL, TosH	External Clock in (OSC1) High or Low Time(2)	.45 x TOSC	—	—	ns	EC
OS31	TosR, TosF	External Clock in (OSC1) Rise or Fall Time(2)	—	—	20	ns	EC
OS40	TckR	CLKO Rise Time(2,5)	—	6	10	ns	
OS41	TckF	CLKO Fall Time(2,5)	—	6	10	ns	

Note 1: Data in “Typ” column is at 5V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

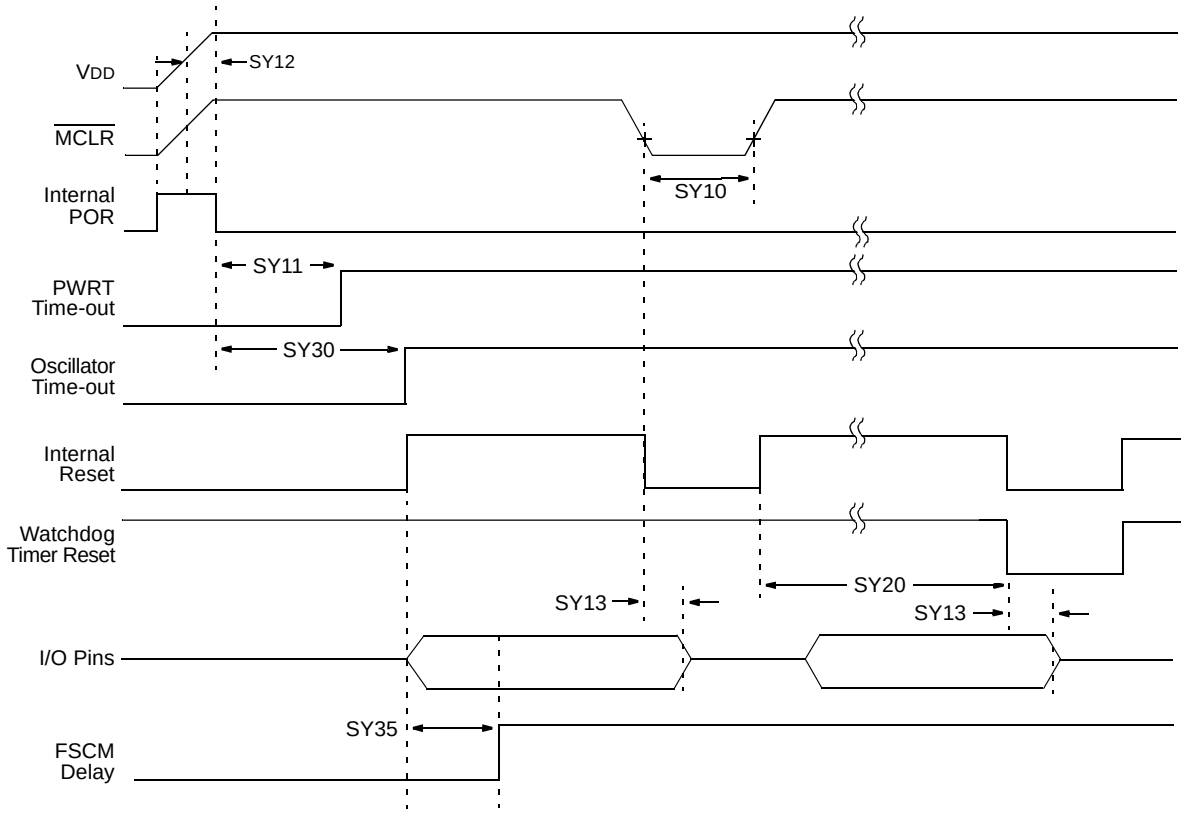
2: These parameters are characterized but not tested in manufacturing.

3: The oscillator frequency (FOSC) is equal to FIN when the PLL is disabled. FOSC is equal to 4 x FIN when the PLL is enabled.

4: Instruction cycle period (TCY) equals two times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at “Min.” values with an external clock applied to the OSC1/CLK1 pin. When an external clock input is used, the “Max.” cycle time limit is “DC” (no clock) for all devices.

5: Measurements are taken in EC mode. The CLKO signal is measured on the OSC2 pin.

FIGURE 21-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING CHARACTERISTICS



Note: Refer to Figure 21-1 for load conditions.

TABLE 21-21: TIMER2 EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions: 3.3V and 5.0V (±10%) (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**		**Min**	**Typ**	**Max**	**Units**	**Conditions**
TB10	TTXH	T2CK High Time	Synchronous, no prescaler	0.5 TCY + 20	—	—	ns	Must also meet Parameter TB15
			Synchronous, with prescaler	10	—	—	ns	
TB11	TTXL	T2CK Low Time	Synchronous, no prescaler	0.5 TCY + 20	—	—	ns	Must also meet Parameter TB15
			Synchronous, with prescaler	10	—	—	ns	
TB15	TTXP	T2CK Input Period	Synchronous, no prescaler	TCY + 10	—	—	ns	N = Prescale value (1, 8, 64, 256)
			Synchronous, with prescaler	Greater of: 20 ns or (TCY + 40)/N	—	—	—	
TB20	TCKEXTMRL	Delay from External T2CK Clock Edge to Timer Increment		0.5 TCY	—	1.5 TCY	—	

TABLE 21-22: TIMER3 EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions: 3.3V and 5.0V (±10%) (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**		**Min**	**Typ**	**Max**	**Units**	**Conditions**
TC10	TTXH	T3CK High Time	Synchronous	0.5 TCY + 20	—	—	ns	Must also meet Parameter TC15
TC11	TTXL	T3CK Low Time	Synchronous	0.5 TCY + 20	—	—	ns	Must also meet Parameter TC15
TC15	TTXP	T3CK Input Period	Synchronous, no prescaler	TCY + 10	—	—	ns	N = Prescale value (1, 8, 64, 256)
			Synchronous, with prescaler	Greater of: 20 ns or (TCY + 40)/N	—	—	—	
TC20	TCKEXTMRL	Delay from External T3CK Clock Edge to Timer Increment		0.5 TCY	—	1.5 TCY	—	

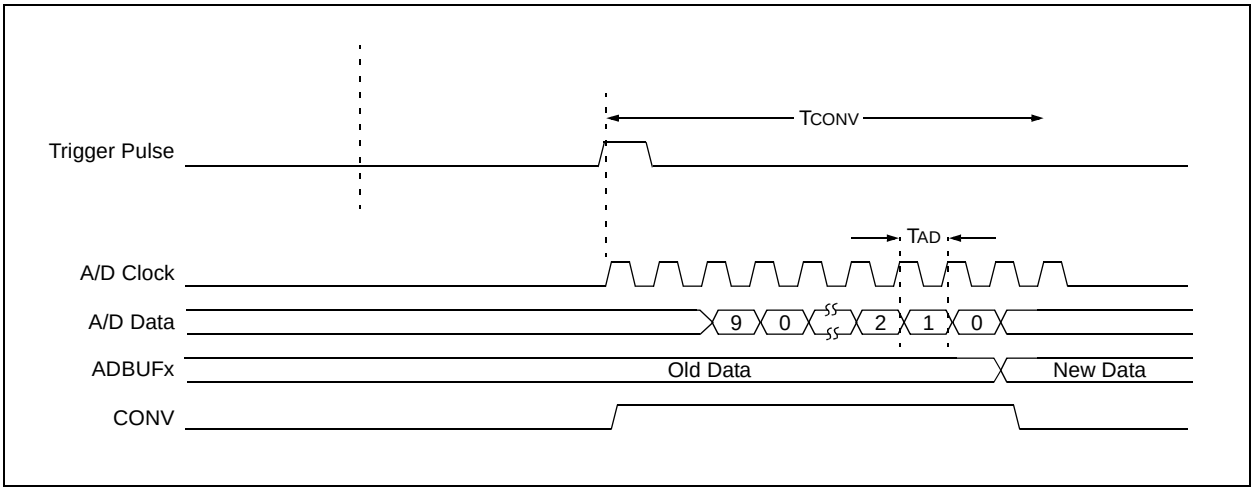
TABLE 21-33: 10-BIT HIGH-SPEED A/D MODULE SPECIFICATIONS (CONTINUED)

AC CHARACTERISTICS			Standard Operating Conditions: 3.3V and 5.0V (±10%) (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ**	**Max.**	**Units**	**Conditions**
AD24	EOFF	Offset Error	—	±0.75	<±2.0	LSb	VINL = AVSS = VSS = 0V, AVDD = VDD = 5V
AD24A	EOFF	Offset Error	—	±0.75	<±2.0	LSb	VINL = AVSS = VSS = 0V, AVDD = VDD = 3.3V
AD25	—	Monotonicity(2)	—	—	—	—	Guaranteed
Dynamic Performance							
AD30	THD	Total Harmonic Distortion	-77	-73	-68	dB	
AD31	SINAD	Signal to Noise and Distortion	—	58	—	dB	
AD32	SFDR	Spurious Free Dynamic Range	—	-73	—	dB	
AD33	FNYQ	Input Signal Bandwidth	—	—	0.5	MHz	
AD34	ENOB	Effective Number of Bits	—	9.4	—	bits	

Note 1: Because the sample caps will eventually lose charge, clock rates below 10 kHz can affect linearity performance, especially at elevated temperatures.

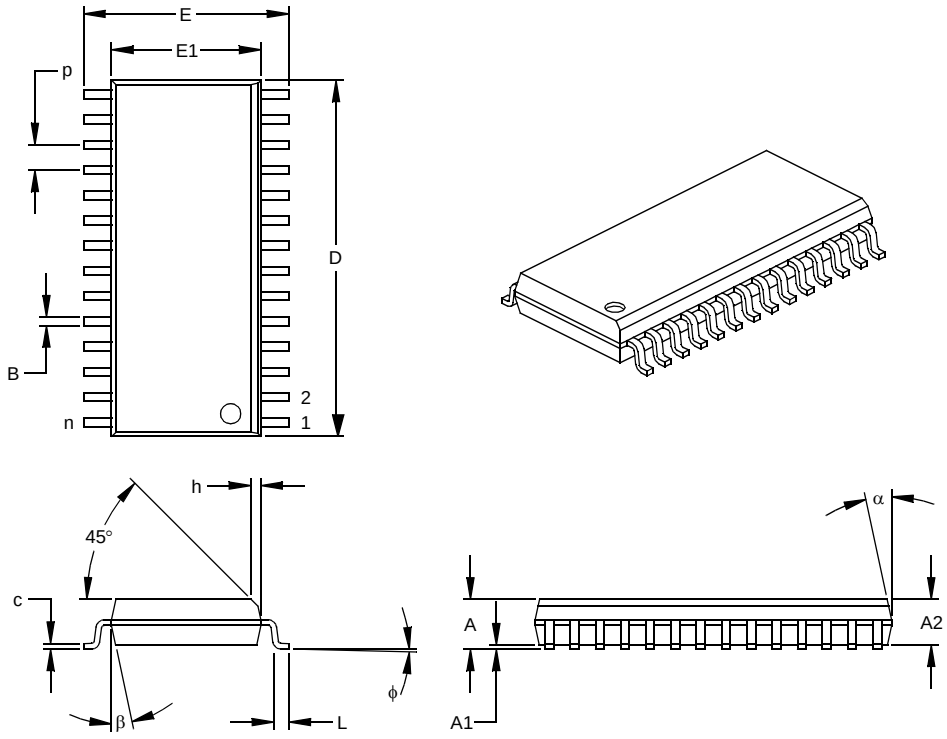
2: The A/D conversion result never decreases with an increase in the input voltage, and has no missing codes.

FIGURE 21-20: A/D CONVERSION TIMING PER INPUT



28-Lead Plastic Small Outline (SO) – Wide, 300 mil Body (SOIC)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		28			28	
Pitch	p		.050			1.27	
Overall Height	A	.093	.099	.104	2.36	2.50	2.64
Molded Package Thickness	A2	.088	.091	.094	2.24	2.31	2.39
Standoff §	A1	.004	.008	.012	0.10	0.20	0.30
Overall Width	E	.394	.407	.420	10.01	10.34	10.67
Molded Package Width	E1	.288	.295	.299	7.32	7.49	7.59
Overall Length	D	.695	.704	.712	17.65	17.87	18.08
Chamfer Distance	h	.010	.020	.029	0.25	0.50	0.74
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle Top	φ	0	4	8	0	4	8
Lead Thickness	c	.009	.011	.013	0.23	0.28	0.33
Lead Width	B	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

***** Controlling Parameter

§ Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.

JEDEC Equivalent: MS-013

Drawing No. C04-052

NOTES: