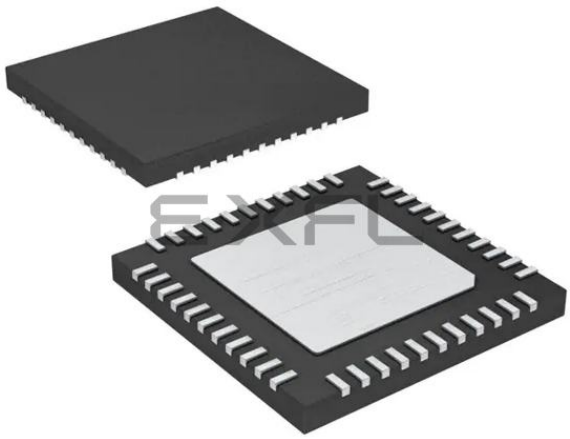
Microchip Technology - DSPIC30F2023T-30I/ML Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	30 MIPs
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	35
Program Memory Size	12KB (4K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic30f2023t-30i-ml

TABLE 1-3: PINOUT I/O DESCRIPTIONS FOR dsPIC30F2023 (CONTINUED)

Pin Name	Pin Type	Buffer Type	Description
PGD PGC PGD1 PGC1 PGD2 PGC2	I/O I I/O I I/O I	ST ST ST ST ST ST	In-Circuit Serial Programming™ data input/output pin. In-Circuit Serial Programming clock input pin. In-Circuit Serial Programming data input/output pin 1. In-Circuit Serial Programming clock input pin 1. In-Circuit Serial Programming data input/output pin 2. In-Circuit Serial Programming clock input pin 2.
RA8-RA11	I/O	ST	PORTA is a bidirectional I/O port.
RB0-RB11	I/O	ST	PORTB is a bidirectional I/O port.
RD0,RD1	I/O	ST	PORTD is a bidirectional I/O port.
RE0-RE7	I/O	ST	PORTE is a bidirectional I/O port.
RF2, RF3, RF6-RF8, RF14, RF15	I/O	ST	PORTF is a bidirectional I/O port.
RG2, RG3	I/O	ST	PORTG is a bidirectional I/O port.
SCK1 SDI1 SDO1 SS1	I/O I O I	ST ST — ST	Synchronous serial clock input/output for SPI #1. SPI #1 Data In. SPI #1 Data Out. SPI #1 Slave Synchronization.
SCL SDA	I/O I/O	ST ST	Synchronous serial clock input/output for I^2C. Synchronous serial data input/output for I^2C.
T1CK T2CK	I I	ST ST	Timer1 external clock input. Timer2 external clock input.
U1RX U1TX U1ARX U1ATX	I O I O	ST — ST —	UART1 Receive. UART1 Transmit. Alternate UART1 Receive. Alternate UART1 Transmit
CMP1A CMP1B CMP1C CMP1D CMP2A CMP2B CMP2C CMP2D CMP3A CMP3B CMP3C CMP3D CMP4A CMP4B CMP4C CMP4D	I I I I I I I I I I I I I I I I	Analog Analog Analog Analog Analog Analog Analog Analog Analog Analog Analog Analog Analog Analog Analog Analog	Comparator 1 Channel A Comparator 1 Channel B Comparator 1 Channel C Comparator 1 Channel D Comparator 2 Channel A Comparator 2 Channel B Comparator 2 Channel C Comparator 2 Channel D Comparator 3 Channel A Comparator 3 Channel B Comparator 3 Channel C Comparator 3 Channel D Comparator 4 Channel A Comparator 4 Channel B Comparator 4 Channel C Comparator 4 Channel D
CN0-CN7	I	ST	Input Change notification inputs Can be software programmed for internal weak pull-ups on all inputs.
V_{DD}	P	—	Positive supply for logic and I/O pins.
V_{SS}	P	—	Ground reference for logic and I/O pins.
EXTREF	I	Analog	External reference to Comparator DAC

Legend: CMOS = CMOS compatible input or output; Analog = Analog input
ST = Schmitt Trigger input with CMOS levels; O = Output
I = Input; P = Power

2.2 Programmer's Model

The programmer's model is shown in Figure 2-1 and consists of 16x16-bit working registers (W0 through W15), 2x40-bit accumulators (ACCA and ACCB), STATUS register (SR), Data Table Page register (TBLPAG), Program Space Visibility Page register (PSVPAG), DO and REPEAT registers (DOSTART, DOEND, DCOUNT and RCOUNT), and Program Counter (PC). The working registers can act as data, address or offset registers. All registers are memory mapped. W0 acts as the W register for file register addressing.

Some of these registers have a shadow register associated with each of them, as shown in Figure 2-1. The shadow register is used as a temporary holding register and can transfer its contents to or from its host register upon the occurrence of an event. None of the shadow registers are accessible directly. The following rules apply for transfer of registers into and out of shadows.

- `PUSH.S` and `POP.S`
  W0, W1, W2, W3, SR (DC, N, OV, Z and C bits only) are transferred.
- `DO` instruction
  DOSTART, DOEND, DCOUNT shadows are pushed on loop start, and popped on loop end.

When a byte operation is performed on a working register, only the Least Significant Byte (LSB) of the target register is affected. However, a benefit of memory mapped working registers is that both the Least and Most Significant Bytes (MSBs) can be manipulated through byte wide data memory space accesses.

2.2.1 SOFTWARE STACK POINTER/ FRAME POINTER

The dsPIC® DSC devices contain a software stack. W15 is the dedicated software Stack Pointer (SP), and will be automatically modified by exception processing and subroutine calls and returns. However, W15 can be referenced by any instruction in the same manner as all other W registers. This simplifies the reading, writing and manipulation of the Stack Pointer (e.g., creating stack frames).

Note:	In order to protect against misaligned stack accesses, W15<0> is always clear.

W15 is initialized to 0x0800 during a Reset. The user may reprogram the SP during initialization to any location within data space.

W14 has been dedicated as a Stack Frame Pointer as defined by the `LNK` and `ULNK` instructions. However, W14 can be referenced by any instruction in the same manner as all other W registers.

2.2.2 STATUS REGISTER

The dsPIC DSC core has a 16-bit STATUS Register (SR), the LSB of which is referred to as the SR Low Byte (SRL) and the MSB as the SR High Byte (SRH). See Figure 2-1 for SR layout.

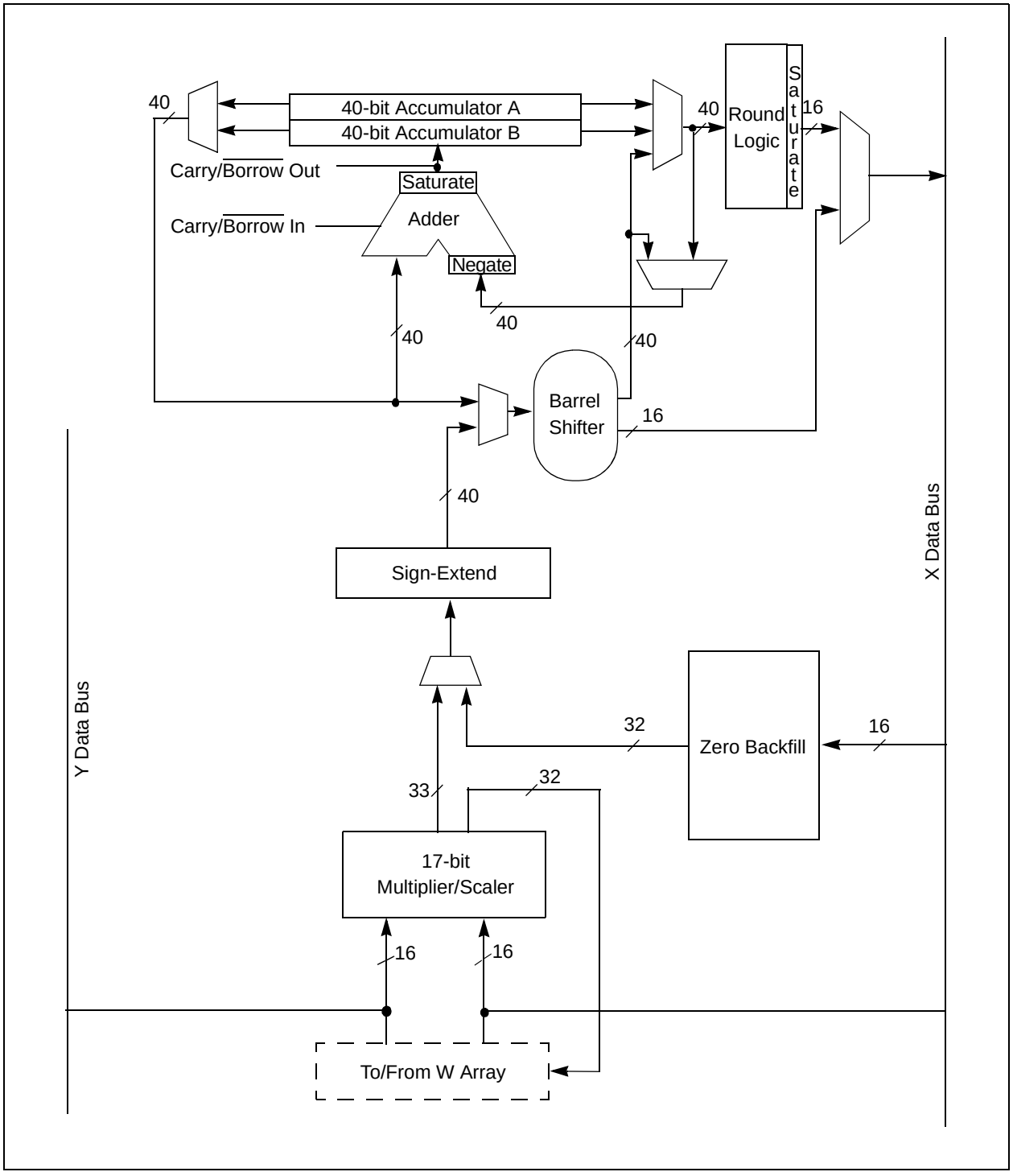
SRL contains all the MCU ALU operation status flags (including the Z bit), as well as the CPU Interrupt Priority Level Status bits, IPL<2:0>, and the REPEAT active Status bit, RA. During exception processing, SRL is concatenated with the MSB of the PC to form a complete word value, which is then stacked.

The upper byte of the STATUS register contains the DSP Adder/Subtracter status bits, the DO Loop Active bit (DA) and the Digit Carry (DC) Status bit.

2.2.3 PROGRAM COUNTER

The Program Counter is 23 bits wide. Bit 0 is always clear. Therefore, the PC can address up to 4M instruction words.

FIGURE 2-2: DSP ENGINE BLOCK DIAGRAM



The SA and SB bits are modified each time data passes through the adder/subtracter, but can only be cleared by the user. When set, they indicate that the accumulator has overflowed its maximum range (bit 31 for 32-bit saturation, or bit 39 for 40-bit saturation) and will be saturated (if saturation is enabled). When saturation is not enabled, SA and SB default to bit 39 overflow and thus indicate that a catastrophic overflow has occurred. If the COVTE bit in the INTCON1 register is set, SA and SB bits will generate an arithmetic warning trap when saturation is disabled.

The overflow and saturation Status bits can optionally be viewed in the STATUS Register (SR) as the logical OR of OA and OB (in bit OAB) and the logical OR of SA and SB (in bit SAB). This allows programmers to check one bit in the STATUS Register to determine if either accumulator has overflowed, or one bit to determine if either accumulator has saturated. This is useful for complex number arithmetic, which typically uses both the accumulators.

The device supports three Saturation and Overflow modes.

1. Bit 39 Overflow and Saturation:
   When bit 39 overflow and saturation occurs, the saturation logic loads the maximally positive 9.31 (0x7FFFFFFFF) or maximally negative 9.31 value (0x8000000000) into the target accumulator. The SA or SB bit is set and remains set until cleared by the user. This is referred to as 'super saturation' and provides protection against erroneous data or unexpected algorithm problems (e.g., gain calculations).
2. Bit 31 Overflow and Saturation:
   When bit 31 overflow and saturation occurs, the saturation logic then loads the maximally positive 1.31 value (0x007FFFFFFF) or maximally negative 1.31 value (0x0080000000) into the target accumulator. The SA or SB bit is set and remains set until cleared by the user. When this Saturation mode is in effect, the guard bits are not used (so the OA, OB or OAB bits are never set).
3. Bit 39 Catastrophic Overflow
   The bit 39 overflow Status bit from the adder is used to set the SA or SB bit, which remain set until cleared by the user. No saturation operation is performed and the accumulator is allowed to overflow (destroying its sign). If the COVTE bit in the INTCON1 register is set, a catastrophic overflow can initiate a trap exception.

2.4.2.2 Accumulator 'Write Back'

The MAC class of instructions (with the exception of MPY, MPY.N, ED and EDAC) can optionally write a rounded version of the high word (bits 31 through 16) of the accumulator that is not targeted by the instruction into data space memory. The write is performed across the X bus into combined X and Y address space. The following addressing modes are supported:

1. W13, Register Direct:
   The rounded contents of the non-target accumulator are written into W13 as a 1.15 fraction.
2. [W13] + = 2, Register Indirect with Post-Increment: The rounded contents of the non-target accumulator are written into the address pointed to by W13 as a 1.15 fraction. W13 is then incremented by 2 (for a word write).

2.4.2.3 Round Logic

The round logic is a combinational block, which performs a conventional (biased) or convergent (unbiased) round function during an accumulator write (store). The Round mode is determined by the state of the RND bit in the CORCON register. It generates a 16-bit, 1.15 data value which is passed to the data space write saturation logic. If rounding is not indicated by the instruction, a truncated 1.15 data value is stored and the least significant word (lsw) is simply discarded.

Conventional rounding takes bit 15 of the accumulator, zero-extends it and adds it to the ACCxH word (bits 16 through 31 of the accumulator). If the ACCxL word (bits 0 through 15 of the accumulator) is between 0x8000 and 0xFFFF (0x8000 included), ACCxH is incremented. If ACCxL is between 0x0000 and 0x7FFF, ACCxH is left unchanged. A consequence of this algorithm is that over a succession of random rounding operations, the value will tend to be biased slightly positive.

Convergent (or unbiased) rounding operates in the same manner as conventional rounding, except when ACCxL equals 0x8000. If this is the case, the LSb (bit 16 of the accumulator) of ACCxH is examined. If it is '1', ACCxH is incremented. If it is '0', ACCxH is not modified. Assuming that bit 16 is effectively random in nature, this scheme will remove any rounding bias that may accumulate.

The SAC and SAC.R instructions store either a truncated (SAC) or rounded (SAC.R) version of the contents of the target accumulator to data memory, via the X bus (subject to data saturation, see **Section 2.4.2.4 "Data Space Write Saturation"**). Note that for the MAC class of instructions, the accumulator write back operation will function in the same manner, addressing combined MCU (X and Y) data space though the X bus. For this class of instructions, the data is always subject to rounding.

REGISTER 5-1: INTCON1: INTERRUPT CONTROL REGISTER 1 (CONTINUED)

bit 2 **STKERR:** Stack Error Trap Status bit
1 = Stack error trap has occurred
0 = Stack error trap has not occurred

bit 1 **OSCFAIL:** Oscillator Failure Trap Status bit
1 = Oscillator failure trap has occurred
0 = Oscillator failure trap has not occurred

bit 0 **Unimplemented:** Read as '0'

9.0 TIMER2/3 MODULE

Note: This data sheet summarizes features of this group of dsPIC30F devices and is not intended to be a complete reference source. For more information on the CPU, peripherals, register descriptions and general device functionality, refer to the "*dsPIC30F Family Reference Manual*" (DS70046).

This section describes the 32-bit General Purpose Timer module (Timer2/3) and associated operational modes. Figure 9-1 depicts the simplified block diagram of the 32-bit Timer2/3 module. Figure 9-2 and Figure 9-3 show Timer2/3 configured as two independent 16-bit timers: Timer2 and Timer3, respectively.

Note: The dsPIC30F1010 device does not feature Timer3. Timer2 is a 'Type B' timer and Timer3 is a 'Type C' timer. Please refer to the appropriate timer type in **Section 21.0 "Electrical Characteristics"** of this document.

The Timer2/3 module is a 32-bit timer, which can be configured as two 16-bit timers, with selectable operating modes. These timers are utilized by other peripheral modules such as:

- Input Capture
- Output Compare/Simple PWM

The following sections provide a detailed description, including setup and control registers, along with associated block diagrams for the operational modes of the timers.

The 32-bit timer has the following modes:

- Two independent 16-bit timers (Timer2 and Timer3) with all 16-bit operating modes (except Asynchronous Counter mode)
- Single 32-bit Timer operation
- Single 32-bit Synchronous Counter

Further, the following operational characteristics are supported:

- ADC Event Trigger
- Timer Gate Operation
- Selectable Prescaler Settings
- Timer Operation during Idle and Sleep modes
- Interrupt on a 32-bit Period Register Match

These operating modes are determined by setting the appropriate bit(s) in the 16-bit T2CON and T3CON SFRs.

For 32-bit timer/counter operation, Timer2 is the least significant word and Timer3 is the most significant word of the 32-bit timer.

Note: For 32-bit timer operation, T3CON control bits are ignored. Only T2CON control bits are used for setup and control. Timer 2 clock and gate inputs are utilized for the 32-bit timer module, but an interrupt is generated with the Timer3 interrupt flag (T3IF) and the interrupt is enabled with the Timer3 interrupt enable bit (T3IE).

16-bit Mode: In the 16-bit mode, Timer2 and Timer3 can be configured as two independent 16-bit timers. Each timer can be set up in either 16-bit Timer mode or 16-bit Synchronous Counter mode. See **Section 8.0 "Timer1 Module"** for details on these two operating modes.

The only functional difference between Timer2 and Timer3 is that Timer2 provides synchronization of the clock prescaler output. This is useful for high-frequency external clock inputs.

32-bit Timer Mode: In the 32-bit Timer mode, the timer increments on every instruction cycle up to a match value, preloaded into the combined 32-bit period register PR3/PR2, then resets to '0' and continues to count.

For synchronous 32-bit reads of the Timer2/Timer3 pair, reading the least significant word (TMR2 register) will cause the most significant word to be read and latched into a 16-bit holding register, termed TMR3HLD.

For synchronous 32-bit writes, the holding register (TMR3HLD) must first be written to. When followed by a write to the TMR2 register, the contents of TMR3HLD will be transferred and latched into the MSB of the 32-bit timer (TMR3).

32-bit Synchronous Counter Mode: In the 32-bit Synchronous Counter mode, the timer increments on the rising edge of the applied external clock signal, which is synchronized with the internal phase clocks. The timer counts up to a match value preloaded in the combined 32-bit period register, PR3/PR2, then resets to '0' and continues.

When the timer is configured for the Synchronous Counter mode of operation and the CPU goes into the Idle mode, the timer will stop incrementing, unless the TSIDL (T2CON<13>) bit = 0. If TSIDL = 1, the timer module logic will resume the incrementing sequence upon termination of the CPU Idle mode.

TABLE 9-1: TIMER2/3 REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
TMR2	0106	Timer2 Register																uuuu uuuu uuuu uuuu
TMR3HLD	0108	Timer3 Holding Register (For 32-bit timer operations only)																uuuu uuuu uuuu uuuu
TMR3	010A	Timer3 Register																uuuu uuuu uuuu uuuu
PR2	010C	Period Register 2																1111 1111 1111 1111
PR3	010E	Period Register 3																1111 1111 1111 1111
T2CON	0110	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS<1:0>		T32	—	TCS	—	0000 0000 0000 0000
T3CON	0112	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS<1:0>		—	—	TCS	—	0000 0000 0000 0000

Legend: u = uninitialized bit

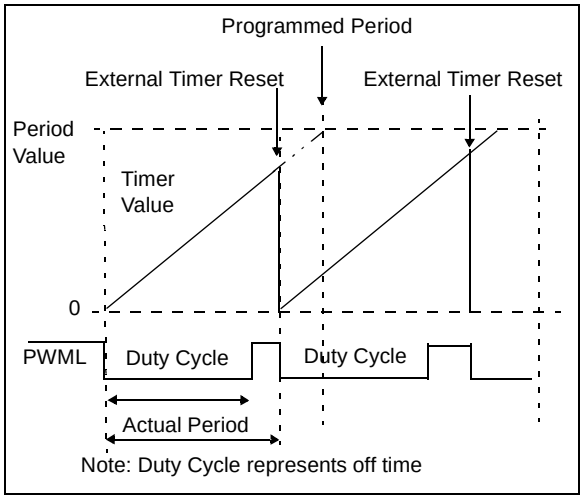
Note: Refer to the "*dsPIC30F Family Reference Manual*" (DS70046) for descriptions of register bit fields.

NOTES:

12.4.7 CONSTANT OFF-TIME PWM

Constant Off-Time mode is shown in Figure 12-9. Constant Off-Time PWM is a variable-frequency mode where the actual PWM period is less than or equal to the specified period value. The PWM time base is externally reset some time after the PWM signal duty cycle value has been reached, and the PWM signal has been deasserted. This mode is implemented by enabling the On-Time PWM mode (Current Reset mode) and using the complementary output.

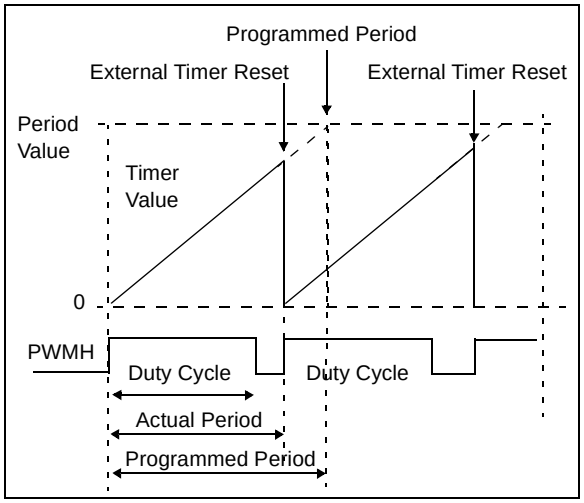
FIGURE 12-9: CONSTANT OFF-TIME PWM



12.4.8 CURRENT RESET PWM MODE

Current Reset PWM is shown in Figure 12-10. Current Reset PWM uses a Variable-Frequency mode where the actual PWM period is less than or equal to the specified period value. The PWM time base is externally reset some time after the PWM signal duty cycle value has been reached and the PWM signal has been deasserted. Current Reset PWM is a constant on-time PWM mode.

FIGURE 12-10: CURRENT RESET PWM

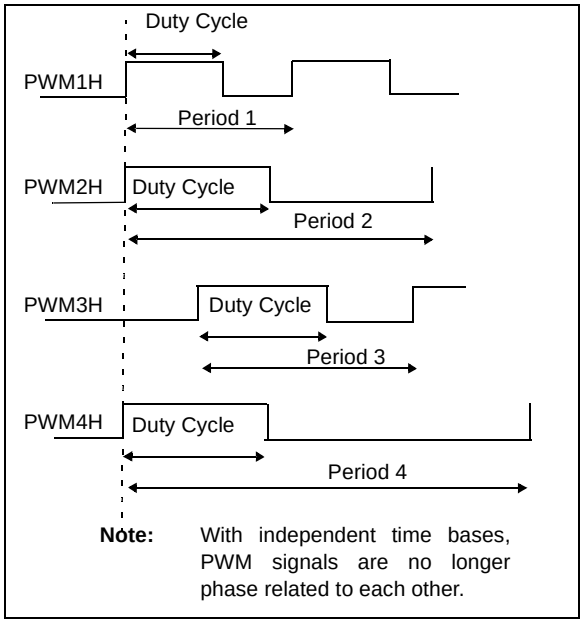


Typically, in the converter application, an energy storage inductor is charged with current while the PWM signal is asserted, and the inductor current is discharged by the load when the PWM signal is deasserted. In this application of current reset PWM, an external current measurement circuit determines when the inductor is discharged, and then generates a signal that the PWM module uses to reset the time base counter. In Current Reset mode, complementary outputs are available.

12.4.9 INDEPENDENT TIME BASE PWM

Independent Time Base PWM, as shown in Figure 12-11, is often used when the dsPIC DSC is controlling different power converter subcircuits such as the Power Factor Correction circuit, which may use 100 kHz PWM, and the full-bridge forward converter section may use 250 kHz PWM.

FIGURE 12-11: INDEPENDENT TIME BASE PWM



12.25 Simultaneous PWM Faults and Current Limits

The current-limit override function, if enabled and active, forces the PWMxH,L pins to the values specified by the CLDAT<1:0> bits in the IOCONx registers UNLESS the Fault function is enabled and active. If the selected Fault input is active, the PWMxH,L outputs assume the values specified by the FLTDAT<1:0> bits in the IOCONx registers.

12.26 PWM Fault and Current-Limit TRG Outputs To ADC

The Fault and current-limit source selection fields in the FCLCONx registers (FLTSRC<3:0> and CLSRC<3:0>) control multiplexers in each PWM generator module. The control multiplexers select the desired Fault and current-limit signals for their respective modules. The selected Fault and current-limit signals are also available to the ADC module as trigger signals that initiate ADC sampling and conversion operations.

12.27 PWM Output Override Priority

If the PWM module is enabled, the priority of PWMx pin ownership is:

1. PWM Generator (lowest priority)
2. Output Override
3. Current-Limit Override
4. Fault Override
5. PENx (GPIO/PWM) ownership (highest priority)

If the PWM module is disabled, the GPIO module controls the PWMx pins.

12.28 Fault and Current-Limit Override Issues with Dead-Time Logic

The PWMxH and PWMxL outputs are immediately driven low (deasserted) as specified by the CLDAT<1:0> and the FLTDAT<1:0> bits when a current-limit or a Fault event occurs.

The override data is gated with the PWM signals going into the dead-time logic block, and at the output of the PWM module, just ahead of the PWM pin output buffers.

Many applications require fast response to current shutdown for accurate current control and/or to limit circuitry damage to Fault currents.

Some applications will set the complementary PWM outputs high in synchronous rectifier designs when a Fault or current-limit event occurs. If the CLDAT or FLTDAT bits are set to '1', and their associated event occurs, then these asserted outputs will be delayed by clocked logic in the dead-time circuitry.

12.29 Asserting Outputs via Current Limit

It is possible to use the CLDAT bits to assert the PWMxH,L outputs in response to a current-limit event. Such behavior could be used as a current "force" feature in response to an external current or voltage measurement that indicates a sudden sharp increase in the load on the power-converter output. Forcing the PWM "ON" could be viewed as a "Feed-Forward" term that allows quick system response to unexpected load increases without waiting for the digital control loop to respond.

12.30 PWM Immediate Update

For high-performance PWM control-loop applications, the user may want to force the duty cycle updates to occur immediately. Setting the IUE bit in the PWMCONx register enables this feature.

In a closed-loop control application, any delay between the sensing of a system's state and the subsequent outputting of PWM control signals that drive the application reduces the loop stability. Setting the IUE bit minimizes the delay between writing the duty cycle registers and the response of the PWM generators to that change.

12.31 PWM Output Override

All control bits associated with the PWM output override function are contained in the IOCONx register.

If the PENH, PENL bits are set, the PWM module controls the PWMx output pins.

The PWM output override bits allow the user to manually drive the PWM I/O pins to specified logic states independent of the duty cycle comparison units.

The OVRDAT<1:0> bits in the IOCONx register determine the state of the PWM I/O pins when a particular output is overridden via the OVRENH,L bits.

The OVRENH, OVRENL bits are active high control bits. When the OVREN bits are set, the corresponding OVRDAT bit overrides the PWM output from the PWM generator.

12.31.1 COMPLEMENTARY OUTPUT MODE

When the PWM is in Complementary Output mode, the dead-time generator is still active with overrides. The output overrides and Fault overrides generate control signals used by the dead-time unit to set the outputs as requested, including dead time.

Dead-time insertion can be performed when PWM channels are overridden manually.

REGISTER 13-3: SPIxCON2: SPIx CONTROL REGISTER 2

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
FRMEN	SPIFSD	FRMPOL	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	U-0
—	—	—	—	—	—	FRMDLY	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **FRMEN**: Framed SPIx Support bit
1 = Framed SPIx support enabled ($\overline{SS}$x pin used as frame sync pulse input/output)
0 = Framed SPIx support disabled

bit 14 **SPIFSD**: Frame Sync Pulse Direction Control bit
1 = Frame sync pulse input (slave)
0 = Frame sync pulse output (master)

bit 13 **FRMPOL**: Frame Sync Pulse Polarity bit
1 = Frame sync pulse is active-high
0 = Frame sync pulse is active-low

bit 12-2 **Unimplemented:** Read as ‘0’

bit 1 **FRMDLY**: Frame Sync Pulse Edge Select bit
1 = Frame sync pulse coincides with first bit clock
0 = Frame sync pulse precedes first bit clock

bit 0 **Unimplemented:** This bit must not be set to ‘1’ by the user application.

REGISTER 15-1: U1MODE: UART1 MODE REGISTER (CONTINUED)

bit 2-1 **PDSEL1:PDSEL0:** Parity and Data Selection bits

11 = 9-bit data, no parity
10 = 8-bit data, odd parity
01 = 8-bit data, even parity
00 = 8-bit data, no parity

bit 0 **STSEL:** Stop Bit Selection bit

1 = Two Stop bits
0 = One Stop bit

17.0 SMPS COMPARATOR MODULE

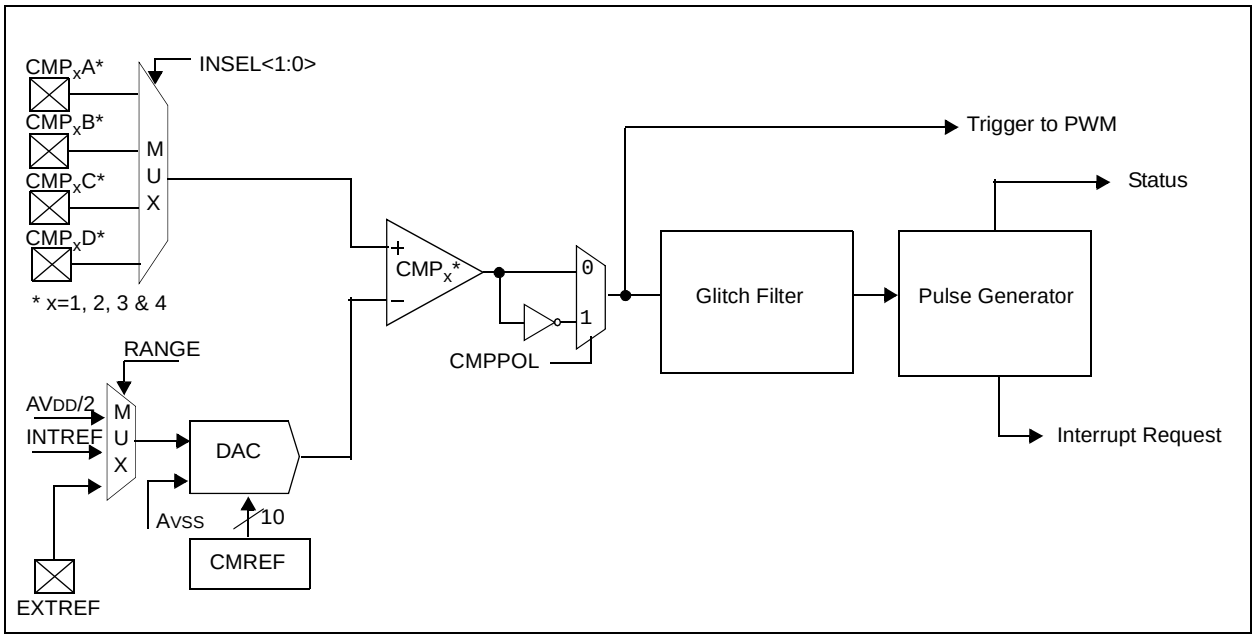
Note: This data sheet summarizes features of this group of dsPIC30F devices and is not intended to be a complete reference source. For more information on the CPU, peripherals, register descriptions and general device functionality, refer to the "*dsPIC30F Family Reference Manual*" (DS70046).

The dsPIC30F SMPS Comparator module monitors current and/or voltage transients that may be too fast for the CPU and ADC to capture.

17.1 Features Overview

- 16 comparator inputs
- 10-bit DAC provides reference
- Programmable output polarity
- Interrupt generation capability
- Selectable Input sources
- DAC has three ranges of operation:
  - AVDD/2
  - Internal Reference 1.2V 1%
  - External Reference < (AVDD - 1.6V)
- ADC sample and convert trigger capability
- Can be disabled to reduce power consumption
- Functional support for PWM Module:
  - PWM Duty Cycle Control
  - PWM Period Control
  - PWM Fault Detect

FIGURE 17-1: COMPARATOR MODULE BLOCK DIAGRAM



17.2 Module Applications

This module provides a means for the SMPS dsPIC DSC devices to monitor voltage and currents in a power conversion application. The ability to detect transient conditions and stimulate the dsPIC DSC processor and/or peripherals without requiring the processor and ADC to constantly monitor voltages or currents frees the dsPIC DSC to perform other tasks.

The Comparator module has a high-speed comparator and an associated 10-bit DAC that provides a programmable reference voltage to one input of the comparator. The polarity of the comparator output is user programmable. The output of the module can be used in the following modes:

- Generate an interrupt
- Trigger an ADC sample and convert process
- Truncate the PWM signal (current limit)
- Truncate the PWM period (current minimum)
- Disable the PWM outputs (Fault-latch)

The output of the Comparator module may be used in multiple modes at the same time, such as: (1) generate an interrupt, (2) have the ADC take a sample and convert it and (3) truncate the PWM output in response to a voltage being detected beyond its expected value.

The Comparator module can also be used to wake-up the system from Sleep or Idle mode when the analog input voltage exceeds the programmed threshold voltage.

REGISTER 17-1: COMPARATOR CONTROL REGISTERx (CMPCONx)

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
CMPON	—	CMPSIDL	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0	R/W-0	R/W-0
INSEL<1:0>		EXTREF	—	CMPSTAT	—	CMPPOL	RANGE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **CMPON:** A/D Operating Mode bit
1 = Comparator module is enabled
0 = Comparator module is disabled (reduces power consumption)

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **CMPSIDL:** Stop in Idle Mode bit
1 = Discontinue module operation when device enters Idle mode.
0 = Continue module operation in Idle mode.

If a device has multiple comparators, any CMPSIDL bit set to ‘1’ disables **ALL** comparators while in Idle mode.

bit 12-8 **Reserved:** Read as ‘0’

bit 7-6 **INSEL<1:0>:** Input Source Select for Comparator bits
00 = Select CMPxA input pin
01 = Select CMPxB input pin
10 = Select CMPxC input pin
11 = Select CMPxD input pin

bit 5 **EXTREF:** Enable External Reference bit
1 = External source provides reference to DAC
0 = Internal reference sources provide source to DAC

bit 4 **Reserved:** Read as ‘0’

bit 3 **CMPSTAT:** Current State of Comparator Output Including CMPPOL Selection bit

bit 2 **Reserved:** Read as ‘0’

bit 1 **CMPPOL:** Comparator Output Polarity Control bit
1 = Output is inverted
0 = Output is non inverted

bit 0 **RANGE:** Selects DAC Output Voltage Range bit
1 = High Range: Max DAC value = AV_{DD}/2, 2.5V @ 5 volt V_{DD}
0 = Low Range: Max DAC value = INTREF, 1.2V ±1%

18.9.2 IDLE MODE

In Idle mode, the clock to the CPU is shutdown while peripherals keep running. Unlike Sleep mode, the clock source remains active.

Several peripherals have a control bit in each module that allows them to operate during Idle.

LPRC fail-safe clock remains active if clock failure detect is enabled.

The processor wakes up from Idle if at least one of the following conditions is true:

- on any interrupt that is individually enabled (IE bit is '1') and meets the required priority level
- on any Reset (POR, $\overline{\text{MCLR}}$)
- on WDT time-out

Upon wake-up from Idle mode, the clock is reapplied to the CPU and instruction execution begins immediately, starting with the instruction following the PWRSAV instruction.

Any interrupt that is individually enabled (using IE bit) and meets the prevailing priority level will be able to wake-up the processor. The processor will process the interrupt and branch to the ISR. The Idle status bit in RCON register is set upon wake-up.

Any Reset, other than POR, will set the Idle status bit. On a POR, the Idle bit is cleared.

If Watchdog Timer is enabled, then the processor will wake-up from Idle mode upon WDT time-out. The Idle and WDTO status bits are both set.

Unlike wake-up from Sleep, there are no time delays involved in wake-up from Idle.

18.10 Device Configuration Registers

The Configuration bits in each device Configuration register specify some of the device modes and are programmed by a device programmer, or by using the In-Circuit Serial Programming (ICSP) feature of the device. Each device Configuration register is a 24-bit register, but only the lower 16 bits of each register are used to hold configuration data. There are six Configuration registers available to the user:

1. FBS (0xF80000): Boot Code Segment Configuration Register
2. FGS (0xF80004): General Code Segment Configuration Register
3. FOSCEL (0xF80006): Oscillator Selection Configuration Register
4. FOSC (0xF80008): Oscillator Configuration Register
5. FWDT (0xF8000A): Watchdog Timer Configuration Register
6. FPOR (0xF8000C): Power-On Reset Configuration Register

The placement of the Configuration bits is automatically handled when you select the device in your device programmer. The desired state of the Configuration bits may be specified in the source code (dependent on the language tool used), or through the programming interface. After the device has been programmed, the application software may read the Configuration bit values through the table read instructions. For additional information, please refer to the programming specifications of the device.

Note:	If the code protection configuration fuse bits (GSS<1:0> and GWRP in the FGS register) have been programmed, an erase of the entire code-protected device is only possible at voltages $V_{DD} \geq 4.5V$.

Table 18-5 shows the bit descriptions of the FGS and FBS registers for the dsPIC30F1010. Table 18-6 shows the bit descriptions of the FGS and FBS registers for dsPIC30F202x devices. Table 18-7 shows the bit descriptions of FWDT and the FPOR registers for dsPIC30F1010/202X devices.

TABLE 19-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of words	# of cycles	Status Flags Affected
11	BTSS	BTSS f,#bit4	Bit Test f, Skip if Set	1	1 (2 or 3)	None
		BTSS Ws,#bit4	Bit Test Ws, Skip if Set	1	1 (2 or 3)	None
12	BTST	BTST f,#bit4	Bit Test f	1	1	Z
		BTST.C Ws,#bit4	Bit Test Ws to C	1	1	C
		BTST.Z Ws,#bit4	Bit Test Ws to Z	1	1	Z
		BTST.C Ws,Wb	Bit Test Ws<Wb> to C	1	1	C
		BTST.Z Ws,Wb	Bit Test Ws<Wb> to Z	1	1	Z
13	BTSTS	BTSTS f,#bit4	Bit Test then Set f	1	1	Z
		BTSTS.C Ws,#bit4	Bit Test Ws to C, then Set	1	1	C
		BTSTS.Z Ws,#bit4	Bit Test Ws to Z, then Set	1	1	Z
14	CALL	CALL lit23	Call subroutine	2	2	None
		CALL Wn	Call indirect subroutine	1	2	None
15	CLR	CLR f	f = 0x0000	1	1	None
		CLR WREG	WREG = 0x0000	1	1	None
		CLR Ws	Ws = 0x0000	1	1	None
		CLR Acc,Wx,Wxd,Wy,Wyd,AWB	Clear Accumulator	1	1	OA,OB,SA,SB
16	CLRWDT	CLRWDT	Clear Watchdog Timer	1	1	WDTO,Sleep
17	COM	COM f	$f = \overline{f}$	1	1	N,Z
		COM f,WREG	$WREG = \overline{f}$	1	1	N,Z
		COM Ws,Wd	$Wd = \overline{Ws}$	1	1	N,Z
18	CP	CP f	Compare f with WREG	1	1	C,DC,N,OV,Z
		CP Wb,#lit5	Compare Wb with lit5	1	1	C,DC,N,OV,Z
		CP Wb,Ws	Compare Wb with Ws (Wb – Ws)	1	1	C,DC,N,OV,Z
19	CP0	CP0 f	Compare f with 0x0000	1	1	C,DC,N,OV,Z
		CP0 Ws	Compare Ws with 0x0000	1	1	C,DC,N,OV,Z
20	CPB	CPB f	Compare f with WREG, with Borrow	1	1	C,DC,N,OV,Z
		CPB Wb,#lit5	Compare Wb with lit5, with Borrow	1	1	C,DC,N,OV,Z
		CPB Wb,Ws	Compare Wb with Ws, with Borrow ($Wb – Ws – \overline{C}$)	1	1	C,DC,N,OV,Z
21	CPSEQ	CPSEQ Wb, Wn	Compare Wb with Wn, skip if =	1	1 (2 or 3)	None
22	CPSGT	CPSGT Wb, Wn	Compare Wb with Wn, skip if >	1	1 (2 or 3)	None
23	CPSLT	CPSLT Wb, Wn	Compare Wb with Wn, skip if <	1	1 (2 or 3)	None
24	CPSNE	CPSNE Wb, Wn	Compare Wb with Wn, skip if ≠	1	1 (2 or 3)	None
25	DAW	DAW Wn	Wn = decimal adjust Wn	1	1	C
26	DEC	DEC f	f = f –1	1	1	C,DC,N,OV,Z
		DEC f,WREG	WREG = f –1	1	1	C,DC,N,OV,Z
		DEC Ws,Wd	Wd = Ws – 1	1	1	C,DC,N,OV,Z
27	DEC2	DEC2 f	f = f –2	1	1	C,DC,N,OV,Z
		DEC2 f,WREG	WREG = f – 2	1	1	C,DC,N,OV,Z
		DEC2 Ws,Wd	Wd = Ws – 2	1	1	C,DC,N,OV,Z
28	DISI	DISI #lit14	Disable Interrupts for k instruction cycles	1	1	None
29	DIV	DIV.S Wm,Wn	Signed 16/16-bit Integer Divide	1	18	N,Z,C, OV
		DIV.SD Wm,Wn	Signed 32/16-bit Integer Divide	1	18	N,Z,C, OV
		DIV.U Wm,Wn	Unsigned 16/16-bit Integer Divide	1	18	N,Z,C, OV
		DIV.UD Wm,Wn	Unsigned 32/16-bit Integer Divide	1	18	N,Z,C, OV
30	DIVF	DIVF Wm,Wn	Signed 16/16-bit Fractional Divide	1	18	N,Z,C, OV
31	DO	DO #lit14,Expr	Do code to PC + Expr, lit14 + 1 times	2	2	None
		DO Wn,Expr	Do code to PC + Expr, (Wn) + 1 times	2	2	None
32	ED	ED Wm * Wm,Acc,Wx,Wy,Wxd	Euclidean Distance (no accumulate)	1	1	OA,OB,OAB, SA,SB,SAB
33	EDAC	EDAC Wm * Wm,Acc,Wx,Wy,Wxd	Euclidean Distance	1	1	OA,OB,OAB, SA,SB,SAB

TABLE 21-16: AC CHARACTERISTICS: INTERNAL RC JITTER

AC CHARACTERISTICS		Standard Operating Conditions: 3.3V and 5.0V (±10%) (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for Extended					
Param No.	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**	
	Internal FRC Jitter @ FRC Freq = 6.4 MHz(1)						
	FRC	-1	—	+1	%	+25°C	VDD = 3.0-3.6V
		-1	—	+1	%	+25°C	VDD = 4.5-5.5V
		-1	—	+1	%	-40°C ≤ TA ≤ +85°C	VDD = 3.0-3.6V
		-1	—	+1	%	-40°C ≤ TA ≤ +85°C	VDD = 4.5-5.5V
		-1	—	+1	%	-40°C ≤ TA ≤ +125°C	VDD = 4.5-5.5V
	Internal FRC Jitter @ FRC Freq = 9.7 MHz(1)						
	FRC	-1	—	+1	%	+25°C	VDD = 3.0-3.6V
		-1	—	+1	%	+25°C	VDD = 4.5-5.5V
		-1	—	+1	%	-40°C ≤ TA ≤ +85°C	VDD = 3.0-3.6V
		-1	—	+1	%	-40°C ≤ TA ≤ +85°C	VDD = 4.5-5.5V
		-1	—	+1	%	-40°C ≤ TA ≤ +125°C	VDD = 4.5-5.5V
	Internal FRC Jitter @ FRC Freq = 14.55 MHz(1)						
	FRC	-1	—	+1	%	+25°C	VDD = 3.0-3.6V
		-1	—	+1	%	+25°C	VDD = 4.5-5.5V
		-1	—	+1	%	-40°C ≤ TA ≤ +85°C	VDD = 3.0-3.6V
		-1	—	+1	%	-40°C ≤ TA ≤ +85°C	VDD = 4.5-5.5V
		-1	—	+1	%	-40°C ≤ TA ≤ +125°C	VDD = 4.5-5.5V

Note 1: Frequency calibrated at +25°C and 5V. TUN bits can be used to compensate for temperature drift.

FIGURE 21-14: SPIx MODULE SLAVE MODE (CKE = 0) TIMING CHARACTERISTICS

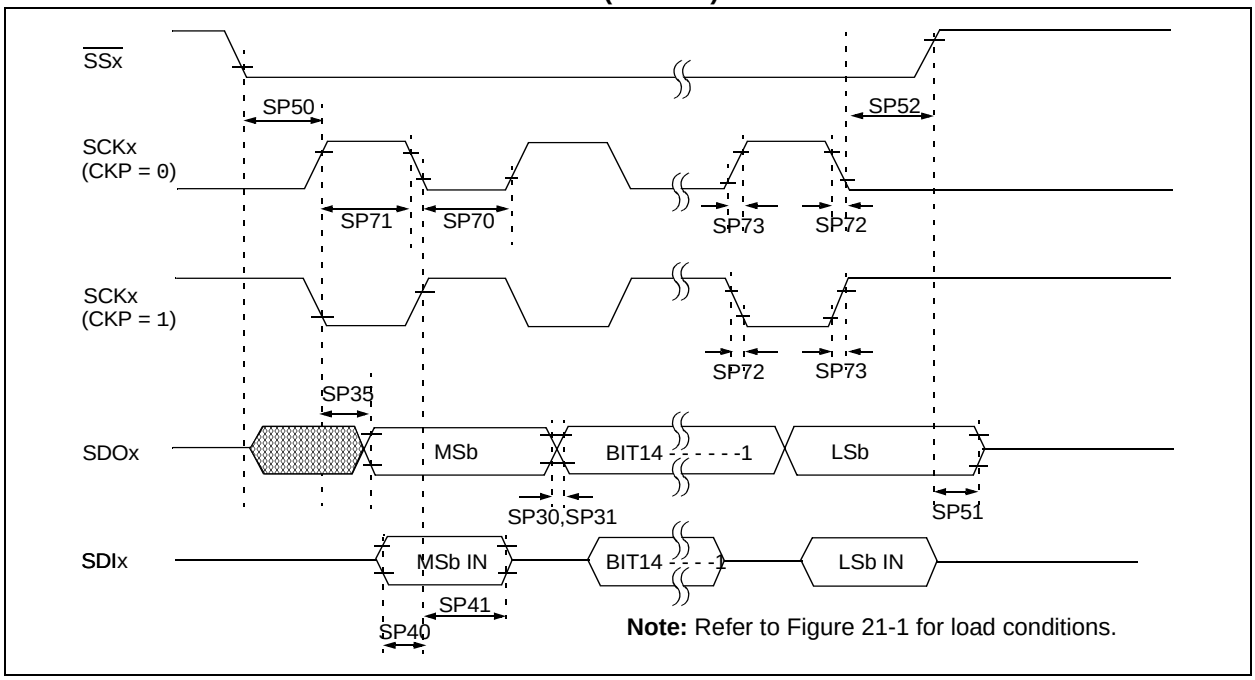


TABLE 21-29: SPIx MODULE SLAVE MODE (CKE = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.3V and 5.0V (±10%) (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic(1)**	**Min**	**Typ(2)**	**Max**	**Units**	**Conditions**
SP70	TscL	SCKx Input Low Time	30	—	—	ns	
SP71	TscH	SCKx Input High Time	30	—	—	ns	
SP72	TscF	SCKx Input Fall Time(3)	—	10	25	ns	
SP73	TscR	SCKx Input Rise Time(3)	—	10	25	ns	
SP30	TdoF	SDOx Data Output Fall Time(3)	—	—	—	ns	See Parameter D032
SP31	TdoR	SDOx Data Output Rise Time(3)	—	—	—	ns	See Parameter D031
SP35	TscH2doV TscL2doV	SDOx Data Output Valid after SCKx Edge	—	—	30	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	20	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	20	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SSx}$↓ to SCKx↑ or SCKx Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SSx}$↑ to SDOx Output High-Impedance(3)	10	—	50	ns	
SP52	TscH2ssH TscL2ssH	$\overline{SSx}$ after SCKx Edge	1.5 TCY + 40	—	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ" column is at 5V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: Assumes 50 pF load on all SPIx pins.

TABLE 21-31: I²C™ BUS DATA TIMING REQUIREMENTS (MASTER MODE)

AC CHARACTERISTICS				Standard Operating Conditions: 3.3V and 5.0V (±10%) (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Param No.	**Symbol**	**Characteristic**		**Min(1)**	**Max**	**Units**	**Conditions**
IM10	TLO:SCL	Clock Low Time	100 kHz mode	TCY/2 (BRG + 1)	—	µs	
			400 kHz mode	TCY/2 (BRG + 1)	—	µs	
			1 MHz mode(2)	TCY/2 (BRG + 1)	—	µs	
IM11	THI:SCL	Clock High Time	100 kHz mode	TCY/2 (BRG + 1)	—	µs	
			400 kHz mode	TCY/2 (BRG + 1)	—	µs	
			1 MHz mode(2)	TCY/2 (BRG + 1)	—	µs	
IM20	TF:SCL	SDA and SCL Fall Time	100 kHz mode	—	300	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode(2)	—	100	ns	
IM21	TR:SCL	SDA and SCL Rise Time	100 kHz mode	—	1000	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode(2)	—	300	ns	
IM25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	
			400 kHz mode	100	—	ns	
			1 MHz mode(2)	TBD	—	ns	
IM26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	ns	
			400 kHz mode	0	0.9	µs	
			1 MHz mode(2)	TBD	—	ns	
IM30	TSU:STA	Start Condition Setup Time	100 kHz mode	TCY/2 (BRG + 1)	—	µs	Only relevant for Repeated Start condition
			400 kHz mode	TCY/2 (BRG + 1)	—	µs	
			1 MHz mode(2)	TCY/2 (BRG + 1)	—	µs	
IM31	THD:STA	Start Condition Hold Time	100 kHz mode	TCY/2 (BRG + 1)	—	µs	After this period, the first clock pulse is generated
			400 kHz mode	TCY/2 (BRG + 1)	—	µs	
			1 MHz mode(2)	TCY/2 (BRG + 1)	—	µs	
IM33	TSU:STO	Stop Condition Setup Time	100 kHz mode	TCY/2 (BRG + 1)	—	µs	
			400 kHz mode	TCY/2 (BRG + 1)	—	µs	
			1 MHz mode(2)	TCY/2 (BRG + 1)	—	µs	
IM34	THD:STO	Stop Condition Hold Time	100 kHz mode	TCY/2 (BRG + 1)	—	ns	
			400 kHz mode	TCY/2 (BRG + 1)	—	ns	
			1 MHz mode(2)	TCY/2 (BRG + 1)	—	ns	
IM40	TAA:SCL	Output Valid from Clock	100 kHz mode	—	3500	ns	
			400 kHz mode	—	1000	ns	
			1 MHz mode(2)	—	—	ns	
IM45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	µs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	µs	
			1 MHz mode(2)	TBD	—	µs	
IM50	CB	Bus Capacitive Loading		—	400	pF	

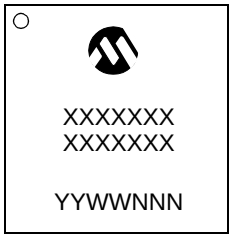
Legend: TBD = To Be Determined

Note 1: BRG is the value of the I²C™ Baud Rate Generator. Refer to the **"Inter-Integrated Circuit™ (I²C)"** section in the *"dsPIC30F Family Reference Manual"* (DS70046).

2: Maximum pin capacitance = 10 pF for all I²C pins (for 1 MHz mode only).

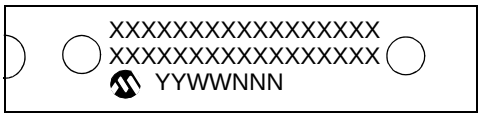
22.0 PACKAGE MARKING INFORMATION

28-Lead QFN-S

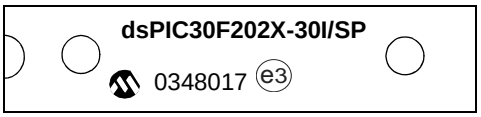


Example

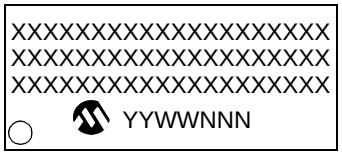
28-Lead PDIP (Skinny DIP)



Example

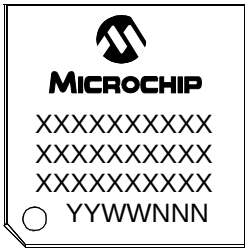


28-Lead SOIC

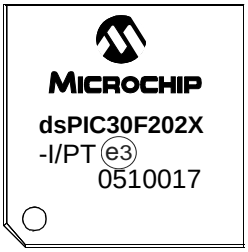


Example

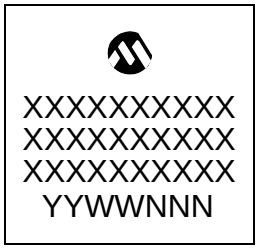
44-Lead TQFP



Example



44-Lead QFN



Example

Legend:	XX...X	Customer-specific information
	e3	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
		Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.