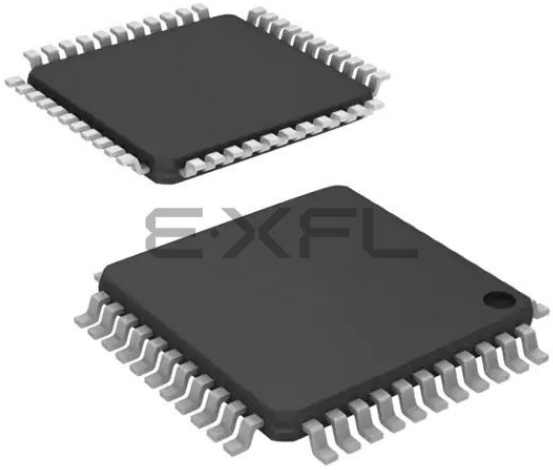

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | dsPIC |
| Core Size | 16-Bit |
| Speed | 30 MIPs |
| Connectivity | I²C, IrDA, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 35 |
| Program Memory Size | 12KB (4K x 24) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 512 x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 5.5V |
| Data Converters | A/D 12x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-TQFP |
| Supplier Device Package | 44-TQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/dspic30f2023t-30i-pt |

## Analog Features:

ADC

- 10-bit resolution
- 2000 Ksps conversion rate
- Up to 12 input channels
- “Conversion pairing” allows simultaneous conversion of two inputs (i.e., current and voltage) with a single trigger
- PWM control loop:
  - Up to six conversion pairs available
  - Each conversion pair has up to four PWM and seven other selectable trigger sources
- Interrupt hardware supports up to 1M interrupts per second

COMPARATOR

- Four Analog Comparators:
  - 20 ns response time
  - 10-bit DAC reference generator
  - Programmable output polarity
  - Selectable input source
  - ADC sample and convert capable
- PWM module interface
  - PWM Duty Cycle Control
  - PWM Period Control
  - PWM Fault Detect
- Special Event Trigger
- PWM-generated ADC Trigger

## Special Microcontroller Features:

- Enhanced Flash program memory:
  - 10,000 erase/write cycle (min.) for industrial temperature range, 100k (typical)
- Self-reprogrammable under software control
- Power-on Reset (POR), Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Flexible Watchdog Timer (WDT) with on-chip low power RC oscillator for reliable operation
- Fail-Safe clock monitor operation
- Detects clock failure and switches to on-chip low power RC oscillator
- Programmable code protection
- In-Circuit Serial Programming™ (ICSP™)
- Selectable Power Management modes
  - Sleep, Idle and Alternate Clock modes

## CMOS Technology:

- Low-power, high-speed Flash technology
- 3.3V and 5.0V operation (±10%)
- Industrial and Extended temperature ranges
- Low power consumption

**dsPIC30F SWITCH MODE POWER SUPPLY FAMILY**

| Product | Pins | Packaging | Program Memory (Bytes) | Data SRAM (Bytes) | Timers | Capture | Compare | UART | SPI | $I^2C$™ | PWM | ADCs | S & H | A/D Inputs | Analog Comparators | GPIO |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| dsPIC30F1010 | 28 | SDIP | 6K | 256 | 2 | 0 | 1 | 1 | 1 | 1 | 2x2 | 1 | 3 | 6 ch | 2 | 21 |
| dsPIC30F1010 | 28 | SOIC | 6K | 256 | 2 | 0 | 1 | 1 | 1 | 1 | 2x2 | 1 | 3 | 6 ch | 2 | 21 |
| dsPIC30F1010 | 28 | QFN-S | 6K | 256 | 2 | 0 | 1 | 1 | 1 | 1 | 2x2 | 1 | 3 | 6 ch | 2 | 21 |
| dsPIC30F2020 | 28 | SDIP | 12K | 512 | 3 | 1 | 2 | 1 | 1 | 1 | 4x2 | 1 | 5 | 8 ch | 4 | 21 |
| dsPIC30F2020 | 28 | SOIC | 12K | 512 | 3 | 1 | 2 | 1 | 1 | 1 | 4x2 | 1 | 5 | 8 ch | 4 | 21 |
| dsPIC30F2020 | 28 | QFN-S | 12K | 512 | 3 | 1 | 2 | 1 | 1 | 1 | 4x2 | 1 | 5 | 8 ch | 4 | 21 |
| dsPIC30F2023 | 44 | QFN | 12K | 512 | 3 | 1 | 2 | 1 | 1 | 1 | 4x2 | 1 | 5 | 12 ch | 4 | 35 |
| dsPIC30F2023 | 44 | TQFP | 12K | 512 | 3 | 1 | 2 | 1 | 1 | 1 | 4x2 | 1 | 5 | 12 ch | 4 | 35 |

**REGISTER 5-15: IPC6: INTERRUPT PRIORITY CONTROL REGISTER 6**

| U-0 | R/W-1 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | CNIP<2:0> | | | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **CNIP<2:0>:** Change Notification Interrupt Priority bits

111 = Interrupt is priority 7 (highest priority interrupt)

•

•

•

001 = Interrupt is priority 1

000 = Interrupt source is disabled

bit 11-0 **Unimplemented:** Read as ‘0’

## 6.0 I/O PORTS

**Note:** This data sheet summarizes features of this group of dsPIC30F devices and is not intended to be a complete reference source. For more information on the CPU, peripherals, register descriptions and general device functionality, refer to the "*dsPIC30F Family Reference Manual*" (DS70046).

All of the device pins (except VDD, VSS, $\overline{\text{MCLR}}$ and OSC1/CLKI) are shared between the peripherals and the parallel I/O ports.

All I/O input ports feature Schmitt Trigger inputs for improved noise immunity.

### 6.1 Parallel I/O (PIO) Ports

When a peripheral is enabled and the peripheral is actively driving an associated pin, the use of the pin as a general purpose output pin is disabled. The I/O pin may be read, but the output driver for the parallel port bit will be disabled. If a peripheral is enabled, but the peripheral is not actively driving a pin, that pin may be driven by a port.

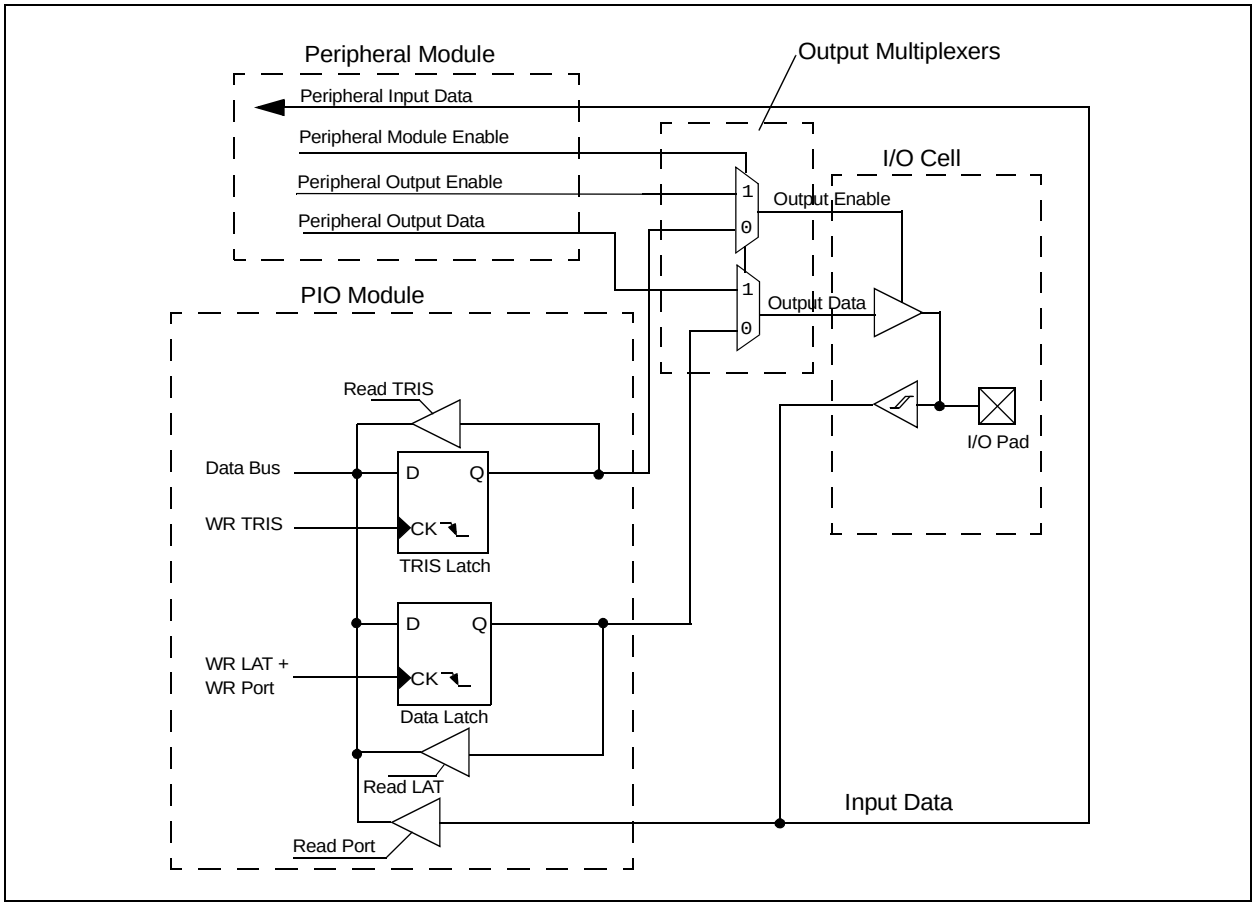
All port pins have three registers directly associated with the operation of the port pin. The data direction register (TRISx) determines whether the pin is an input or an output. If the data direction bit is a '1', then the pin is an input. All port pins are defined as inputs after a Reset. Reads from the latch (LATx), read the latch. Writes to the latch, write the latch (LATx). Reads from the port (PORTx), read the port pins, and writes to the port pins, write the latch (LATx).

Any bit and its associated data and control registers that are not valid for a particular device will be disabled. That means the corresponding LATx and TRISx registers and the port pin will read as zeros.

When a pin is shared with another peripheral or function that is defined as an input only, it is nevertheless regarded as a dedicated port because there is no other competing source of outputs.

A Parallel I/O (PIO) port that shares a pin with a peripheral is, in general, subservient to the peripheral. The peripheral's output buffer data and control signals are provided to a pair of multiplexers. The multiplexers select whether the peripheral or the associated port has ownership of the output data and control signals of the I/O pad cell. Figure 6-1 shows how ports are shared with other peripherals, and the associated I/O cell (pad) to which they are connected. Table 6-1 and Table 6-2 show the register formats for the shared ports, PORTA through PORTF, for the dsPIC30F1010/2020 and PORTA through PORTG for the dsPIC30F2023 device, respectively.

**FIGURE 6-1: BLOCK DIAGRAM OF A SHARED PORT STRUCTURE**



## 6.2 Configuring Analog Port Pins

The use of the ADPCFG and TRIS registers control the operation of the A/D port pins. The port pins that are desired as analog inputs must have their corresponding TRIS bit set (input). If the TRIS bit is cleared (output), the digital output level ($V_{OH}$ or $V_{OL}$) will be converted.

When reading the PORT register, all pins configured as analog input channel will read as cleared (a low level).

Pins configured as digital inputs will not convert an analog input. Analog levels on any pin that is defined as a digital input (including the ANx pins), may cause the input buffer to consume current that exceeds the device specifications.

### 6.2.1 I/O PORT WRITE/READ TIMING

One instruction cycle is required between a port direction change or port write operation and a read operation of the same port. Typically this instruction would be a NOP.

**EXAMPLE 6-1: PORT WRITE/READ EXAMPLE**

```
MOV 0xFF00, W0; Configure PORTB<15:8>
      ; as inputs
MOV W0, TRISBB; and PORTB<7:0> as outputs
NOP   ; Delay 1 cycle
BTSS PORTB, #13; Next Instruction
```

## 6.3 Input Change Notification

The input change notification function of the I/O ports allows the dsPIC30F1010/202X devices to generate interrupt requests to the processor in response to a change-of-state on selected input pins. This feature is capable of detecting input change-of-states even in Sleep mode, when the clocks are disabled. There are 8 external signals (CN0 through CN7) that can be selected (enabled) for generating an interrupt request on a change-of-state.

There are two control registers associated with the CN module. The CNEN1 register contain the CN interrupt enable (CNxIE) control bits for each of the CN input pins. Setting any of these bits enables a CN interrupt for the corresponding pins.

Each CN pin also has a weak pull-up connected to it. The pull-ups act as a current source that is connected to the pin and eliminate the need for external resistors when push button or keypad devices are connected. The pull-ups are enabled separately using the CNPU1 register, which contain the weak pull-up enable (CNxPUE) bits for each of the CN pins. Setting any of the control bits enables the weak pull-ups for the corresponding pins.

**Note:** Pull-ups on change notification pins should always be disabled whenever the port pin is configured as a digital output.

## 8.0 TIMER1 MODULE

**Note:** This data sheet summarizes features of this group of dsPIC30F devices and is not intended to be a complete reference source. For more information on the CPU, peripherals, register descriptions and general device functionality, refer to the "*dsPIC30F Family Reference Manual*" (DS70046).

This section describes the 16-bit General Purpose Timer1 module and associated operational modes. Figure 8-1 depicts the simplified block diagram of the 16-bit Timer1 Module.

**Note:** Timer1 is a 'Type A' timer. Please refer to the specifications for a Type A timer in **Section 21.0 "Electrical Characteristics"** of this document.

The following sections provide a detailed description of the operational modes of the timers, including setup and control registers along with associated block diagrams.

The Timer1 module is a 16-bit timer which can serve as the time counter for the real-time clock, or operate as a free running interval timer/counter. The 16-bit timer has the following modes:

- 16-bit Timer
- 16-bit Synchronous Counter
- 16-bit Asynchronous Counter

Further, the following operational characteristics are supported:

- Timer gate operation
- Selectable prescaler settings
- Timer operation during CPU Idle and Sleep modes
- Interrupt on 16-bit period register match or falling edge of external gate signal

These operating modes are determined by setting the appropriate bit(s) in the 16-bit SFR, T1CON. Figure 8-1 presents a block diagram of the 16-bit timer module.

**16-bit Timer Mode:** In the 16-bit Timer mode, the timer increments on every instruction cycle up to a match value, preloaded into the period register PR1, then resets to 0 and continues to count.

When the CPU goes into the Idle mode, the timer will stop incrementing, unless the TSIDL (T1CON<13>) bit = 0. If TSIDL = 1, the timer module logic will resume the incrementing sequence upon termination of the CPU Idle mode.

**16-bit Synchronous Counter Mode:** In the 16-bit Synchronous Counter mode, the timer increments on the rising edge of the applied external clock signal, which is synchronized with the internal phase clocks. The timer counts up to a match value preloaded in PR1, then resets to 0 and continues.

When the CPU goes into the Idle mode, the timer will stop incrementing, unless the respective TSIDL bit = 0. If TSIDL = 1, the timer module logic will resume the incrementing sequence upon termination of the CPU Idle mode.

**16-bit Asynchronous Counter Mode:** In the 16-bit Asynchronous Counter mode, the timer increments on every rising edge of the applied external clock signal. The timer counts up to a match value preloaded in PR1, then resets to '0' and continues.

When the timer is configured for the Asynchronous mode of operation and the CPU goes into the Idle mode, the timer will stop incrementing if TSIDL = 1.

## 10.1 Simple Capture Event Mode

The simple capture events in the dsPIC30F product family are:

- Capture every falling edge
- Capture every rising edge
- Capture every 4th rising edge
- Capture every 16th rising edge
- Capture every rising and falling edge

These simple Input Capture modes are configured by setting the appropriate bits ICM<2:0> (ICxCON<2:0>).

### 10.1.1 CAPTURE PRESCALER

There are four input capture prescaler settings, specified by bits ICM<2:0> (ICxCON<2:0>). Whenever the capture channel is turned off, the prescaler counter will be cleared. In addition, any Reset will clear the prescaler counter.

### 10.1.2 CAPTURE BUFFER OPERATION

Each capture channel has an associated FIFO buffer, which is four 16-bit words deep. There are two status flags, which provide status on the FIFO buffer:

- ICBFNE – Input Capture Buffer Not Empty
- ICOV – Input Capture Overflow

The ICBFNE will be set on the first input capture event and remain set until all capture events have been read from the FIFO. As each word is read from the FIFO, the remaining words are advanced by one position within the buffer.

In the event that the FIFO is full with four capture events and a fifth capture event occurs prior to a read of the FIFO, an Overflow condition will occur and the ICOV bit will be set to a logic ‘1’. The fifth capture event is lost and is not stored in the FIFO. No additional events will be captured until all four events have been read from the buffer.

If a FIFO read is performed after the last read and no new capture event has been received, the read will yield indeterminate results.

### 10.1.3 TIMER2 AND TIMER3 SELECTION MODE

The input capture module consists of up to 8 input capture channels. Each channel can select between one of two timers for the time base, Timer2 or Timer3.

Selection of the timer resource is accomplished through SFR bit ICTMR (ICxCON<7>). Timer3 is the default timer resource available for the input capture module.

### 10.1.4 HALL SENSOR MODE

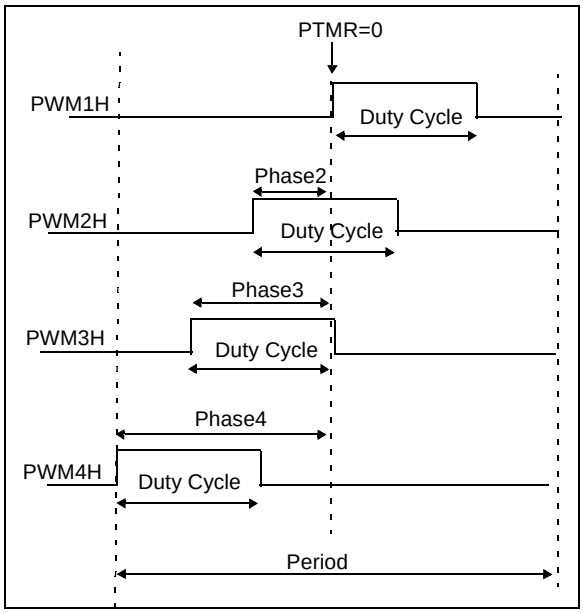
When the input capture module is set for capture on every edge, rising and falling, ICM<2:0> = 001, the following operations are performed by the input capture logic:

- The input capture interrupt flag is set on every edge, rising and falling.
- The Interrupt on Capture mode setting bits, ICI<1:0>, are ignored, since every capture generates an interrupt.
- A Capture Overflow condition is not generated in this mode.

### 12.4.4 MULTI-PHASE PWM MODE

Multi-Phase PWM, as shown in Figure 12-6, uses phase-shift values in the Phase registers to shift the PWM outputs relative to the primary time base. Because the phase-shift values are added to the primary time base, the phase-shifted outputs occur earlier than a PWM channel that specifies zero phase shift. In Multi-Phase mode, the specified phase shift is fixed by the application's design.

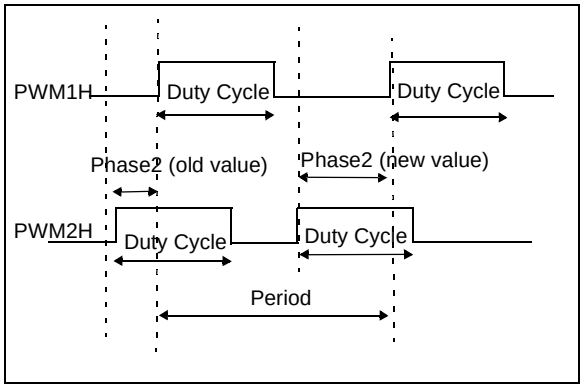
**FIGURE 12-6: MULTI-PHASE PWM**




### 12.4.5 VARIABLE PHASE PWM MODE

Figure 12-7 shows the waveforms for Variable Phase-Shift PWM. Power-converter circuits constantly change the phase shift among PWM channels as a means to control the flow of power, in contrast to most PWM circuits that vary the duty cycle of PWM signals to control power flow. Often, in variable phase applications, the PWM duty cycle is maintained at 50%. The phase-shift value should be updated when the PWM signal is not asserted. Complementary outputs are available in Variable Phase-Shift mode.

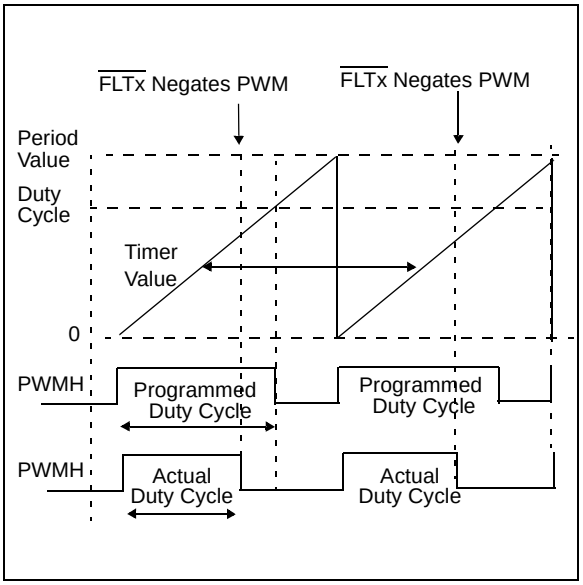
**FIGURE 12-7: VARIABLE PHASE PWM**




### 12.4.6 CURRENT-LIMIT PWM MODE

Figure 12-8 shows Cycle-by-Cycle Current-Limit mode. This mode truncates the asserted PWM signal when the selected external Fault signal is asserted. The PWM output values are specified by the Fault override bits (FLTDAT<1:0>) in the IOCONx register. The override output remains in effect until the beginning of the next PWM cycle. This mode is sometimes used in Power Factor Correction (PFC) circuits where the inductor current controls the PWM on time. This is a constant frequency PWM mode.

**FIGURE 12-8: CYCLE-BY-CYCLE CURRENT-LIMIT PWM MODE**



## 12.36 EXTERNAL SYNCHRONIZATION FEATURES

In large power conversion systems, it is often desirable to be able to synchronize multiple power controllers to ensure that “beat frequencies” are not generated within the system, or as a means to ensure “quiet” periods during which current and voltage measurements can be made.

dsPIC30F202X devices (excluding 28-pin packages) have input and/or output pins that provide the capability to either synchronize the SMPS dsPIC DSC device with an external device or have external devices synchronized to the SMPS dsPIC DSC. These synchronizing features are enabled via the SYNCIEN and SYNCOEN bits in the PTCON control register in the PWM module.

The SYNCPOL bit in the PTCON register selects whether the rising edge or the falling edge of the SYNCI signal is the active edge. The SYNCPOL bit in the PTCON register also selects whether the SYNCO output pulse is low active or high active.

The SYNCSRC<2:0> bits in the PTCON register specify the source for the SYNCI signal.

If the SYNCI feature is enabled, the primary time base counter is reset when an active SYNCI edge is detected. If the SYNCO feature is enabled, an output pulse is generated when the primary time base counter rolls over at the end of a PWM cycle.

The recommended SYNCI pulse width should be more than 100 nsec. The expected SYNCO output pulse width will be approximately 100 nsec.

When using the SYNCI feature, it is recommended that the user program the period register with a period value that is slightly longer than the expected period of the external synchronization input signal. This provides protection in case the SYNCI signal is not received due to noise or external component failure. With a reasonable period value programmed into the PTPER register, the local power conversion process should remain operational even if the global synchronization signal is not received.

## 12.37 CPU LOAD STAGGERING

The SMPS dsPIC DSC has the ability to stagger the individual trigger comparison operations. This feature helps to level the processor’s workload to minimize situations where the processor is overloaded.

Assume a situation where there are four PWM channels controlling four independent voltage outputs. Assume further that each PWM generator is operating at 1000 kHz (1 µsec period) and each control loop is operating at 125 kHz (8 µsec).

The TRGDIV<2:0> bits in each TRGCONx register will be set to ‘111’, which selects that every 8th trigger comparison match will generate a trigger signal to the ADC to capture data and begin a conversion process.

If the stagger-in-time feature did not exist, all of the requests from all of the PWM trigger registers might occur at the same time. If this “pile-up” were to happen, some data sample might become stale (outdated) by the time the data for all four channels can be processed.

With the stagger-in-time feature, the trigger signals are spaced out over time (during succeeding PWM periods) so that all of the data is processed in an orderly manner.

The ROLL counter is a counter connected to the primary time base counter. The ROLL counter is incremented each time the primary time base counter reaches terminal count (period rollover).

The stagger-in-time feature is controlled by the TRGSTRT<5:0> bits in the TRGCONx registers. The TRGSTRT<5:0> bits specify the count value of the ROLL counter that must be matched before an individual trigger comparison module in each of the PWM generators can begin to count the trigger comparison events as specified by the TRGDIV<2:0> bits in the PWMCONx registers.

So, in our example with the four PWM generators, the first PWM’s TRGSTRT<5:0> bits would be ‘000’, the second PWM’s TRGSTRT bits would be set to ‘010’, the third PWM’s TRGSTRT bits would be set to ‘100’ and the fourth PWM’s TRGSTRT bits would be set to ‘110’. Therefore, over a total of eight PWM cycles, the four separate control loops could be run each with their own 2-µsec time period.

## 12.38 EXTERNAL TRIGGER BLANKING

Using the LEB<9:3> bits in the LEBCONx registers, the PWM module has the capability to blank (ignore) the external current and Fault inputs for a period of 0 to 1024 nsec. This feature is useful if power transistor turn-on induced transients make current sensing difficult at the start of a PWM cycle.

**REGISTER 15-2: U1STA: UART1 STATUS AND CONTROL REGISTER (CONTINUED)**

bit 4 **RIDLE:** Receiver Idle bit (Read-Only)

1 = Receiver is Idle
0 = Receiver is active

bit 3 **PERR:** Parity Error Status bit (Read-Only)

1 = Parity error has been detected for the current character (character at the top of the receive FIFO)
0 = Parity error has not been detected

bit 2 **FERR:** Framing Error Status bit (Read-Only)

1 = Framing error has been detected for the current character (character at the top of the receive FIFO)
0 = Framing error has not been detected

bit 1 **OERR:** Receive Buffer Overrun Error Status bit (Read/Clear-Only)

1 = Receive buffer has overflowed
0 = Receive buffer has not overflowed (clearing a previously set OERR bit (1 → 0 transition) will reset the receiver buffer and the RSR to the empty state)

bit 0 **URXDA:** Receive Buffer Data Available bit (Read-Only)

1 = Receive buffer has data, at least one more character can be read
0 = Receive buffer is empty

**REGISTER 16-1: A/D CONTROL REGISTER (ADCON) (CONTINUED)**

bit 2-0 **ADCS<2:0>:** A/D Conversion Clock Divider Select bits

If PLL is enabled (assume 15 MHz external clock as clock source):
111 = FADC/18 = 13.3 MHz @ 30 MIPS
110 = FADC/16 = 15.0 MHz @ 30 MIPS
101 = FADC/14 = 17.1 MHz @ 30 MIPS
100 = FADC/12 = 20.0 MHz @ 30 MIPS
011 = FADC/10 = 24.0 MHz @ 30 MIPS
010 = FADC/8 = 30.0 MHz @ 30 MIPS
001 = FADC/6 = Reserved, defaults to 30 MHz @ 30 MIPS
000 = FADC/4 = Reserved, defaults to 30 MHz @ 30 MIPS

If PLL is disabled (assume 15 MHz external clock as clock source):
111 = FADC/18 = 0.83 MHz @ 7.5 MIPS
110 = FADC/16 = 0.93 MHz @ 7.5 MIPS
101 = FADC/14 = 1.07 MHz @ 7.5 MIPS
100 = FADC/12 = 1.25 MHz @ 7.5 MIPS
011 = FADC/10 = 1.5 MHz @ 7.5 MIPS
010 = FADC/8 = 1.87 MHz @ 7.5 MIPS
001 = FADC/6 = 2.5 MHz @ 7.5 MIPS
000 = FADC/4 = 3.75 MHz @ 7.5 MIPS

**Note:** See Figure 18-2 for ADC clock derivation.

**EXAMPLE 16-1: ADC BASE REGISTER CODE (CONTINUED)**

```
; The actual pair conversion interrupt handler
; Don't forget to pop the stack when done and return from interrupt

ADC_PAIR0_PROC:

    ...                     ; The ADC pair 0 conversion complete handler
    POP.S                   ; Restore W0-W3 and SR registers
    RETFIE                  ; Return from Interrupt

ADC_PAIR1_PROC:

    ...                     ; The ADC pair 1 conversion complete handler
    POP.S                   ; Restore W0-W3 and SR registers
    RETFIE                  ; Return from Interrupt

ADC_PAIR2_PROC:

    ...                     ; The ADC pair 2 conversion complete handler
    POP.S                   ; Restore W0-W3 and SR registers
    RETFIE                  ; Return from Interrupt

ADC_PAIR3_PROC:

    ...                     ; The ADC pair 3 conversion complete handler
    POP.S                   ; Restore W0-W3 and SR registers
    RETFIE                  ; Return from Interrupt

ADC_PAIR4_PROC:

    ...                     ; The ADC pair 4 conversion complete handler
    POP.S                   ; Restore W0-W3 and SR registers
    RETFIE                  ; Return from Interrupt

ADC_PAIR5_PROC:

    ...                     ; The ADC pair 5 conversion complete handler
    POP.S                   ; Restore W0-W3 and SR registers
    RETFIE                  ; Return from Interrupt
```

## 16.15 Changing A/D Clock

In general, the ADC cannot accept changes to the ADC clock divisor while ADON = 1. If the user makes A/D clock changes while ADON = 1, the results will be indeterminate.

## 16.16 Sample and Conversion

The ADC module always assigns two ADC clock periods for the sampling process. When operating at the maximum conversion rate of 2 Msps per channel, the sampling period is:

2 x 41.6 nsec = 83.3 nsec.

Each ADC pair specified in the ADCPCx registers initiates a sample operation when the selected trigger event occurs. The conversion of the sampled analog data occurs as resources become available.

If a new trigger event occurs for a specific channel before a previous sample and convert request for that channel has been processed, the newer request is ignored. It is the user's responsibility not to exceed the conversion rate capability for the module.

The actual conversion process requires 10 additional ADC clocks. The conversion is processed serially, bit 9 first, then bit 8, down to bit 0. The result is stored when the conversion is completed.

**TABLE 17-1: ANALOG COMPARATOR CONTROL REGISTER MAP**

| File Name | ADR | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CMPCON1 | 04C0 | CMPON | — | CMPSIDL | — | — | — | — | — | INSEL<1:0> | | EXTREF | — | CMPSTAT | — | CMPPOL | RANGE | 0000 |
| CMPDAC1 | 04C2 | — | — | — | — | — | — | CMREF<9:0> | | | | | | | | | | 0000 |
| CMPCON2 | 04C4 | CMPON | — | CMPSIDL | — | — | — | — | — | INSEL<1:0> | | EXTREF | — | CMPSTAT | — | CMPPOL | RANGE | 0000 |
| CMPDAC2 | 04C6 | — | — | — | — | — | — | CMREF<9:0> | | | | | | | | | | 0000 |
| CMPCON3 | 04C8 | CMPON | — | CMPSIDL | — | — | — | — | — | INSEL<1:0> | | EXTREF | — | CMPSTAT | — | CMPPOL | RANGE | 0000 |
| CMPDAC3 | 04CA | — | — | — | — | — | — | CMREF<9:0> | | | | | | | | | | 0000 |
| CMPCON4 | 04CC | CMPON | — | CMPSIDL | — | — | — | — | — | INSEL<1:0> | | EXTREF | — | CMPSTAT | — | CMPPOL | RANGE | 0000 |
| CMPDAC4 | 04CE | — | — | — | — | — | — | CMREF<9:0> | | | | | | | | | | 0000 |

**REGISTER 18-6: FOSC: OSCILLATOR SELECTION CONFIGURATION BITS**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 23 | | | | | | | bit 16 |

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/P | R/P | R/P | U-0 | U-0 | R/P | R/P | R/P |
|---|---|---|---|---|---|---|---|
| FCKSM<1:0> | | FRANGE | — | — | OSCIOFNC | POSCMD<1:0> | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 23-8 **Unimplemented:** Read as ‘0’

bit 7-6 **FCKSM<1:0>:** Clock Switching and Monitor Selection Configuration bits

1x = Clock switching is disabled, fail-safe clock monitor is disabled
01 = Clock switching is enabled, fail-safe clock monitor is disabled
00 = Clock switching is enabled, fail-safe clock monitor is enabled

bit 5 **FRANGE:** Frequency Range Select for FRC and PLL bit
Acts like a “Gear Shift” feature that enables the dsPIC DSC device to operate at reduced MIPS at a reduced supply voltage (3.3V)

| FRANGE Bit Value | Temperature Rating | FRC Frequency (Nominal) | PLL VCO (Nominal) |
|---|---|---|---|
| 1 = High Range | Industrial<br>Extended | 14.55 MHz<br>9.7 MHz | 466 MHz (480 MHz max.)<br>310 MHz (320 MHz max.) |
| 0 = Low Range | Industrial<br>Extended | 9.7 MHz<br>6.4 MHz | 310 MHz (320 MHz max.)<br>205 MHz (211 MHz max.) |

bit 4-3 **Unimplemented:** Read as ‘0’

bit 3 **OSCIOFNC:** OSC2 Pin I/O Enable bit

1 = CLKO output signal active on the OSCO pin
0 = CLKO output disabled

bit 1-0 **POSCMD<1:0>:** Primary Oscillator Mode

11 = Primary Oscillator Disabled
10 = HS oscillator mode selected
01 = Reserved
00 = External clock mode selected

**TABLE 21-8: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.3V and 5.0V (±10%) (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ(1)** | **Max** | **Units** | **Conditions** |
| | VIL | **Input Low Voltage(2)** | | | | | |
| DI10 | | I/O Pins:<br>with Schmitt Trigger Buffer | VSS | — | 0.2 VDD | V | |
| DI15 | | $\overline{MCLR}$ | VSS | — | 0.2 VDD | V | |
| DI16 | | OSC1 (in HS mode) | VSS | — | 0.2 VDD | V | |
| DI18 | | SDA, SCL | VSS | — | 0.3 VDD | V | SMbus disabled |
| DI19 | | SDA, SCL | VSS | — | 0.2 VDD | V | SMbus enabled |
| | VIH | **Input High Voltage(2)** | | | | | |
| DI20 | | I/O Pins:<br>with Schmitt Trigger Buffer | 0.8 VDD | — | VDD | V | |
| DI25 | | $\overline{MCLR}$ | 0.8 VDD | — | VDD | V | |
| DI26 | | OSC1 (in HS mode) | 0.7 VDD | — | VDD | V | |
| DI28 | | SDA, SCL | 0.7 VDD | — | VDD | V | SMbus disabled |
| DI29 | | SDA, SCL | 0.8 VDD | — | VDD | V | SMbus enabled |
| | IIL | **Input Leakage Current(2,3,4)** | | | | | |
| DI50 | | I/O Ports | — | 0.01 | ±1 | μA | VSS ≤ VPIN ≤ VDD,<br>Pin at high-impedance |
| DI51 | | Analog Input Pins | — | 0.50 | — | μA | VSS ≤ VPIN ≤ VDD,<br>Pin at high-impedance |
| DI55 | | $\overline{MCLR}$ | — | 0.05 | ±5 | μA | VSS ≤ VPIN ≤ VDD |
| DI56 | | OSC1 | — | 0.05 | ±5 | μA | VSS ≤ VPIN ≤ VDD,<br>HS Oscillator mode |

**Note 1:** Data in "Typ" column is at 5V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**2:** These parameters are characterized but not tested in manufacturing.

**3:** The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

**4:** Negative current is defined as current sourced by the pin.

**TABLE 21-18: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER AND TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.3V and 5.0V (±10%) (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic(1)** | **Min** | **Typ(2)** | **Max** | **Units** | **Conditions** |
| SY10 | TMCL | $\overline{\text{MCLR}}$ Pulse Width (low) | 2 | — | — | μs | -40°C to +125°C |
| SY11 | TPWRT | Power-up Timer Period | 0.75<br>1.5<br>3<br>6<br>12<br>24<br>48<br>96 | 1<br>2<br>4<br>8<br>16<br>32<br>64<br>128 | 1.25<br>2.5<br>5<br>10<br>20<br>40<br>80<br>160 | ms | -40°C to +125°C, user programmable |
| SY12 | TPOR | Power-on Reset Delay | 3 | 10 | 30 | μs | -40°C to +125°C |
| SY13 | TIOZ | I/O High-impedance from $\overline{\text{MCLR}}$ Low or Watchdog Timer Reset | — | 0.8 | 1.0 | μs | |
| SY20 | TWDT1<br><br>TWDT2 | Watchdog Timer Time-out Period (No Prescaler) | 1.4<br><br>1.4 | 2.1<br><br>2.1 | 2.8<br><br>2.8 | ms<br><br>ms | VDD = 5V, -40°C to +125°C<br>VDD = 3.3V, -40°C to +125°C |
| SY30 | TOST | Oscillation Start-up Timer Period | — | 1024 TOSC | — | — | TOSC = OSC1 period |
| SY35 | TFSCM | Fail-Safe Clock Monitor Delay | — | 500 | — | μs | -40°C to +125°C |

**Note 1:** These parameters are characterized but not tested in manufacturing.

**2:** Data in "Typ" column is at 5V, +25°C unless otherwise stated.

**TABLE 21-21: TIMER2 EXTERNAL CLOCK TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | | Standard Operating Conditions: 3.3V and 5.0V (±10%) (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | | **Min** | **Typ** | **Max** | **Units** | **Conditions** |
| TB10 | TTXH | T2CK High Time | Synchronous, no prescaler | 0.5 TCY + 20 | — | — | ns | Must also meet Parameter TB15 |
| | | | Synchronous, with prescaler | 10 | — | — | ns | |
| TB11 | TTXL | T2CK Low Time | Synchronous, no prescaler | 0.5 TCY + 20 | — | — | ns | Must also meet Parameter TB15 |
| | | | Synchronous, with prescaler | 10 | — | — | ns | |
| TB15 | TTXP | T2CK Input Period | Synchronous, no prescaler | TCY + 10 | — | — | ns | N = Prescale value (1, 8, 64, 256) |
| | | | Synchronous, with prescaler | Greater of: 20 ns or (TCY + 40)/N | — | — | — | |
| TB20 | TCKEXTMRL | Delay from External T2CK Clock Edge to Timer Increment | | 0.5 TCY | — | 1.5 TCY | — | |

**TABLE 21-22: TIMER3 EXTERNAL CLOCK TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | | Standard Operating Conditions: 3.3V and 5.0V (±10%) (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | | **Min** | **Typ** | **Max** | **Units** | **Conditions** |
| TC10 | TTXH | T3CK High Time | Synchronous | 0.5 TCY + 20 | — | — | ns | Must also meet Parameter TC15 |
| TC11 | TTXL | T3CK Low Time | Synchronous | 0.5 TCY + 20 | — | — | ns | Must also meet Parameter TC15 |
| TC15 | TTXP | T3CK Input Period | Synchronous, no prescaler | TCY + 10 | — | — | ns | N = Prescale value (1, 8, 64, 256) |
| | | | Synchronous, with prescaler | Greater of: 20 ns or (TCY + 40)/N | — | — | — | |
| TC20 | TCKEXTMRL | Delay from External T3CK Clock Edge to Timer Increment | | 0.5 TCY | — | 1.5 TCY | — | |

**FIGURE 21-9: OCx/PWM MODULE TIMING CHARACTERISTICS**

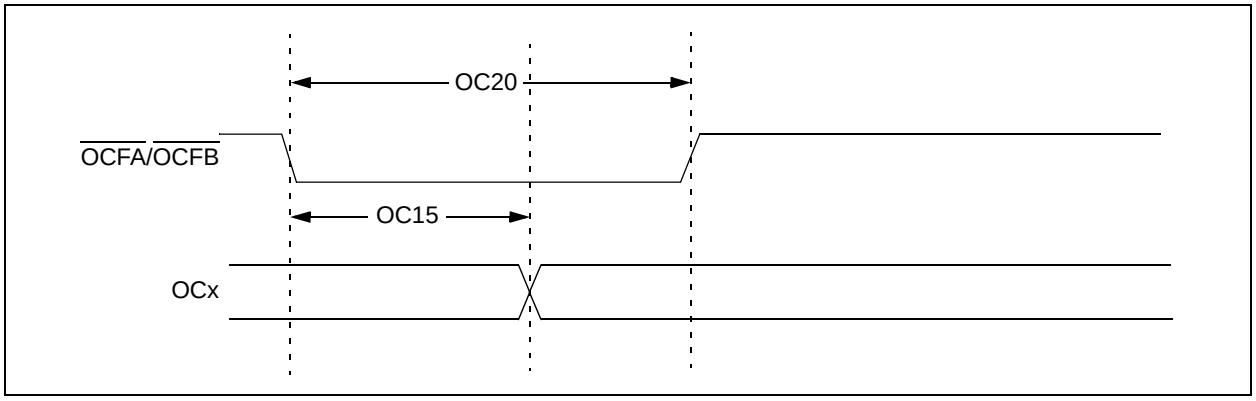



**TABLE 21-25: SIMPLE OCx/PWM MODE TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | | Standard Operating Conditions: 3.3V and 5.0V (±10%) (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic(1)** | **Min** | **Typ(2)** | **Max** | **Units** | **Conditions** | |
| OC15 | TFD | Fault Input to PWM I/O Change | — | — | 25 | ns | VDD = 3.3V | -40°C to +85°C |
| | | | | | TBD | ns | VDD = 5V | |
| OC20 | TFLT | Fault Input Pulse Width | — | — | 50 | ns | VDD = 3.3V | -40°C to +85°C |
| | | | | | TBD | ns | VDD = 5V | |

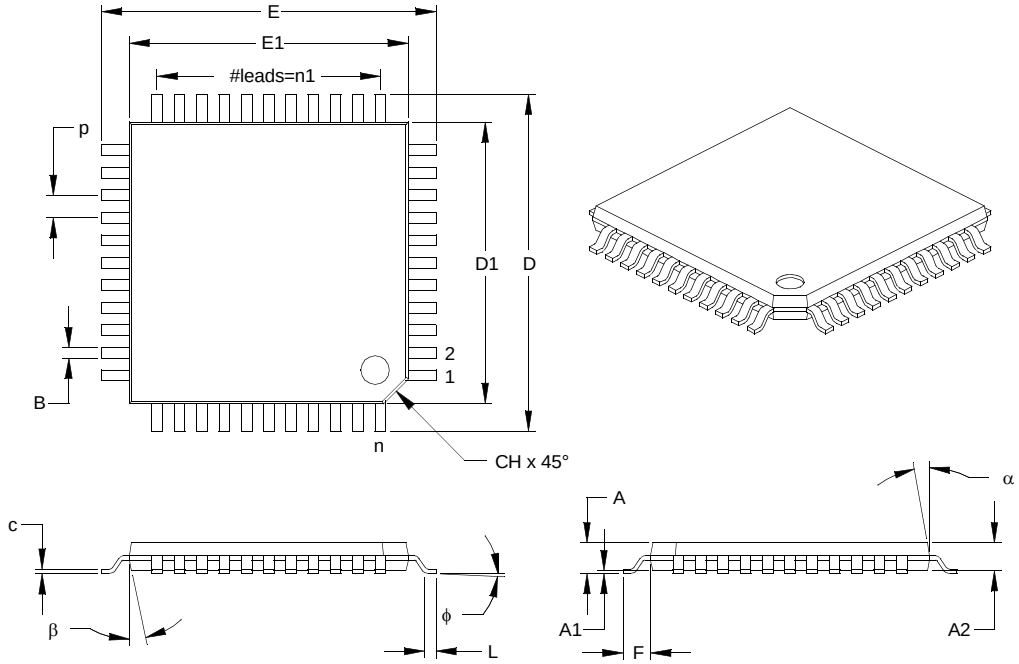
**Legend:** TBD = To Be Determined

**Note 1:** These parameters are characterized but not tested in manufacturing.

**2:** Data in “Typ” column is at 5V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

## 44-Lead Plastic Thin Quad Flatpack (PT) 10x10x1 mm Body, 1.0/0.10 mm Lead Form (TQFP)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | INCHES | | | MILLIMETERS* | | |
|---|---|---|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX | MIN | NOM | MAX |
| Number of Pins | n | | 44 | | | 44 | |
| Pitch | p | | .031 | | | 0.80 | |
| Pins per Side | n1 | | 11 | | | 11 | |
| Overall Height | A | .039 | .043 | .047 | 1.00 | 1.10 | 1.20 |
| Molded Package Thickness | A2 | .037 | .039 | .041 | 0.95 | 1.00 | 1.05 |
| Standoff | A1 | .002 | .004 | .006 | 0.05 | 0.10 | 0.15 |
| Foot Length | L | .018 | .024 | .030 | 0.45 | 0.60 | 0.75 |
| Footprint (Reference) | F | | .039 REF. | | | 1.00 REF. | |
| Foot Angle | ϕ | 0 | 3.5 | 7 | 0 | 3.5 | 7 |
| Overall Width | E | .463 | .472 | .482 | 11.75 | 12.00 | 12.25 |
| Overall Length | D | .463 | .472 | .482 | 11.75 | 12.00 | 12.25 |
| Molded Package Width | E1 | .390 | .394 | .398 | 9.90 | 10.00 | 10.10 |
| Molded Package Length | D1 | .390 | .394 | .398 | 9.90 | 10.00 | 10.10 |
| Lead Thickness | c | .004 | .006 | .008 | 0.09 | 0.15 | 0.20 |
| Lead Width | B | .012 | .015 | .017 | 0.30 | 0.38 | 0.44 |
| Pin 1 Corner Chamfer | CH | .025 | .035 | .045 | 0.64 | 0.89 | 1.14 |
| Mold Draft Angle Top | α | 5 | 10 | 15 | 5 | 10 | 15 |
| Mold Draft Angle Bottom | β | 5 | 10 | 15 | 5 | 10 | 15 |

***** Controlling Parameter

**Notes:**

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

REF: Reference Dimension, usually without tolerance, for information purposes only.

See ASME Y14.5M

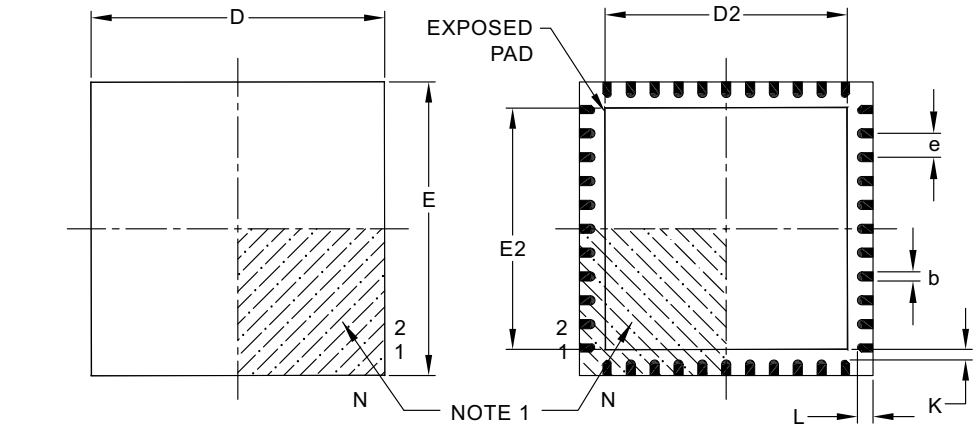
JEDEC Equivalent: MS-026

Drawing No. C04-076

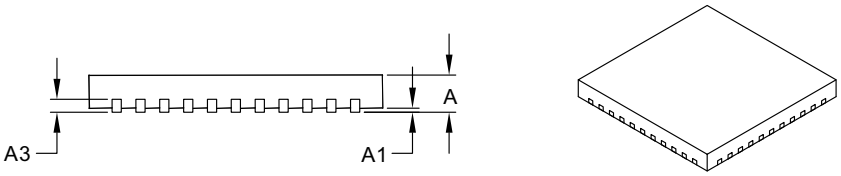
Revised 07-22-05

### 44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body (QFN)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




**TOP VIEW** **BOTTOM VIEW**




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 44 | |
| Pitch | e | | 0.65 BSC | |
| Overall Height | A | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Contact Thickness | A3 | | 0.20 REF | |
| Overall Width | E | | 8.00 BSC | |
| Exposed Pad Width | E2 | 6.30 | 6.45 | 6.80 |
| Overall Length | D | | 8.00 BSC | |
| Exposed Pad Length | D2 | 6.30 | 6.45 | 6.80 |
| Contact Width | b | 0.25 | 0.30 | 0.38 |
| Contact Length § | L | 0.30 | 0.40 | 0.50 |
| Contact-to-Exposed Pad § | K | 0.20 | — | — |

**Notes:**
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

□ □ □ □ Microchip Technology Drawing No. C04–103, Sept. 8, 2006

**NOTES:**