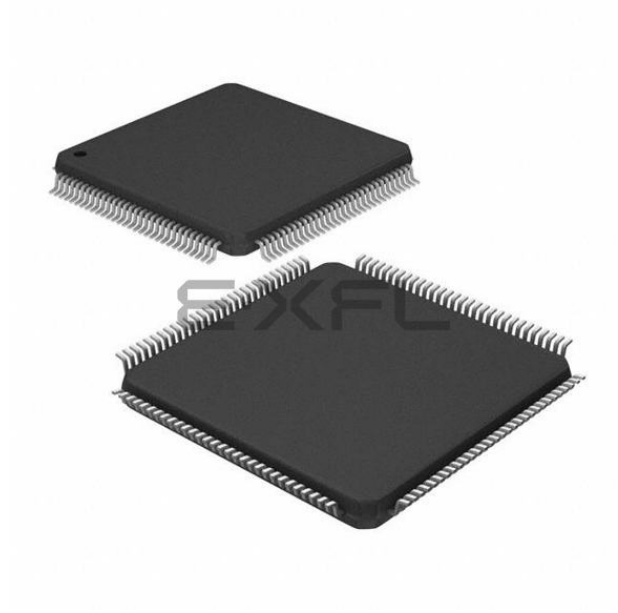
Renesas Electronics America Inc - R4F24545NVFPV Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8S/2600
Core Size	16-Bit
Speed	32MHz
Connectivity	EBI/EMI, I²C, IrDA, SCI, SSU, UART/USART, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	83
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b; D/A 2x8b
Oscillator Type	External
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP
Supplier Device Package	120-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r4f24545nvfpv

		Pin No.				
		H8S/2456, H8S/2456R		H8S/2454		
Type	Symbol	PLQP0144KA-A	PTLG0145JB-A	PLQP0120LA-A, PLQP0120KA-A	I/O	Function
A/D converter, D/A converter	AV_{CC}	111	B11	93	Input	Analog power-supply pin for the A/D converter and D/A converter. When the A/D converter and D/A converter are not used, this pin should be connected to the system power supply (V_{CC}).
	AV_{SS}	129	A7	105	Input	Ground pin for the A/D converter and D/A converter. This pin should be connected to the system power supply (V_{SS}).
	Vref	112	B12	94	Input	Reference voltage input pin for the A/D converter and D/A converter. When the A/D converter and D/A converter are not used, this pin should be connected to the system power supply (V_{CC}).
I/O ports	P17 to P10	49 to 42	L5, K6, K5, N4, M5, L4, M4, N3	41 to 34	Input/ output	8-bit input/output pins.
	P27 to P25 P20	58 to 56 51	K7, L8, N7, L6	49 to 47 42	Input/ output	4-bit input/output pins.
	P35 to P30	137 to 142	A5, B4, C5, A4, B3, C4	113 to 118	Input/ output	6-bit input/output pins.
	P47 to P40	120 to 113	B8, C9, B9, A10, C10, B10, C11, A11	102 to 95	Input	8-bit input pins.
	P53 to P50	136 to 133	D4, C6, B5, A6	112 to 109	Input/ output	4-bit input/output pins.
	P65 to P60	106 to 104, 83 to 81	C13, D12, D10, J10, K13, J12	—	Input/ output	6-bit input/output pins.
	P85	61	M8	50	Input/ output	6-bit input/output pins in the H8S/2456 Group and H8S/2456R Group. 3-bit input/output pins in the H8S/2454 Group.
	P84*2	60	N8	—		
	P83	59	K8	85		
	P82*2	34	K3	—		
	P81	33	L2	86		
	P80*2	3	C2	—		

Bit	Bit Name	Initial Value	R/W	Description
9	IRQ4SCB	0	R/W	IRQ4 Sense Control B
8	IRQ4SCA	0	R/W	IRQ4 Sense Control A 00: Interrupt request generated at $\overline{\text{IRQ4}}$ input low level 01: Interrupt request generated at falling edge of $\overline{\text{IRQ4}}$ input 10: Interrupt request generated at rising edge of $\overline{\text{IRQ4}}$ input 11: Interrupt request generated at both falling and rising edges of $\overline{\text{IRQ4}}$ input
7	IRQ3SCB	0	R/W	IRQ3 Sense Control B
6	IRQ3SCA	0	R/W	IRQ3 Sense Control A 00: Interrupt request generated at $\overline{\text{IRQ3}}$ input low level 01: Interrupt request generated at falling edge of $\overline{\text{IRQ3}}$ input 10: Interrupt request generated at rising edge of $\overline{\text{IRQ3}}$ input 11: Interrupt request generated at both falling and rising edges of $\overline{\text{IRQ3}}$ input
5	IRQ2SCB	0	R/W	IRQ2 Sense Control B
4	IRQ2SCA	0	R/W	IRQ2 Sense Control A 00: Interrupt request generated at $\overline{\text{IRQ2}}$ input low level 01: Interrupt request generated at falling edge of $\overline{\text{IRQ2}}$ input 10: Interrupt request generated at rising edge of $\overline{\text{IRQ2}}$ input 11: Interrupt request generated at both falling and rising edges of $\overline{\text{IRQ2}}$ input

5.7.6 IRQ Status Register (ISR)

Depending on the pin status following a reset, IRQnF may be set to 1. Therefore, always read ISR and clear it to 0 after resets.

6.5.3 Basic Timing

(1) 8-Bit, 2-State Access Space

Figure 6.10 shows the bus timing for an 8-bit, 2-state access space. When an 8-bit access space is accessed, the upper half (D15 to D8) of the data bus is used. The $\overline{\text{LWR}}$ pin is always fixed high. Wait states can be inserted.

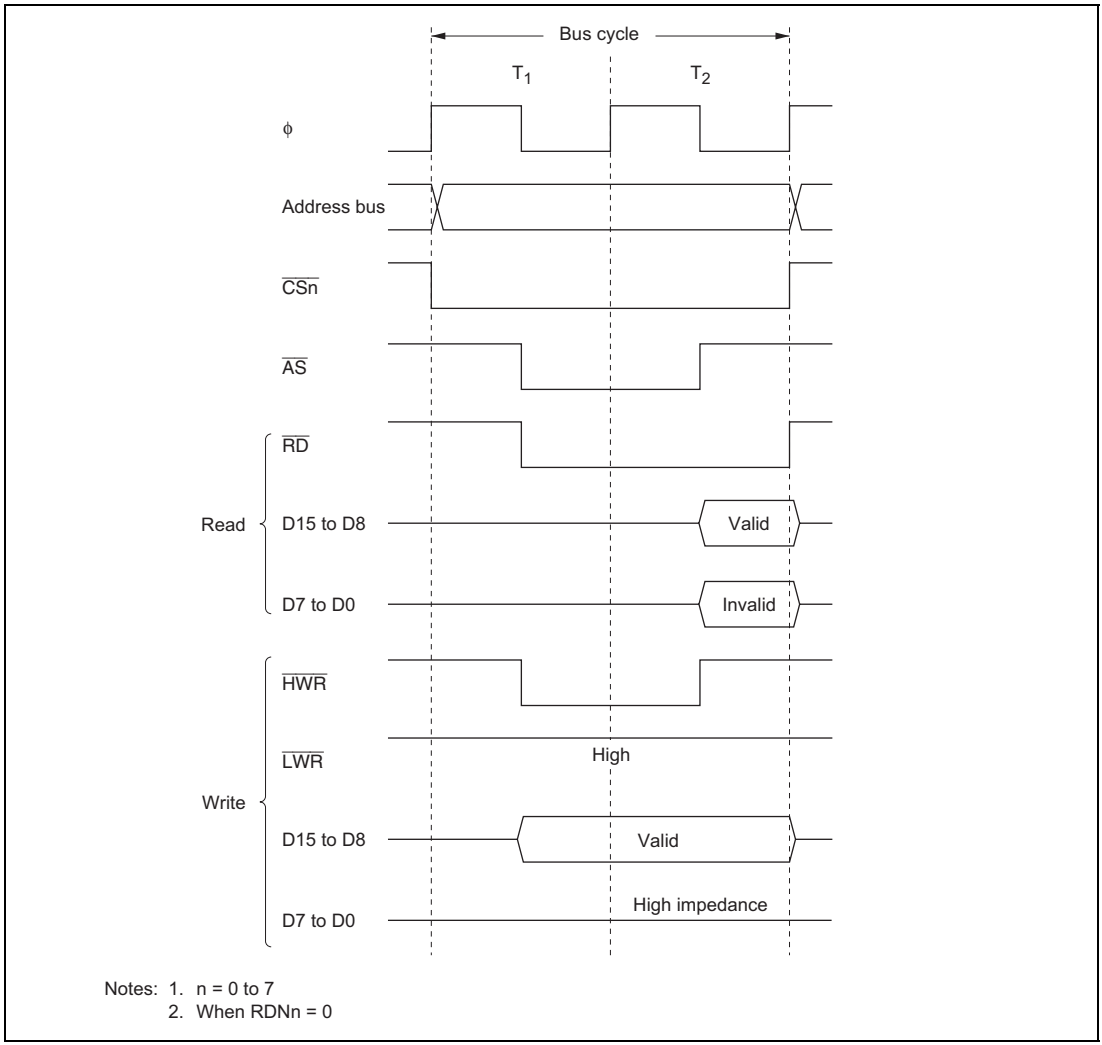


Figure 6.10 Bus Timing for 8-Bit, 2-State Access Space

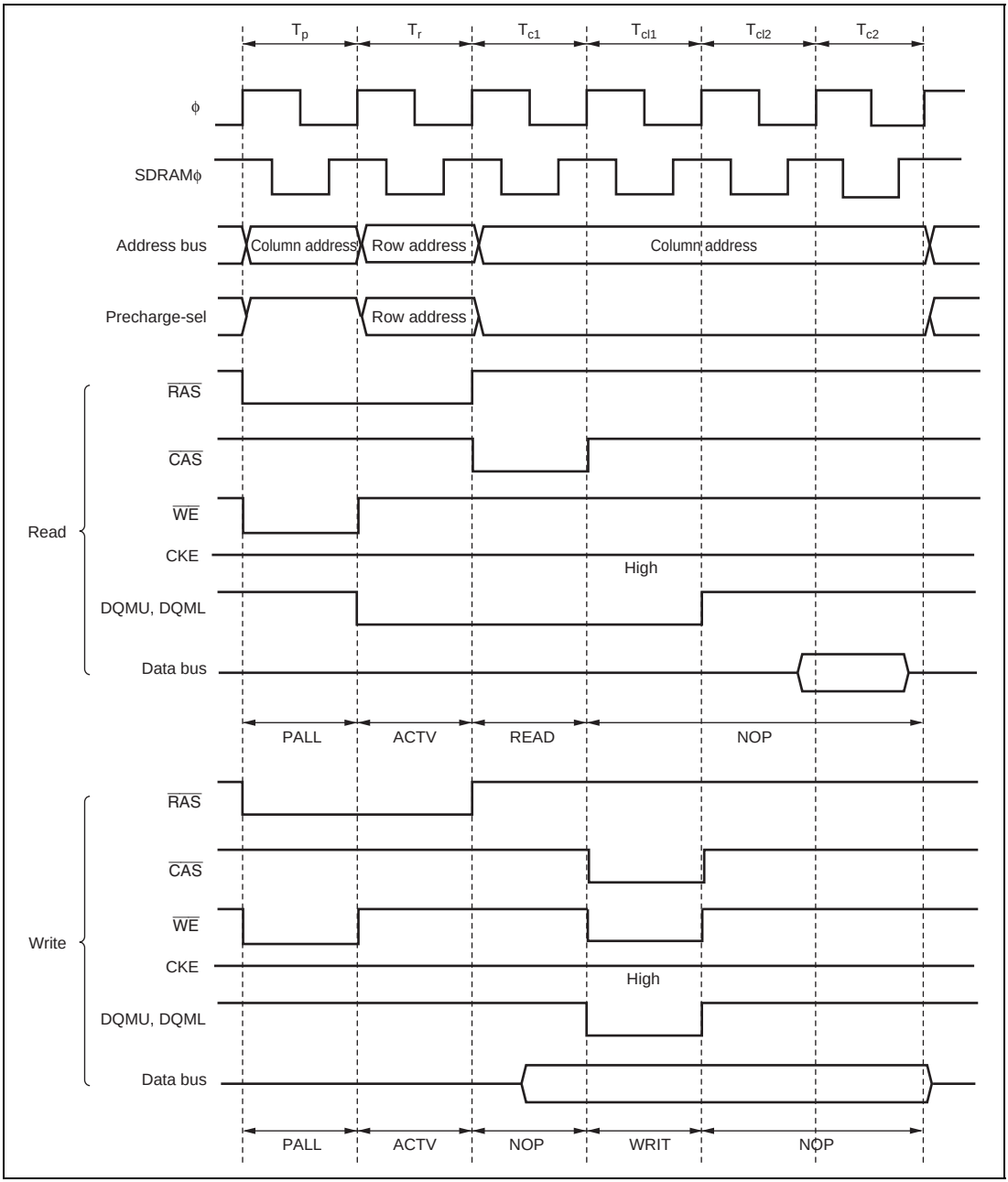


Figure 6.57 CAS Latency Control Timing (SDWCD = 0, CAS Latency 3)

Table 22.2 Overview of Flash Memory Programming Modes

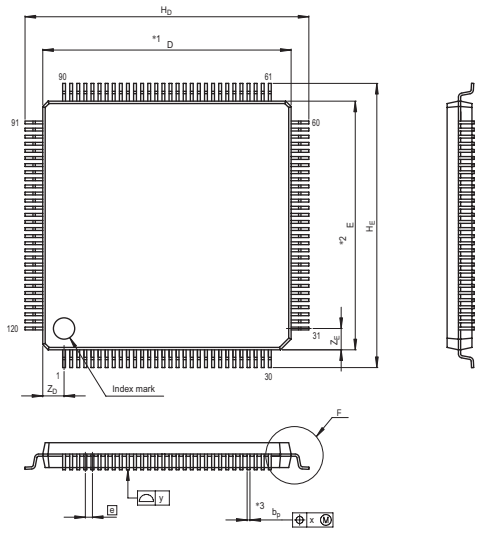
	On-board Programming Mode		Off-board Mode
Item	**User Programming Mode**	**Boot Mode**	**Programmer Mode**
Functional overview	The user ROM is programmed by the CPU through execution of software commands. EW0 mode: Programming can be done from outside of the flash memory.	The user ROM is programmed through the on-chip SCI interface. Standard serial I/O mode 1: Clock-synchronous serial I/O Standard serial I/O mode 2: Asynchronous serial I/O	The user ROM is programmed through a dedicated parallel programmer.
Programmable area	User ROM, data flash	User ROM, data flash	User ROM, data flash
Operating mode	Single-chip mode, on-chip ROM enabled expanded mode (EW0 mode)	Boot mode	Programmer mode
ROM programmer	—	—	Parallel programmer

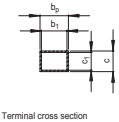
Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output high voltage	All output pins	V_{OH}	V_{CC} – 0.3	—	—	V	I_{OH} = –200 µA
			V_{CC} – 0.5	—	—	V	I_{OH} = –1 mA
			V_{CC} – 0.8	—	—	V	I_{OH} = –2 mA
Output low voltage	All output pins	V_{OL}	—	—	0.4	V	I_{OL} = 4.0 mA
	P26 to P27*4, P32 to P35*4, P50 to P51*4		—	—	0.4	V	I_{OL} = 8.0 mA
Input leakage current	$\overline{RES}$	$\|I_{in}\|$	—	—	10.0	µA	V_{in} = 0.5 to V_{CC} –0.5 V
	$\overline{STBY}$, NMI, MD2 to MD0		—	—	1.0	µA	
	Port 4, Port 9		—	—	1.0	µA	V_{in} = 0.5 to AV_{CC} –0.5 V

Notes: Port 2, P32 to P35, P50, P51, P81, and P83 are 5 V-tolerant pins.

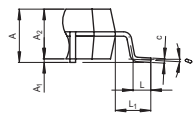
1. When the A/D and D/A converters are not used, the AV_{CC}, V_{ref}, and AV_{SS} pins should not be open. Connect the AV_{CC} and V_{ref} pins to V_{CC}, and the AV_{SS} pin to V_{SS}.
2. When used as $\overline{IRQ}$, TIOC, TCLK, TMRI, SCL, or SDA.
3. When used as other than $\overline{IRQ}$, TIOC, TCLK, TMRI, SCL, or SDA.
4. When used as SCL or SDA.
5. When used as SSO, SSI, SSCK, $\overline{SCS}$, $\overline{WAIT}$, $\overline{ADTRG1}$ or $\overline{DREQ}$.
6. When used as other than SSO, SSI, SSCK, $\overline{SCS}$, $\overline{WAIT}$, $\overline{ADTRG1}$ or $\overline{DREQ}$.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP120-16x16-0.50	PLQP0120KA-A	—	0.9g





Terminal cross section



Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	15.9	16.0	16.1
E	15.9	16.0	16.1
A_2	—	1.4	—
H_D	17.8	18.0	18.2
H_E	17.8	18.0	18.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	0.75	—
Z_E	—	0.75	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure B.4 Package Dimensions (PLQ0120KA-A)