Renesas Electronics America Inc - R4F24565NVFQV Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8S/2600
Core Size	16-Bit
Speed	32MHz
Connectivity	EBI/EMI, I²C, IrDA, SCI, SSU, UART/USART, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	96
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b; D/A 2x8b
Oscillator Type	External
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r4f24565nvfqv

		Pin No.				
		H8S/2456, H8S/2456R		H8S/2454		
Type	Symbol	PLQP0144KA-A	PTLG0145JB-A	PLQP0120LA-A, PLQP0120KA-A	I/O	Function
Bus control	$\overline{\text{WAIT-A}}$	84	J11	69	Input	Requests insertion of a wait state in the bus cycles when accessing an external 3-state address space.
	$\overline{\text{WAIT-B}}$	56	N7	47		
	$\overline{\text{OE-A}}$	38	M2	69	Output	Output enable signal when accessing the DRAM space.
	$\overline{\text{OE-B}}$	137	A5	113		
	CKE-A*1	38	M2	—	Output	Clock enable signal when the synchronous DRAM interface is set.
	CKE-B*1	137	A5	—		
Interrupts	NMI	40	N1	32	Input	Nonmaskable interrupt request pin. This pin should be fixed high when not used.
	$\overline{\text{IRQ15-A}}$ to $\overline{\text{IRQ8-A}}$*2	86, 85, 106 to 104, 83 to 81	H10, H12, C13, D12, D10, J10, K13, J12	—		These pins request a maskable interrupt. The input pins of $\overline{\text{IRQn-A}}$ and $\overline{\text{IRQn-B}}$ are selected by the IRQ pin select register (ITSR) of the interrupt controller. (n = 0 to 15, m=0 to 8, 13 to 15 for the H8S/2456R Group and H8S/2456) (n = 0 to 7 for the H8S/2454 Group)
	$\overline{\text{IRQ7-A}}$ to $\overline{\text{IRQ0-A}}$	31 to 28, 136 to 133	J3, K2, J1, K4, D4, C6, B5, A6	29 to 26, 112 to 109		
	$\overline{\text{IRQ15-B}}$ to $\overline{\text{IRQ13-B}}$*2 $\overline{\text{IRQ8-B}}$*2	58 to 56 51	K7, L8, N7, L6	—		
	$\overline{\text{IRQ7-B}}$ to $\overline{\text{IRQ0-B}}$	38, 37, 61 to 59, 34, 33, 3	M2, N2, M8, N8, K8, K3, L2, C2	102 to 95		
DMA controller (DMAC)	$\overline{\text{DREQ1}}$	82	K13, J12	35	Input	These signals request DMAC activation.
	$\overline{\text{DREQ0}}$	81		34		
	$\overline{\text{TEND1}}$	104	D10	37	Output	These signals indicate the end of DMAC data transfer.
	$\overline{\text{TEND0}}$	83	J10	36		
	$\overline{\text{DACK1}}$	106	C13	39	Output	DMAC single address transfer acknowledge signals.
	$\overline{\text{DACK0}}$	105	D12	38		
EXDMA controller (EXDMAC) *2	$\overline{\text{EDREQ3}}$	33	L2	—	Input	These signals request EXDMAC activation.
	$\overline{\text{EDREQ2}}$	3	C2			
	$\overline{\text{ETEND3}}$	59	K8	—	Output	These signals indicate the end of EXDMAC data transfer.
	$\overline{\text{ETEND2}}$	34	K3			
	$\overline{\text{EDACK3}}$	61	M8	—	Output	EXDMAC single address transfer acknowledge signals.
	$\overline{\text{EDACK2}}$	60	N8			

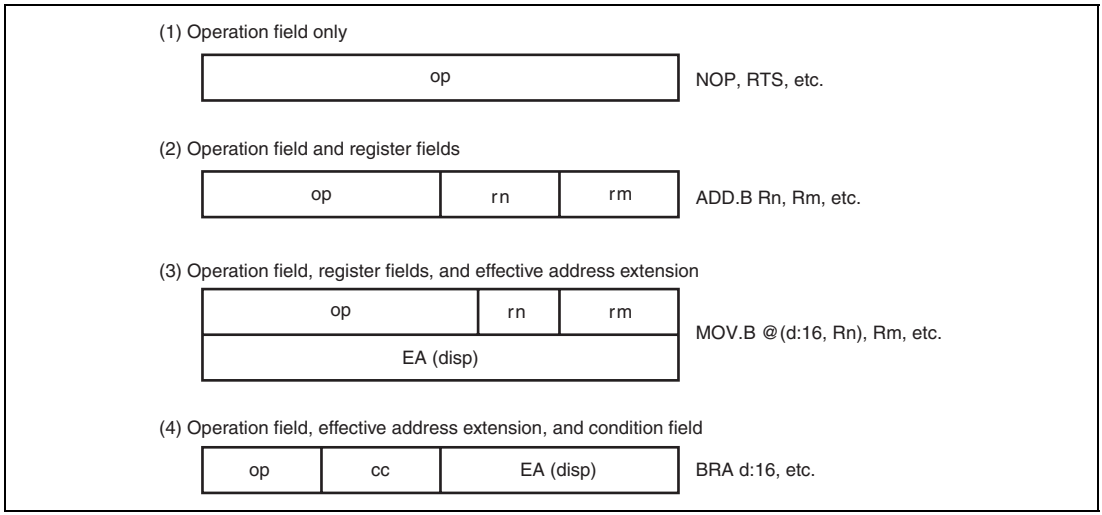
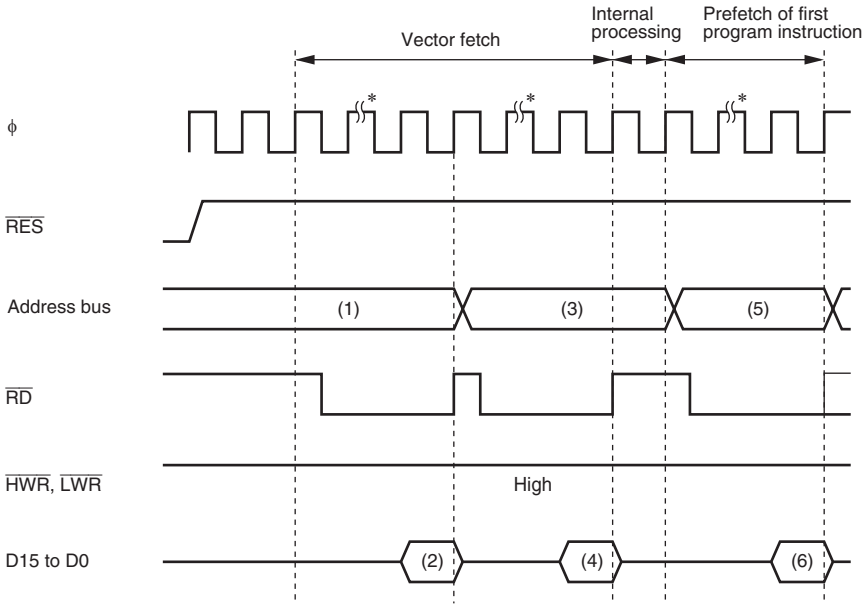


Figure 2.11 Instruction Formats (Examples)



(1)(3) Reset exception handling vector address (when reset, (1)=H'000000, (3)=H'000002)
(2)(4) Start address (contents of reset exception handling vector address)
(5) Start address ((5)=(2)(4))
(6) First program instruction

Note: * Seven program wait states are inserted.

Figure 4.2 Reset Sequence (Advanced Mode with On-chip ROM Disabled)

4.3.2 Interrupts after Reset

If an interrupt is accepted after a reset but before the stack pointer (SP) is initialized, the PC and CCR will not be saved correctly, leading to a program crash. To prevent this, all interrupt requests, including NMI, are disabled immediately after a reset. Since the first instruction of a program is always executed immediately after the reset state ends, make sure that this instruction initializes the stack pointer (example: MOV.L #xx: 32, SP).

4.3.3 On-Chip Peripheral Functions after Reset Release

After reset release, MSTPCR is initialized to H'0FFF, EXMSTPCR is initialized to H'FFFF, and all modules except the DMAC, EXDMAC, and DTC enter the module stop state.

Consequently, on-chip peripheral module registers cannot be read or written to. Register reading and writing is enabled when the module stop state is exited.

Bit	Bit Name	Initial Value	R/W	Description
10	—	0	R/W	Reserved This bit can be read from or written to. However, the write value should always be 0.
9	RCD1	0	R/W	RAS-CAS Wait Control
8	RCD0	0	R/W	These bits select a wait cycle to be inserted between the $\overline{RAS}$ assert cycle and $\overline{CAS}$ assert cycle. A 1- to 4-state wait cycle can be inserted. 00: Wait cycle not inserted 01: 1-state wait cycle inserted 10: 2-state wait cycle inserted 11: 3-state wait cycle inserted
7 to 4	—	All 0	R/W	Reserved These bits can be read from or written to. However, the write value should always be 0.
3	CKSPE*	0	R/W	Clock Suspend Enable Enables clock suspend mode for extend read data during DMAC and EXDMAC single address transfer with the synchronous DRAM interface. 0: Disables clock suspend mode 1: Enables clock suspend mode
2	—	0	R/W	Reserved This bit can be read from or written to. However, the write value should always be 0.
1	RDXC1*	0	R/W	Read Data Extension Cycle Number Selection
0	RDXC0*	0	R/W	Selects the number of read data extension cycle (Tsp) insertion state in clock suspend mode. These bits are valid when the CKSPE bit is set to 1. 00: Inserts 1 state 01: Inserts 2 state 10: Inserts 3 state 11: Inserts 4 state

Note: * Not supported by the H8S/2456 Group and H8S/2454 Group.

6.8.8 Row Address Output State Control

When the command interval specification from the ACTV command to the next READ/WRIT command cannot be satisfied, 1 to 3 states (Trw) that output the NOP command can be inserted between the Tr cycle that outputs the ACTV command and the Tc1 cycle that outputs the column address by setting the RCD1 and RCD0 bits of DRACCR. Use the optimum setting for the wait time according to the synchronous DRAM connected and the operating frequency of this LSI. Figure 6.58 shows an example of the timing when the one Trw state is set.

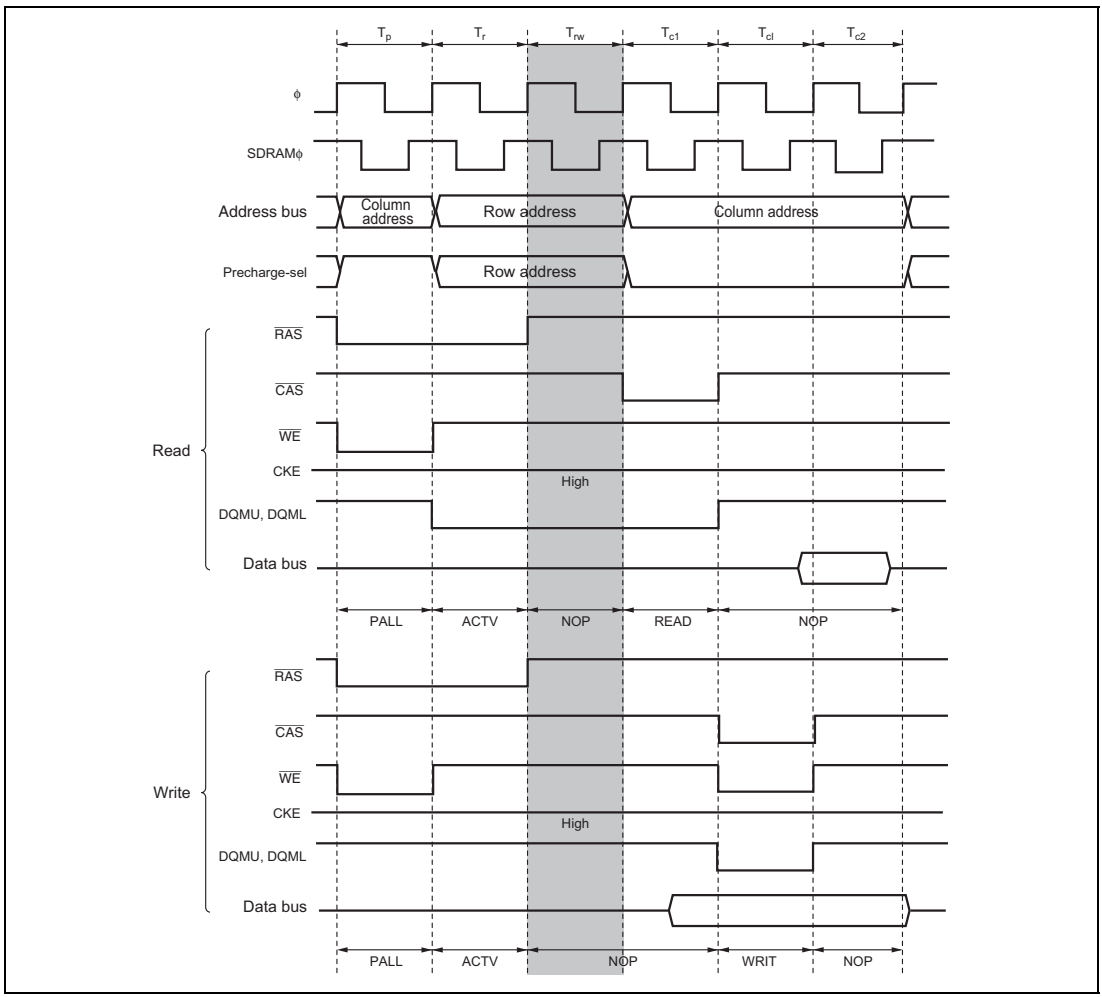


Figure 6.58 Example of Access Timing when Row Address Output Hold State Is 1 State (RCD1 = 0, RCD0 = 1, SDWCD = 0, CAS Latency 2)

7.3.4 DMA Control Registers (DMACRA and DMACRB)

DMACR controls the operation of each DMAC channel.

The DMA has four DMACR registers: DMACR_0A in channel 0 (channel 0A), DMACR_0B in channel 0 (channel 0B), DMACR_1A in channel 1 (channel 1A), and DMACR_1B in channel 1 (channel 1B). In short address mode, channels A and B operate independently, and in full address mode, channels A and B operate together. The bit functions in the DMACR registers differ according to the transfer mode.

(1) Short Address Mode:

- DMACR_0A, DMACR_0B, DMACR_1A, and DMARC_1B

Bit	Bit Name	Initial Value	R/W	Description
7	DTSZ	0	R/W	Data Transfer Size Selects the size of data to be transferred at one time. 0: Byte-size transfer 1: Word-size transfer
6	DTID	0	R/W	Data Transfer Increment/Decrement Selects incrementing or decrementing of MAR after every data transfer in sequential mode or repeat mode. In idle mode, MAR is neither incremented nor decremented. 0: MAR is incremented after a data transfer (Initial value) • When DTSZ = 0, MAR is incremented by 1 • When DTSZ = 1, MAR is incremented by 2 1: MAR is decremented after a data transfer • When DTSZ = 0, MAR is decremented by 1 • When DTSZ = 1, MAR is decremented by 2

Bit	Bit Name	Initial Value	R/W	Description
3	DTIE1B	0	R/W	Data Transfer End Interrupt Enable 1B
2	DTIE1A	0	R/W	Data Transfer End Interrupt Enable 1A
1	DTIE0B	0	R/W	Data Transfer End Interrupt Enable 0B
0	DTIE0A	0	R/W	Data Transfer End Interrupt Enable 0A These bits enable or disable an interrupt to the CPU or DTC when transfer ends. If the DTIE bit is set to 1 when DTE = 0, the DMAC regards this as indicating the end of a transfer, and issues a transfer end interrupt request to the CPU or DTC. A transfer end interrupt can be canceled either by clearing the DTIE bit to 0 in the interrupt handling routine, or by performing processing to continue transfer by setting the transfer counter and address register again, and then setting the DTE bit to 1.

(2) Full Address Mode:

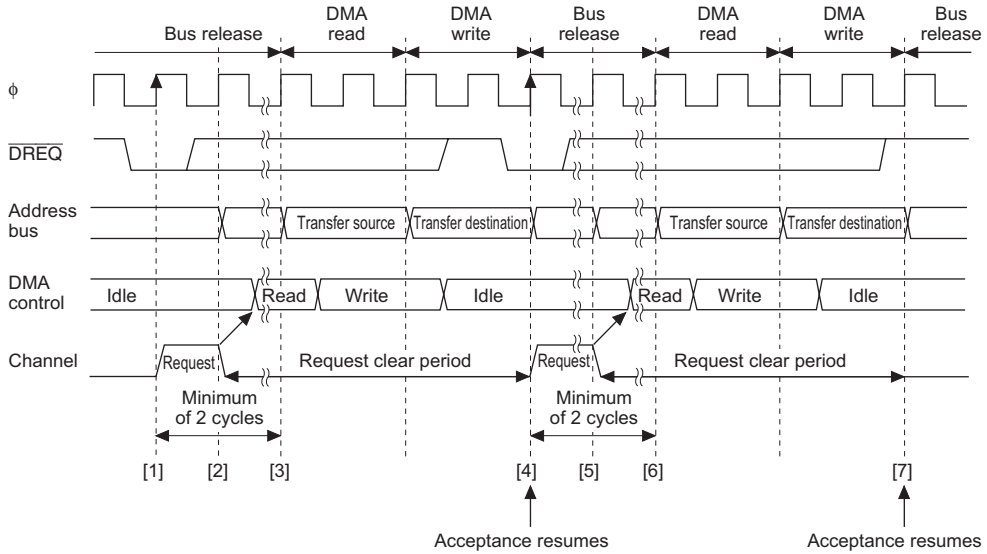
- DMABCRH

Bit	Bit Name	Initial Value	R/W	Description
15	FAE1	0	R/W	Full Address Enable 1 Specifies whether channel 1 is to be used in short address mode or full address mode. In full address mode, channels 1A and 1B are used together as channel 1. 0: Short address mode 1: Full address mode
14	FAE0	0	R/W	Full Address Enable 0 Specifies whether channel 0 is to be used in short address mode or full address mode. In full address mode, channels 0A and 0B are used together as channel 0. 0: Short address mode 1: Full address mode

(5) $\overline{\text{DREQ}}$ Pin Falling Edge Activation Timing

Set the DTA bit in DMABCRH to 1 for the channel for which the $\overline{\text{DREQ}}$ pin is selected.

Figure 7.22 shows an example of normal mode transfer activated by the $\overline{\text{DREQ}}$ pin falling edge.



[1] Acceptance after transfer enabling; the $\overline{\text{DREQ}}$ pin low level is sampled on the rising edge of φ, and the request is held.

[2] [5] The request is cleared at the next bus break, and activation is started in the DMAC.

[3] [6] Start of DMA cycle; $\overline{\text{DREQ}}$ pin high level sampling on the rising edge of φ starts.

[4] [7] When the $\overline{\text{DREQ}}$ pin high level has been sampled, acceptance is resumed after the write cycle is completed.
(As in [1], the $\overline{\text{DREQ}}$ pin low level is sampled on the rising edge of φ, and the request is held.)

Note: In write data buffer mode, bus breaks from [2] to [7] may be hidden, and not visible.

Figure 7.22 Example of $\overline{\text{DREQ}}$ Pin Falling Edge Activated Normal Mode Transfer

7.5.14 DMAC and NMI Interrupts

When an NMI interrupt is requested, burst mode transfer in full address mode is interrupted. An NMI interrupt does not affect the operation of the DMAC in other modes.

In full address mode, transfer is enabled for a channel when both the DTE bit and DTME bit in DMABCRL are set to 1. With burst mode setting, the DTME bit is cleared when an NMI interrupt is requested.

If the DTME bit is cleared during burst mode transfer, the DMAC discontinues transfer on completion of the 1-byte or 1-word transfer in progress, then releases the bus, which passes to the CPU.

The channel on which transfer was interrupted can be restarted by setting the DTME bit to 1 again. Figure 7.35 shows the procedure for continuing transfer when it has been interrupted by an NMI interrupt on a channel designated for burst mode transfer.

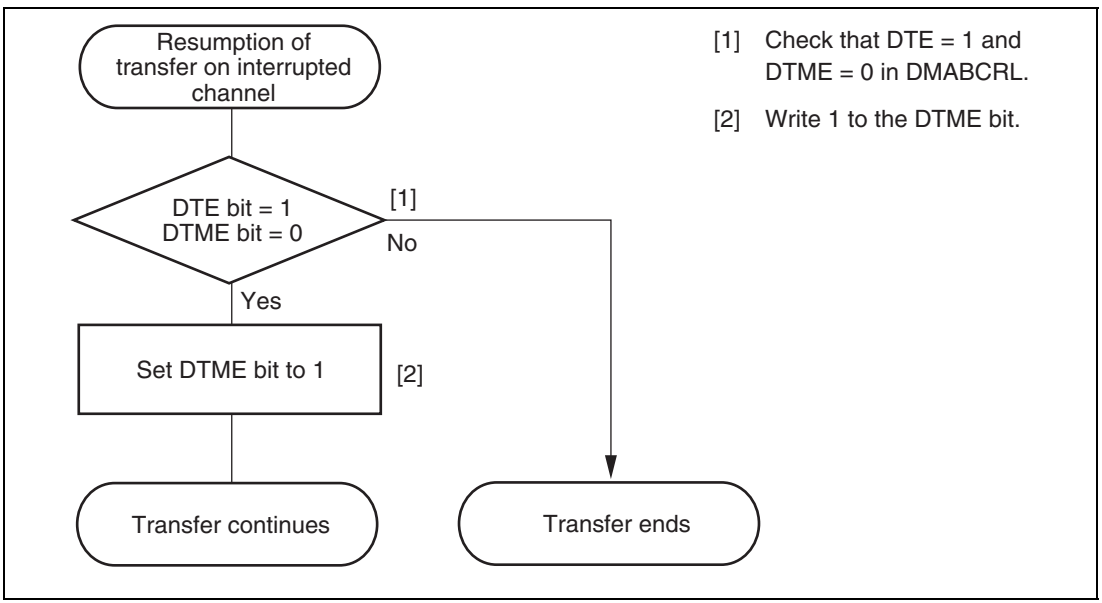


Figure 7.35 Example of Procedure for Continuing Transfer on Channel Interrupted by NMI Interrupt

Bit	Bit Name	Initial Value	R/W	Description
10	AMS	0	R/W	Address Mode Select Selects single address mode or dual address mode. When single address mode is selected, the $\overline{\text{EDACK}}$ pin is valid. 0: Dual address mode 1: Single address mode
9	MDS1	0	R/W	Mode Select 1 and 0 These bits specify the activation source, bus mode, and transfer mode. 00: Auto request, cycle steal mode, normal transfer mode 01: Auto request, burst mode, normal transfer mode 10: External request, cycle steal mode, normal transfer mode 11: External request, cycle steal mode, block transfer mode
8	MDS0	0	R/W	
7	EDIE	0	R/W	EXDMA Interrupt Enable Enables or disables interrupt requests. When this bit is set to 1, an interrupt is requested when the IRF bit is set to 1. The interrupt request is cleared by clearing this bit or the IRF bit to 0. 0: Interrupt request is not generated 1: Interrupt request is generated

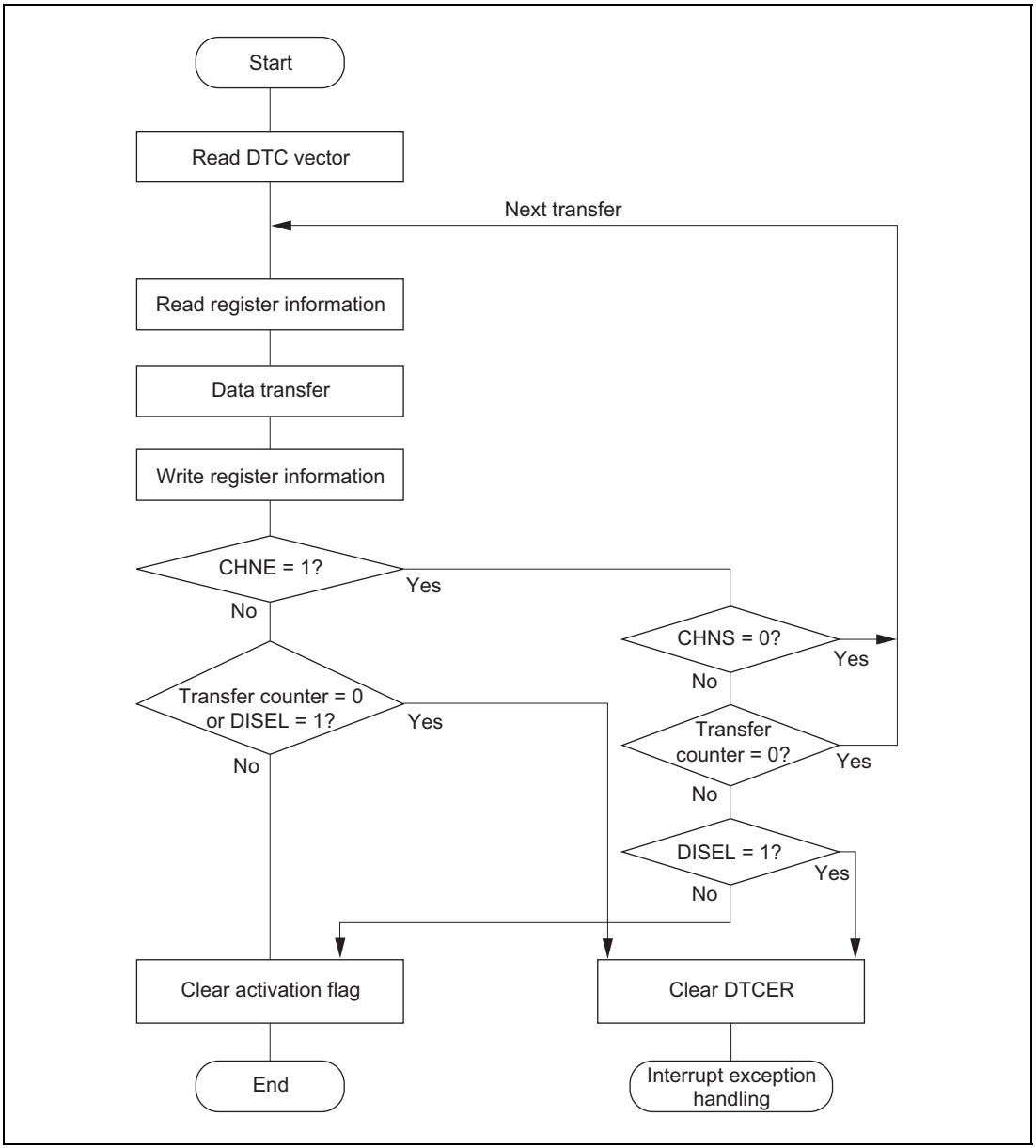


Figure 9.5 Flowchart of DTC Operation

Port	Description	Mode 1	Mode 2	Mode 4	Mode 3, 7 EXPE = 1	Mode 3, 7 EXPE = 0	Schmitt-triggered input Pin*	Input Pull-up MOS Capability	Open Drain Output Capability	5-V Tolerance
Port A	General I/O port also functioning as address outputs, interrupt inputs, SSU I/Os, SCI I/Os, and bus control signal outputs	PA7/A23/CS7/IRQ7-A/ SSO0-B		PA7/A23/CS7/IRQ7-A/ SSO0-B		PA7/IRQ7-A/ SSO0-B	IRQ7-A	O	All output pin functions other than address outputs and CS7	—
		PA6/A22/IRQ6-A/ SSI0-B		PA6/A22/IRQ6-A/ SSI0-B		PA6/IRQ6-A/ SSI0-B	IRQ6-A			
		PA5/A21/IRQ5-A/ SSCK0-B		PA5/A21/IRQ5-A/ SSCK0-B		PA5/IRQ5-A/ SSCK0-B	IRQ5-A			
		A20/IRQ4-A		PA4/A20/IRQ4-A/ SCS0-B		PA4/IRQ4-A/ SCS0-B	IRQ4-A			
		A19		PA3/A19/SCK4-B		PA3/SCK4-B	—			
		A18		PA2/A18/RxD4-B		PA2/RxD4-B				
		A17		PA1/A17/TxD4-B		PA1/TxD4-B				
		A16		PA0/A16		PA0				
Port B	General I/O port also functioning as address outputs and TPU I/Os	A15		PB7/A15		PB7/TIOCB8 /TCLKH	TIOCB8/ TCLKH	O	All output pin functions other than address outputs	—
		A14		PB6/A14		PB6/TIOCA8	TIOCA8			
		A13		PB5/A13		PB5/TIOCB7 /TCLKG	TIOCB7/ TCLKG			
		A12		PB4/A12		PB4/TIOCA7	TIOCA7			
		A11		PB3/A11		PB3/TIOCD 6/TCLKF	TIOCD6/ TCLKF			
		A10		PB2/A10		PB2/TIOCC 6/TCLKE	TIOCC6/ TCLKE			
		A9		PB1/A9		PB1/TIOCB6	TIOCB6			
		A8		PB0/A8		PB0/TIOCA6	TIOCA6			
Port C	General I/O port also functioning as address outputs and TPU I/Os	A7		PC7/A7		PC7/ TIOCB11	TIOCB11	O	All output pin functions other than address outputs	—
		A6		PC6/A6		PC6/ TIOCA11	TIOCA11			
		A5		PC5/A5		PC5/ TIOCB10	TIOCB10			
		A4		PC4/A4		PC4/ TIOCA10	TIOCA10			
		A3		PC3/A3		PC3/ TIOCD9	TIOCD9			
		A2		PC2/A2		PC2/ TIOCC9	TIOCC9			
		A1		PC1/A1		PC1/ TIOCB9	TIOCB9			
		A0		PC0/A0		PC0/ TIOCA9	TIOCA9			

TPU channel 4 settings	(2)	(1)	(2)	(2)	(1)	(2)
MD3 to MD0	B'0000, B'01xx		B'0010	B'0011		
IOB3 to IOB0	B'0000, B'0100, B'1xxx	B'0001 to B'0011, B'0101 to B'0111	—	B'xx00	Other than B'xx00	
CCLR1, CCLR0	—	—	—	—	Other than B'10	B'10
Output function	—	Output compare output	—	—	PWM mode 2 output	—

[Legend]

x: Don't care

- P20/PO0-A/TIOCA3-A/TMRI0-A/PUPD+

  The pin function is switched as shown below according to the combination of the TPU channel 3 settings (by bits MD3 to MD0 in TMDR_3, bits IOA3 to IOA0 in TIOR H_3, and bits CCLR2 to CCLR0 in TCR_3), bit NDER0 in NDERL of the PPG, bit PULLUP_E in CTLR of the USB, bits PPGS, TPUS and TMRS in PFCR3, and bit P20DDR.

PULLUP_E	0				1
TPU channel 3 settings	(1) in table below	(2) in table below			—
P20DDR	—	0	1		—
NDER0	—	—	0	1	—
Pin function	TIOCA3-A output*5	P20 input	P20 output	PO0-A output*4	PUPD+ output
		TIOCA3-A input*1*5			
	$\overline{\text{IRQ8-B}}$-A input*2*6				

(4) Status Flag Clearing Timing

After a status flag is read as 1 by the CPU, it is cleared by writing 0 to it. When the DTC or DMAC is activated, the flag is cleared automatically. Figure 11.43 shows the timing for status flag clearing by the CPU, and figure 11.44 shows the timing for status flag clearing by the DTC or DMAC.

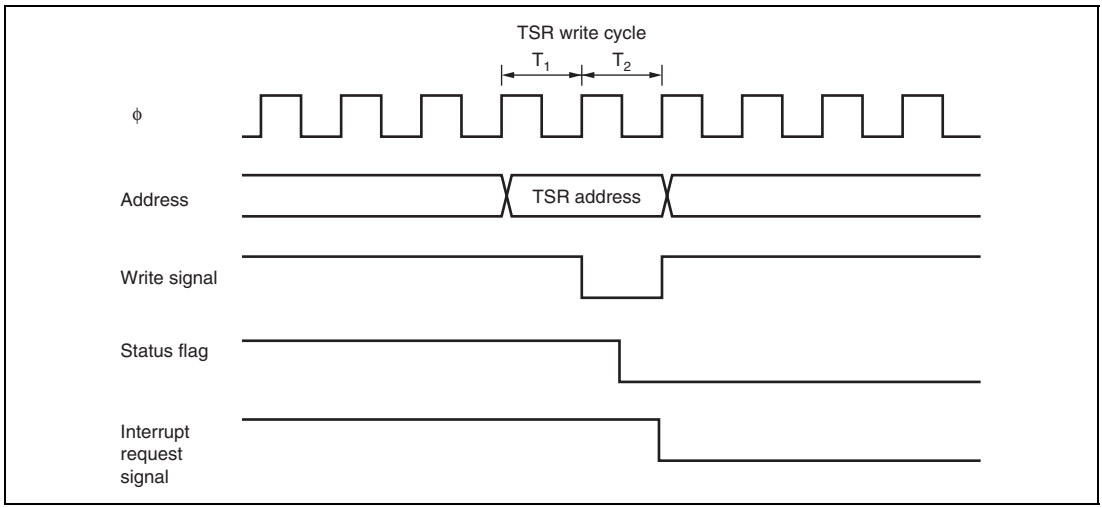


Figure 11.43 Timing for Status Flag Clearing by CPU

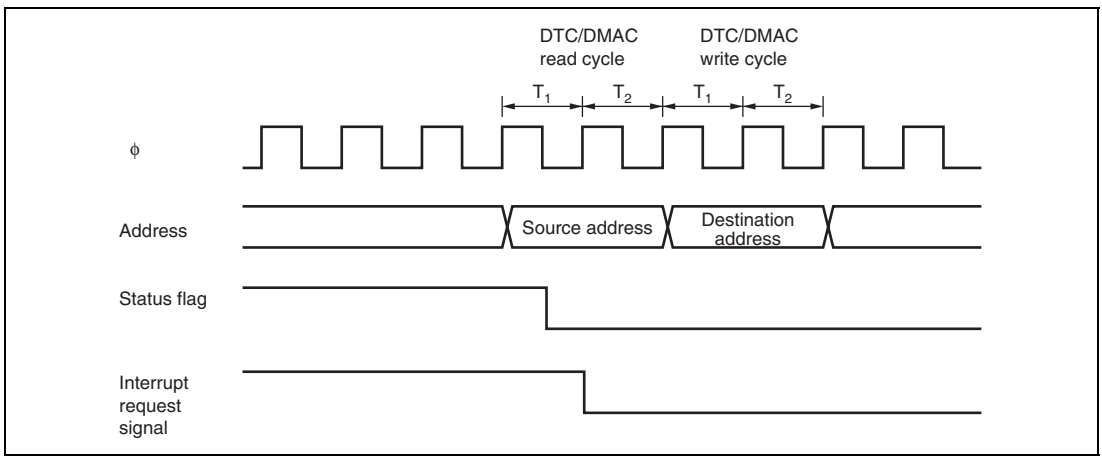


Figure 11.44 Timing for Status Flag Clearing by DTC/DMAC Activation

13.8.3 Contention between TCOR Write and Compare Match

During the T_2 state of a TCOR write cycle, the TCOR write has priority and the compare match signal is inhibited even if a compare match event occurs as shown in figure 13.13.

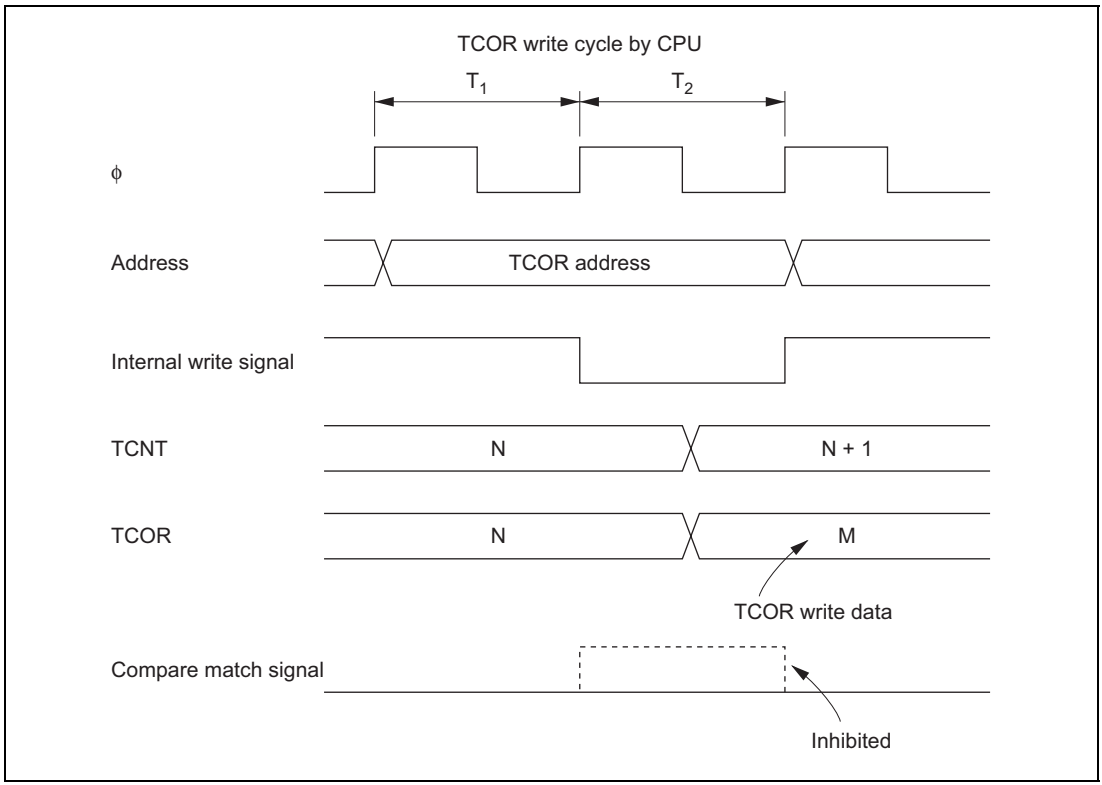


Figure 13.13 Contention between TCOR Write and Compare Match

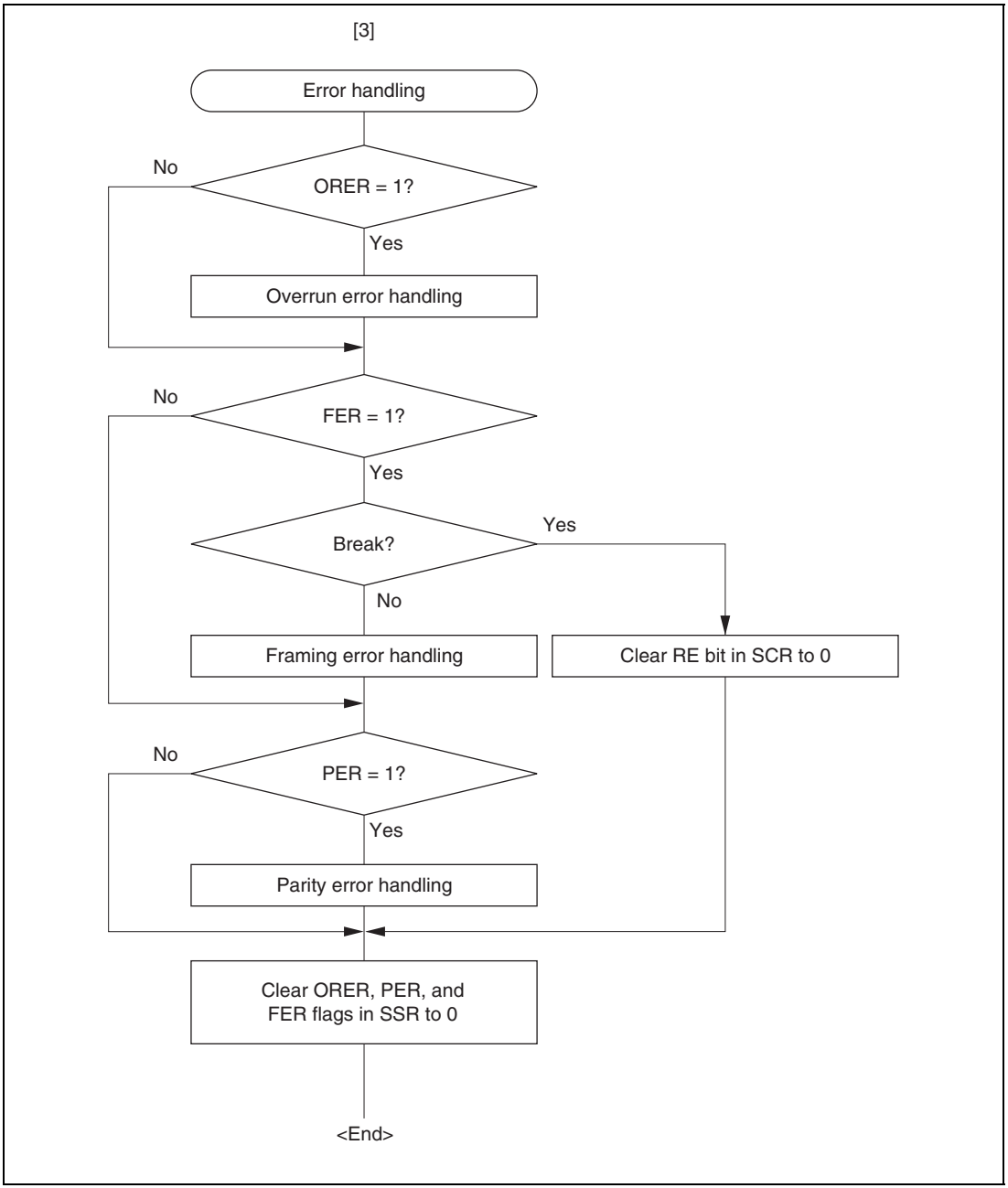


Figure 15.9 Sample Serial Reception Data Flowchart (2)

Bit	Bit Name	Initial Value	R/W	Description
4	RWUPS	0	R	Remote Wakeup Status This status bit indicates remote wakeup command from USB host is enabled or disabled. This bit is set to 0 when remote wakeup command from UBM host is disabled by Device_Remote_Wakeup due to Set Feature or Clear Feature request. This bit is set to 1 when remote wakeup command is enabled.
3	RSME	0	R/W	Resume Enable This bit releases the suspend state (or executes remote wakeup). When RSME is set to 1, resume request starts. If RSME is once set to 1, clear this bit to 0 again afterwards. In this case, the value 1 set to RSME must be kept for at least one clock period of 12-MHz clock.
2	PWMD	0	R/W	Bus Power Mode This bit specifies the USB power mode. When PWMD is set to 0, the self-power mode is selected for this module. When set to 1, the bus-power mode is selected.
1	EP0 ASCE	0	R/W	EP0 Automatic Stall Clear Enable Setting the EP0 ASCE bit to 1 automatically clears the EP0 stall setting bit (the EP0 STLS bit in EPSTL0) after the stall handshake is returned to the host. When the EP0 ASCE bit is set to 0, the stall setting bit is not automatically cleared and must be cleared by the users. To enable the automatic stall clear function, make sure that the EP0 ASCE bit should be set to 1 before the EP0 STLS bit in EPSTL0 is set to 1.
0	PRTRST	1	R/W	Protocol Processing Block Reset 0: The protocol processing block is placed in operation state. 1: The protocol processing block is placed in reset state.

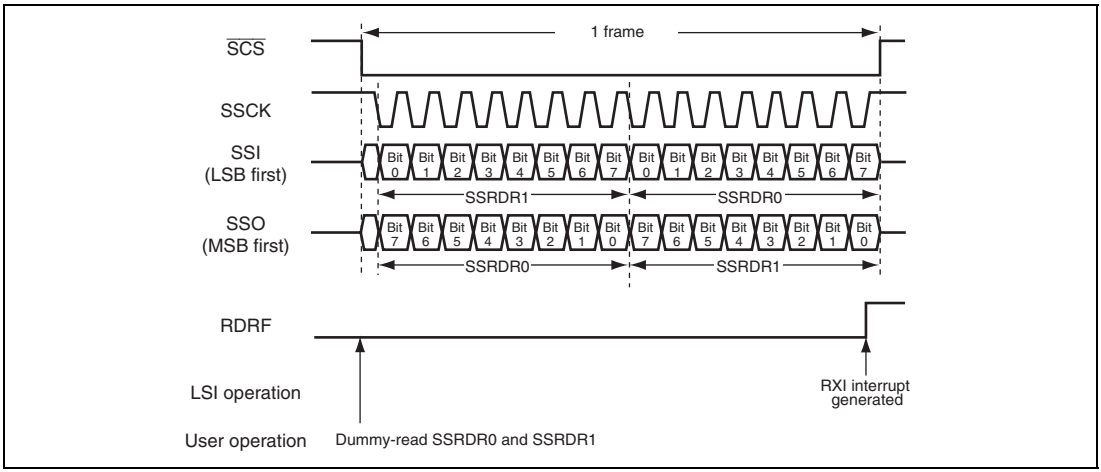


Figure 20.7 (2) Example of Reception Operation (SSU Mode) When 16-bit data length is selected (SSRDR0 and SSRDR1 are valid) with CPOS = 0 and CPHS = 0

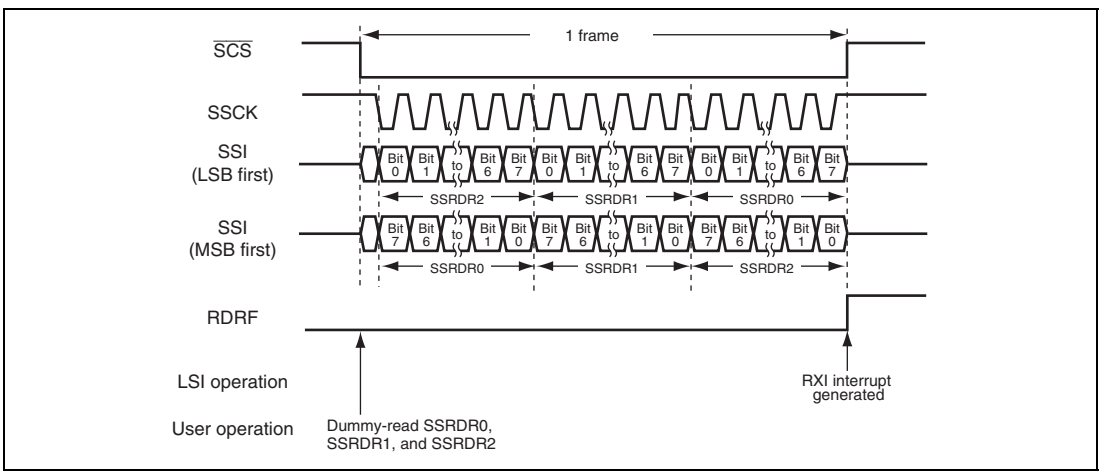


Figure 20.7 Example of Reception Operation (SSU Mode) When 24-bit data length is selected (SSRDR0, SSRDR1, and SSRDR2 are valid) with CPOS = 0 and CPHS = 0 (3)

(a) Erasure Selection

The boot program will transfer the erasure program. User ROM data is erased by the transferred erasure program.

Command	H'48

- Command, H'48, (1 byte): Erasure selection

Response	H'06

- Response, H'06, (1 byte): Response for erasure selection

  After the erasure program has been transferred, the boot program will return ACK.

Error response	H'C8	ERROR

- Error response, H'C8, (1 byte): Response to erasure selection
- ERROR (1 byte): Error code

  H'54: Selection processing error (transfer error occurs and processing is not completed)

(b) Block Erasure

The boot program will erase the contents of the specified block.

Command	H'58	Size	Block number	SUM

- Command, H'58, (1 byte): Block erasure
- Size (1 byte): The number of bytes that represents the erasure block number

  This is fixed to 1.
- Block number (1 byte): Number of the block to be erased
- SUM (1 byte): Checksum

Response	H'06

- Response, H'06, (1 byte): Response to Erasure

  After erasure has been completed, the boot program will return ACK.

Error Response	H'D8	ERROR

- Error Response, H'D8, (1 byte): Response to block erasure
- ERROR (1 byte): Error code

  H'11: Sum check error

  H'29: Block number error

  Block number is incorrect.

  H'51: Erasure error

  An error has occurred during erasure.

S