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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8S/2600
Core Size	16-Bit
Speed	32MHz
Connectivity	EBI/EMI, I²C, IrDA, SCI, SSU, UART/USART, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	94
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b; D/A 2x8b
Oscillator Type	External
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r4f24568nvfqv

6.3.12 Refresh Timer Counter (RTCNT)

RTCNT is an 8-bit readable/writable up-counter. RTCNT counts up using the internal clock selected by bits RTCK2 to RTCK0 in REFCR.

When RTCNT matches RTCOR (compare match), the CMF flag in REFCR is set to 1 and RTCNT is cleared to H'00. If the RFSHE bit in REFCR is set to 1 at this time, a refresh cycle is started. If the RFSHE bit is cleared to 0 and the CMIE bit in REFCR is set to 1, a compare match interrupt (CMI) is generated.

RTCNT is initialized to H'00 by a reset and in hardware standby mode. It is not initialized in software standby mode.

6.3.13 Refresh Time Constant Register (RTCOR)

RTCOR is an 8-bit readable/writable register that sets the period for compare match operations with RTCNT.

The values of RTCOR and RTCNT are constantly compared, and if they match, the CMF flag in REFCR is set to 1 and RTCNT is cleared to H'00.

RTCOR is initialized to H'FF by a reset and in hardware standby mode. It is not initialized in software standby mode.

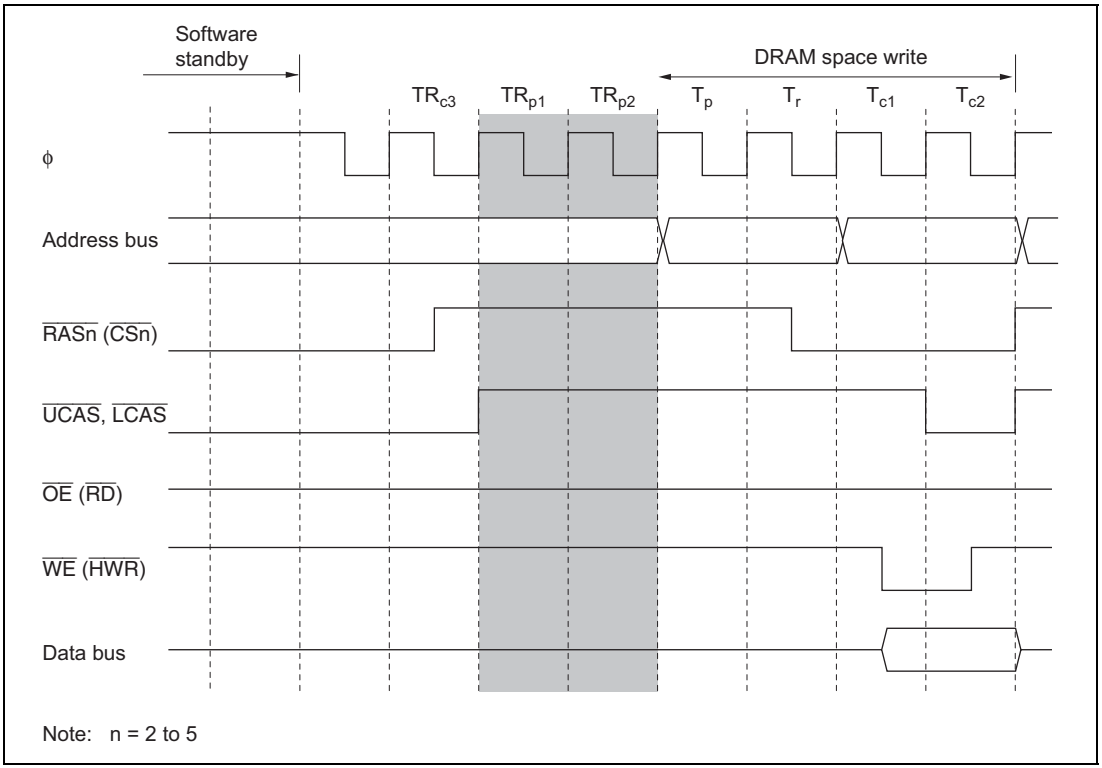

Figure 6.52 Example of Timing when Precharge Time after Self-Refreshing Is Extended by 2 States

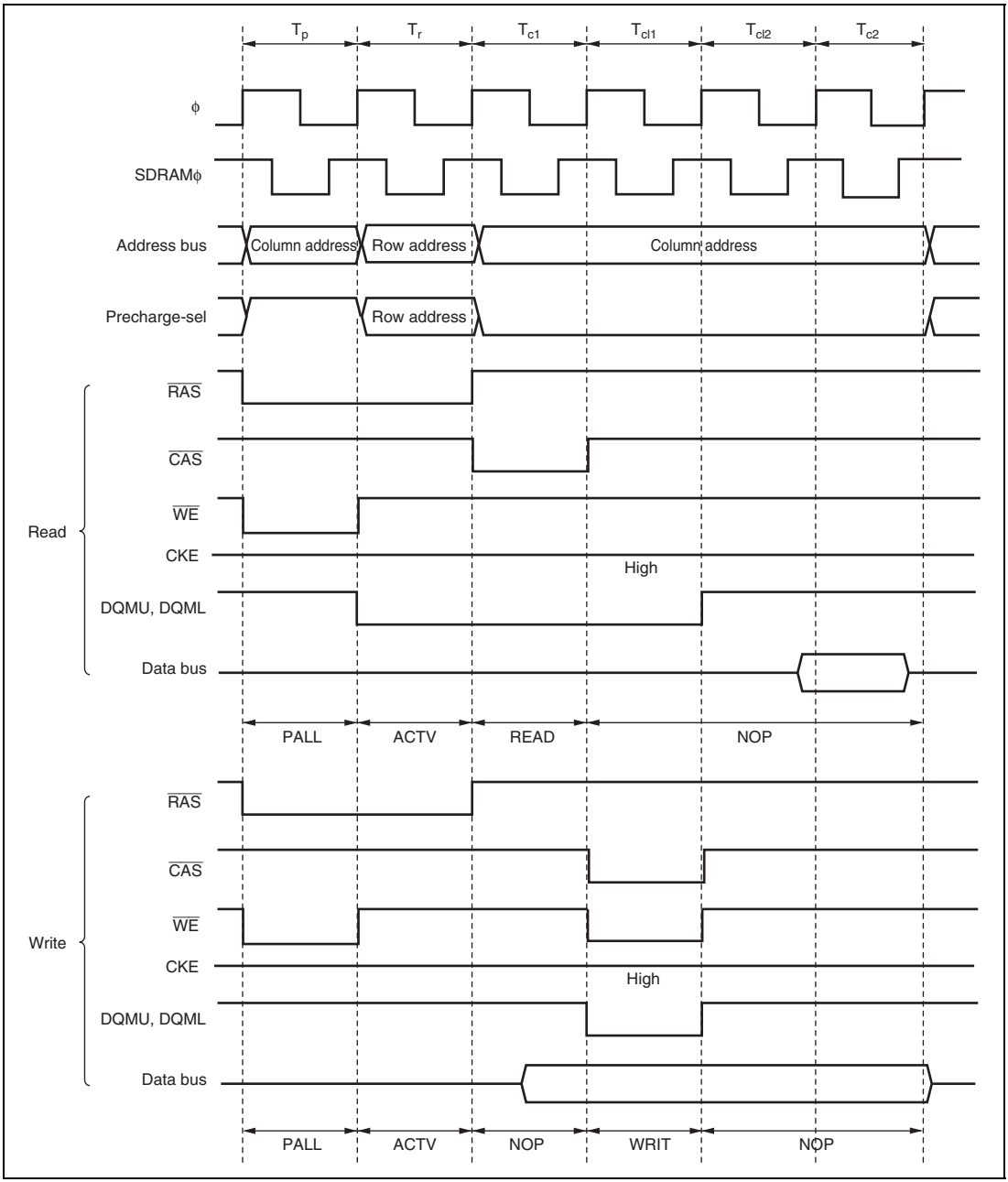

Figure 6.57 CAS Latency Control Timing (SDWCD = 0, CAS Latency 3)

Bit	Bit Name	Initial Value	R/W	Description
12	SARA4	0	R/W	Source Address Repeat Area
11	SARA3	0	R/W	These bits specify the source address (EDSAR) repeat area. The repeat area function updates the specified lower address bits, leaving the remaining upper address bits always the same. A repeat area size of 2 bytes to 8 Mbytes can be specified. The setting interval is a power-of-two number of bytes. When repeat area overflow results from incrementing or decrementing an address, the lower address is the start address of the repeat area in the case of address incrementing, or the last address of the repeat area in the case of address decrementing. If the SARIE bit is set to 1, an interrupt can be requested when repeat area overflow occurs. 00000: Not designated as repeat area 00001: Lower 1 bit (2-byte area) designated as repeat area 00010: Lower 2 bits (4-byte area) designated as repeat area 00011: Lower 3 bits (8-byte area) designated as repeat area 00100: Lower 4 bits (16-byte area) designated as repeat area : : 10011: Lower 19 bits (512-Kbyte area) designated as repeat area 10100: Lower 20 bits (1-Mbyte area) designated as repeat area 10101: Lower 21 bits (2-Mbyte area) designated as repeat area 10110: Lower 22 bits (4-Mbyte area) designated as repeat area 10111: Lower 23 bits (8-Mbyte area) designated as repeat area 11xxx: Setting prohibited
10	SARA2	0	R/W	
9	SARA1	0	R/W	
8	SARA0	0	R/W	

Figure 8.14 shows examples of transfer timing in cases that include auto request cycle steal mode.

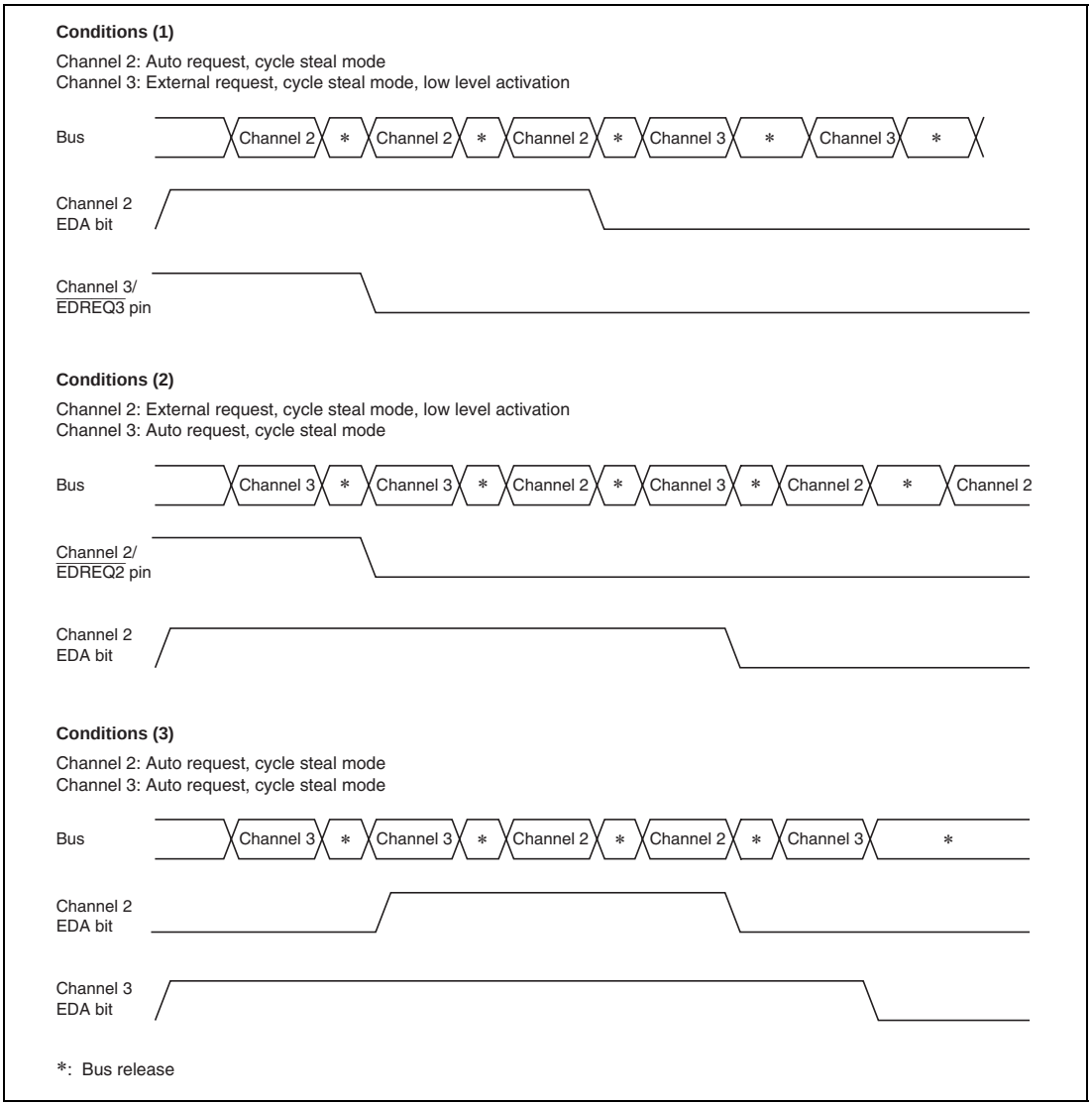

Figure 8.14 Examples of Channel Priority Timing

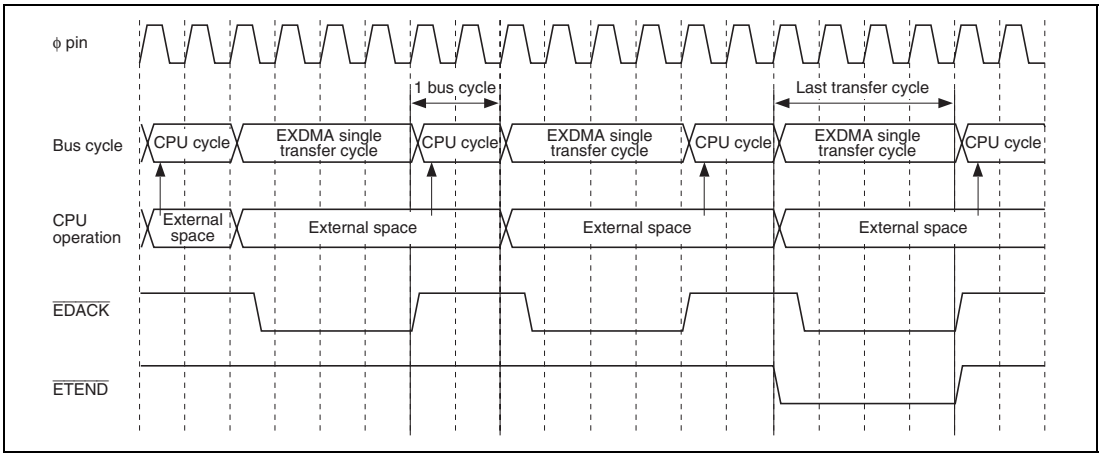

Figure 8.29 Auto Request/Cycle Steal Mode/Normal Transfer Mode (CPU Cycles/Single Address Mode)

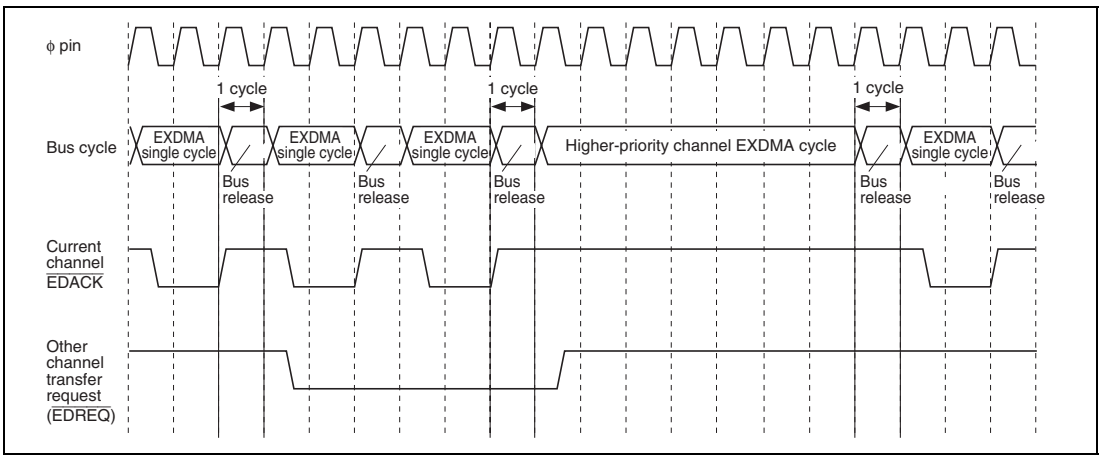

Figure 8.30 Auto Request/Cycle Steal Mode/Normal Transfer Mode (Contention with Another Channel/Single Address Mode)

TPU channel 1 settings	(2)	(1)	(2)	(2)	(1)	(2)
MD3 to MD0	B'0000, B'01xx		B'0010	B'0011		
IOB3 to IOB0	B'0000, B'0100, B'1xxx	B'0001 to B'0011, B'0101 to B'0111	—	B'xx00	Other than B'xx00	
CCLR1, CCLR0	—	—	—	—	Other than B'10	B'10
Output function	—	Output compare output	—	—	PWM mode 2 output	—

[Legend]

x: Don't care

SSU settings	(1)	(1)	(3)	(3)	(2)	(1)	(2)	(1)	(1)	(1)	(1)	(2)	(1)	(2)	(2)	(1)	(2)
SSUMS	0							0				1*1					
BIDE	0							1*2				0					
MSS	0				1			0		1		0			1		
TE	0		1		0		1	0	1	0	1	0		1	0		1
RE	0	1	0	1	1	0	1	1	0	1	0	1	0	1	1	0	1
Pin state	—	—	SSI output	SSI output	SSI input	—	SSI input	—	—	—	—	SSI input	—	SSI input	SSI input	—	SSI input

[Legend]

—: Not used as the SSU pin (can be used as an I/O port).

Notes: See tables 20.4 to 20.6.

1. Do not set BIDE to 1 when SSUMS = 1 in SSU.
2. Do not specify that TE = RE = 1 when operating with BIDE = 1 (bidirectional mode).

10.16.4 Port H Open Drain Control Register (PHODR)

PHODR specifies the output type of each port H pin.

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	—	All 0	—	Reserved These bits are always read as 0. Only the initial values should be written to these bits.
3	PH3ODR	0	R/W	When not specified for $\overline{CS4}$, $\overline{CS5}$, $\overline{CS6}$, $\overline{CS7}$, $\overline{OE\text{-}A}$, CKE-A*, $\overline{RAS4}$, $\overline{RAS5}$, $\overline{WE}$*, or SDRAMϕ* output, setting a PHODR bit to 1 makes the corresponding pin an NMOS open-drain output pin, while clearing a PHODR bit to 0 makes the corresponding pin a CMOS output pin.
2	PH2ODR	0	R/W	
1	PH1ODR	0	R/W	
0	PH0ODR	0	R/W	

Note: * Not supported in the H8S/2456 Group.

12.4.3 Example of Normal Pulse Output (Example of Five-Phase Pulse Output)

Figure 12.5 shows an example in which pulse output is used for cyclic five-phase pulse output.

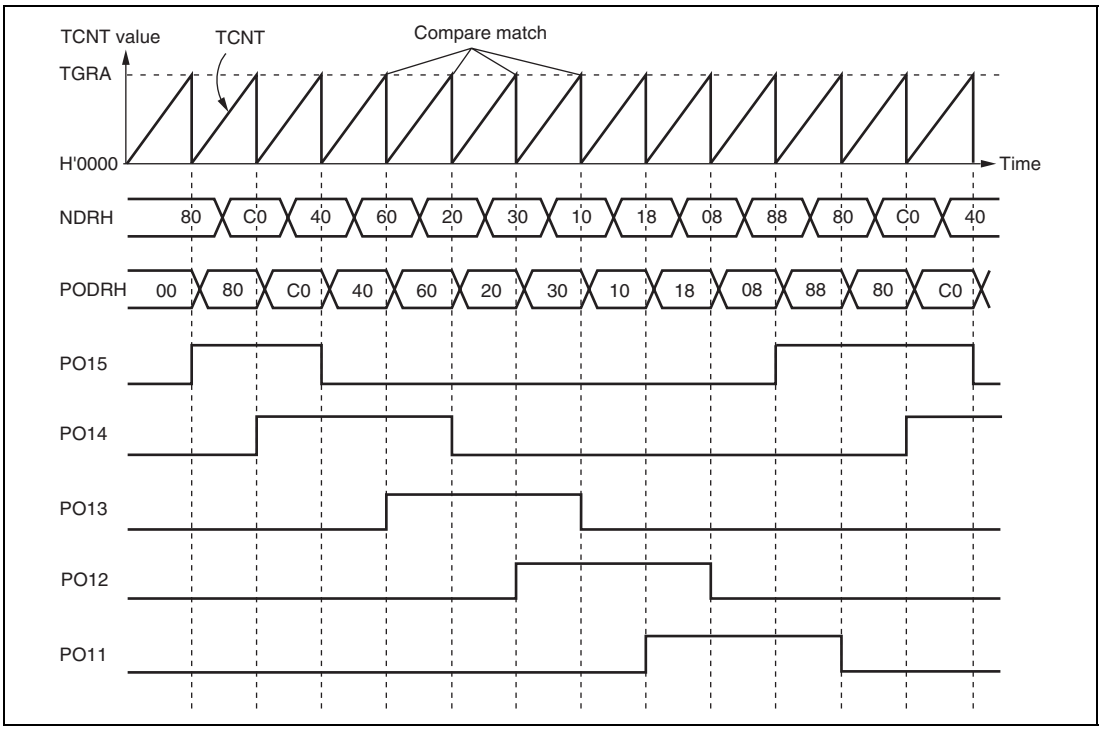

Figure 12.5 Normal Pulse Output Example (Five-Phase Pulse Output)

1. Set up TGRA in TPU which is used as the output trigger to be an output compare register. Set a cycle in TGRA so that the counter will be cleared by compare match A. Set the TGIEA bit in TIER to 1 to enable the compare match/input capture A (TGIA) interrupt.
2. Write H'F8 in P1DDR and NDERH, and set the G3CMS1, G3CMS0, G2CMS1, and G2CMS0 bits in PCR to select compare match in the TPU channel set up in the previous step to be the output trigger. Write output data H'80 in NDRH.
3. The timer counter in the TPU channel starts. When compare match A occurs, the NDRH contents are transferred to PODRH and output. The TGIA interrupt handling routine writes the next output data (H'C0) in NDRH.
4. Five-phase pulse output (one or two phases active at a time) can be obtained subsequently by writing H'40, H'60, H'20, H'30, H'10, H'18, H'08, H'88... at successive TGIA interrupts.

   If the DTC or DMAC is set for activation by the TGIA interrupt, pulse output can be obtained without imposing a load on the CPU.

15.2 Input/Output Pins

Table 15.1 shows the pin configuration of the serial communication interface.

Table 15.1 Pin Configuration

Channel	Pin Name*	I/O	Function
0	SCK0	I/O	Channel 0 clock input/output
	RxD0/IrRxD	Input	Channel 0 receive data input (normal/IrDA)
	TxD0/IrTxD	Output	Channel 0 transmit data output (normal/IrDA)
1	SCK1	I/O	Channel 1 clock input/output
	RxD1	Input	Channel 1 receive data input
	TxD1	Output	Channel 1 transmit data output
2	SCK2	I/O	Channel 2 clock input/output
	RxD2	Input	Channel 2 receive data input
	TxD2	Output	Channel 2 transmit data output
3	SCK3	I/O	Channel 3 clock input/output
	RxD3	Input	Channel 3 receive data input
	TxD3	Output	Channel 3 transmit data output
4	SCK4	I/O	Channel 4 clock input/output
	RxD4	Input	Channel 4 receive data input
	TxD4	Output	Channel 4 transmit data output

Note: * Pin names SCK, RxD, and TxD are used in the text for all channels, omitting the channel designation.

Section 16 USB Function Module (USB)

This LSI incorporates a USB function module (USB).

16.1 Features

- The protocol block conforming to USB2.0 and transceiver process USB protocol automatically.

  Automatic processing of USB standard commands for endpoint 0 (some commands and class/vendor commands require decoding and processing by firmware)
- Transfer speed: Supports full-speed (12 Mbps)
- Endpoint configuration:

Endpoint Name	Abbreviation	Transfer Type	Maximum Packet Size	FIFO Buffer Capacity (Byte)	DMA Transfer
Endpoint 0	EP0s	Setup	8	8	—
	EP0i	Control-in	16	16	—
	EP0o	Control-out	16	16	—
Endpoint 1	EP1	Bulk-out	64	128	Possible
Endpoint 2	EP2	Bulk-in	64	128	Possible
Endpoint 3	EP3	Interrupt-in	16	16	—

Configuration1-Interface0 to 3-AlternateSetting0- ◄——— EndPoint1 to 3

- Interrupt requests: Generates various interrupt signals necessary for USB transmission/reception
- Power mode: Self power mode or bus power mode can be selected by the power mode bit (PWMD) in the control register (CTLR).

Legend:

S: Start condition. The master device drives SDA from high to low while SCL is high.

SLA: Slave address

R/$\overline{W}$: Indicates the direction of data transfer: from the slave device to the master device when R/$\overline{W}$ is 1, or from the master device to the slave device when R/$\overline{W}$ is 0.

A: Acknowledge. The receiving device drives SDA to low.

DATA: Transferred data

P: Stop condition. The master device drives SDA from low to high while SCL is high.

17.4.2 Master Transmit Operation

In I²C bus format master transmit mode, the master device outputs the transmit clock and transmit data, and the slave device returns an acknowledge signal. The transmission procedure and operations in master transmit mode are described below.

1. Set the ICE bit in ICCRA to 1. Set the WAIT bit in ICMR and the CKS3 to CKS0 bits in ICCR1 to 1. (Initial setting)
2. Read the BBSY flag in ICCRB to confirm that the bus is free. Set the MST and TRS bits in ICCRA to select master transmit mode. Then, write 1 to BBSY and 0 to SCP using MOV instruction. (Start condition issued) This generates the start condition.
3. After confirming that TDRE in ICSR has been set, write the transmit data (the first byte data show the slave address and R/W) to ICDRT. After this, when TDRE is cleared to 0, data is transferred from ICDRT to ICDRS. TDRE is set again.
4. When transmission of one byte data is completed while TDRE is 1, TEND in ICSR is set to 1 at the rise of the 9th transmit clock pulse. Read the ACKBR bit in ICIER, and confirm that the slave device has been selected. Then, write second byte data to ICDRT, and clear TDRE and TEND. When ACKBR is 1, the slave device has not been acknowledged, so issue the stop condition. To issue the stop condition, write 0 to BBSY and SCP using MOV instruction. SCL is fixed low until the transmit data is prepared or the stop condition is issued.
5. The transmit data after the second byte is written to ICDRT every time TDRE is set, thus clearing TDRE.
6. Write the number of bytes to be transmitted to ICDRT. Wait until TEND is set (the end of last byte data transmission) while TDRE is 1, or wait for NACK (NACKF in ICSR = 1) from the receive device while ACKE in ICIER is 1. Then, issue the stop condition to clear TEND or NACKF.
7. When the STOP bit in ICSR is set to 1, the operation returns to the slave receive mode.

20.3.4 SS Enable Register (SSER)

SSER performs transfer/receive control of synchronous serial communication and setting of interrupt enable.

Bit	Bit Name	Initial Value	R/W	Description
7	TE	0	R/W	Transmit Enable When this bit is set to 1, transmission is enabled.
6	RE	0	R/W	Receive Enable When this bit is set to 1, reception is enabled.
5, 4	—	All 0	R/W	Reserved These bits are always read as 0. The write value should always be 0.
3	TEIE	0	R/W	Transmit End Interrupt Enable When this bit is set to 1, a TEI interrupt request is enabled.
2	TIE	0	R/W	Transmit Interrupt Enable When this bit is set to 1, a TXI interrupt request is enabled.
1	RIE	0	R/W	Receive Interrupt Enable When this bit is set to 1, an RXI interrupt request and an OEI interrupt request are enabled.
0	CEIE	0	R/W	Conflict Error Interrupt Enable When this bit is set to 1, a CEI interrupt request is enabled.

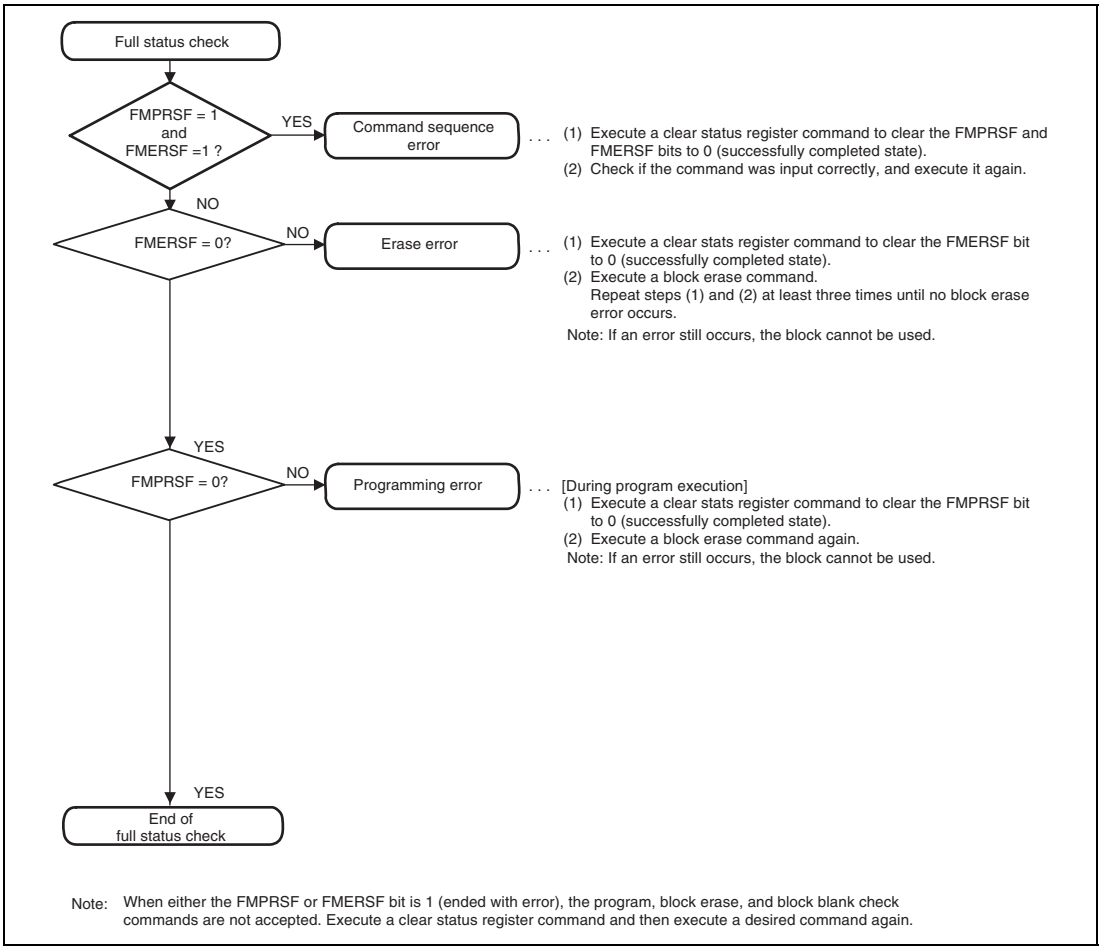

Figure 22.6 Flowchart of Full Status Check Processing and Corrective Actions for Each Error

(4) Inquiry/Selection State

The boot program returns information from the flash memory in response to the host's inquiry commands and sets the device code, clock mode, and bit rate in response to the host's selection command.

Inquiry and selection commands are listed below.

Table 22.9 Inquiry and Selection Commands

Command	Command Name	Description
H'20	Supported Device Inquiry	Inquiry regarding device codes and product name
H'10	Device Selection	Selection of device code
H'21	Clock Mode Inquiry	Inquiry regarding numbers of clock modes and values of each mode
H'11	Clock Mode Selection	Indication of the selected clock mode
H'22	Multiplication Ratio Inquiry	Inquiry regarding the number of frequency-multiplied clock types, the number of multiplication ratios, and the values of each multiple
H'23	Operating Clock Frequency Inquiry	Inquiry regarding the maximum and minimum values of the main clock and peripheral clocks
H'25	User ROM Information Inquiry	Inquiry regarding the number of user ROMs and the start and last addresses of each ROM
H'26	Erased Block Information Inquiry	Inquiry regarding the number of blocks and the start and last addresses of each block
H'27	Programming Unit Inquiry	Inquiry regarding the unit of programming data
H'3F	New Bit Rate Selection	Selection of new bit rate
H'40	Transition to Programming/Erasing State	Erasing of user ROM and entry to programming/erasing state
H'4F	Boot Program Status Inquiry	Inquiry regarding the operated status of the boot program

Section 23 Clock Pulse Generator

This LSI has an on-chip clock pulse generator (CPG) that generates the system clock (φ) and internal clocks. The clock pulse generator consists of an oscillator circuit, a system-clock PLL circuit and a divider.

Figure 23.1 shows a block diagram of the clock pulse generator.

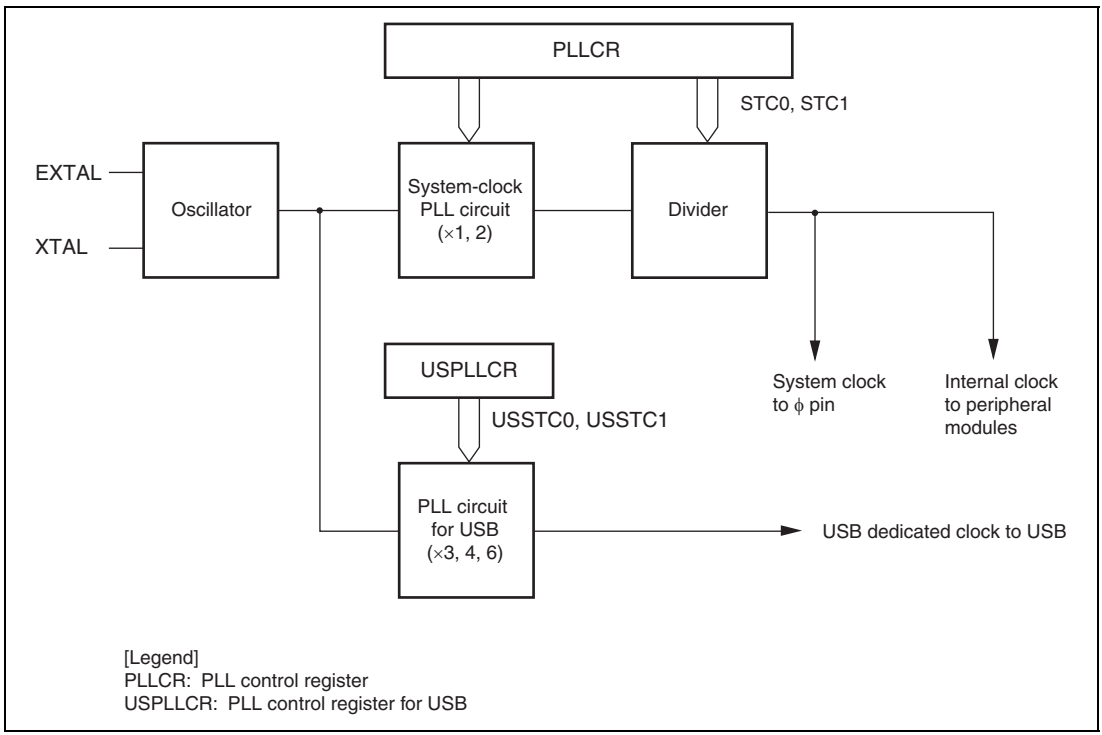

Figure 23.1 Block Diagram of Clock Pulse Generator

The frequency of the system clock from the oscillator can be changed by means of the system-clock PLL circuit and divider. Frequency changes are made by software by means of settings in the PLL control register (PLLCR).

The USB module requires a 48-MHz clock. Set the frequency of the USB dedicated clock (cku toe 48 MHz. Changes to the frequency of the USB dedicated clock are made by software by means of settings in the USB PLL control register (USPLLCR).

Table 26.18 DC Characteristics (2)

Conditions: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, $V_{SS} = AV_{SS}$ = 0 V*1

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Three-state leakage current (off state)	Ports 1 to 3, P50 to P53, Ports 8, Ports A to G	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0.5 to V_{CC} –0.5 V
Input pull-up MOS current	Ports A to E	$-I_p$	10	—	300	µA	V_{CC} = 3.0 to 3.6 V V_{in} = 0 V
Input capacitance	$\overline{RES}$	C_{in}	—	—	30	pF	V_{in} = 0 V
	NMI		—	—	30	pF	f = 1 MHz
	All input pins except $\overline{RES}$ and NMI		—	—	18	pF	T_a = 25°C
Supply current*2	Normal operation	I_{CC}*4	—	45 (3.3 V)	60	mA	f = 33 MHz
	Sleep mode		—	35 (3.3 V)	45	mA	f = 33 MHz
	Standby mode*3		—	20	80	µA	$T_a \leq$ 50°C
			—	80	500	µA	50°C < T_a
Analog power supply current	During A/D and D/A conversion	AI_{CC}	—	0.5 (3.3 V)	2.0	mA	When channel 1 is in use
	Idling		—	0.01	5.0	µA	When channel 1 is in use
Reference power supply current	During A/D and D/A conversion	AI_{CC}	—	0.5 (3.3 V)	1.0	mA	
	Idling		—	0.01	5.0	µA	
RAM standby voltage		V_{RAM}	2.5	—	—	V	
V_{CC} start voltage*5		$V_{CC\ start}$	—	—	0.3	V	
V_{CC} rising slope*5		SV_{CC}	—	—	20	ms/V	

Notes: 1. When the A/D and D/A converters are not used, the AV_{CC}, V_{ref}, and AV_{SS} pins should not be open. Connect the AV_{CC} and V_{ref} pins to V_{CC}, and the AV_{SS} pin to V_{SS}.

2. Supply current values are for V_{IH}min = V_{CC} –0.2 V and V_{IL}max = 0.2 V with all output pins unloaded and all input pull-up MOSs in the off state.

Table 26.28 USB PLL Characteristics

Conditions: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0V, EXTAL = 8 to 16 MHz

Item	Symbol	Min	Max	Unit	Test Conditions
PLL for USB: oscillation stabilization time	t_{USOSC}	1	—	ms	Figure 26.38

26.2.7 Flash Memory Characteristics

Table 26.29 Flash Memory Characteristics

Conditions: V_{CC} = 3.0 to 3.6V, AV_{CC} = 3.0 to 3.6V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0V, ϕ = 8 MHz to 33 MHz

		Standard value			
Item	Applicable area	Min.	Typ.	Max.	Unit
Programming and erase count*1	User ROM	1000*2	—	—	Times
	Data flash area	10000*2	—	—	
Programming time (per 4 bytes)	User ROM	—	150	4000	µs
	Data flash area	—	300	4000	
Erase time (per 1 block)	User ROM	—	300	3000	ms
	Data flash area	—	300	3000	
Programming and erase voltage	User ROM	3.0	—	3.6	V
	Data flash area				
Read voltage	User ROM	3.0	—	3.6	V
	Data flash area				
Access state	User ROM	1	—	—	State
	Data flash area	2	—	—	

Notes: 1. In the system where multiple programming are executed, erase once so as to effectively diminish the programming times after having written with leaving the blank area as least as possible by shifting writing address one by one.

For example, if 16 bytes per 1 set is being programmed, erase once after maximum 256 sets of programming has been done, which diminish the effective programming times.

Keep the information of the times of erasure and set up the limitation times is recommended.

2. If an erase error is occurred, execute the clear status command -> erase command for at least 3 times until no erase error is occurred.

Item	Page	Revision (See Manual for Details)
• PF2/$\overline{\text{LCAS}}$/DQML*[6]/ $\overline{\text{IRQ15-A}}$/SSI0-C (H8S/2456 Group and H8S/2456R Group) • Modes 3 and 7 (EXPE = 0)	659	Notes amended 2. When using as SSI0-C input, set SSI0S1 and SSI0S0 in PFCR5 to B'10 before other register setting. 3. When using as SSI0-C output, set SSI0S1 and SSI0S0 in PFCR5 to B'10 before other register setting.
• PF2/$\overline{\text{CS6}}$/$\overline{\text{LCAS}}$/SSI 0-C (H8S/2454 Group) • Modes 3 and 7 (EXPE = 0)	661	Notes amended 1. When using as SSI0-C input, set SSI0S1 and SSI0S0 in PFCR5 to B'10 before other register setting. 2. When using as SSI0-C output, set SSI0S1 and SSI0S0 in PFCR5 to B'10 before other register setting.
• PF1/$\overline{\text{UCAS}}$/DQMU*[6]/ $\overline{\text{IRQ14-A}}$/SSCK0-C (H8S/2456 Group and H8S/2456R Group) • Modes 3 and 7 (EXPE = 0)	662	Notes amended 2. When using as SSCK0-C input, set SSCK0S1 and SSCK0S0 in PFCR5 to B'10 before other register setting. 3. When using as SSCK0-C output, set SSCK0S1 and SSCK0S0 in PFCR5 to B'10 before other register setting.
• PF1/$\overline{\text{CS5}}$/$\overline{\text{UCAS}}$/ SSCK0-C (H8S/2454 Group) • Modes 3 and 7 (EXPE = 0)	663	Notes amended 1. When using as SSCK0-C input, set SSCK0S1 and SSCK0S0 in PFCR5 to B'10 before other register setting. 2. When using as SSCK0-C output, set SSCK0S1 and SSCK0S0 in PFCR5 to B'10 before other register setting.
• PF0/$\overline{\text{WAIT-A}}$/ $\overline{\text{ADTRG0-B}}$/$\overline{\text{SCS0-C}}$ (H8S/2456 Group and H8S/2456R Group) • Modes 3 and 7 (EXPE = 0)	665	Notes amended 2. When using as $\overline{\text{SCS0-C}}$ input, set SCS0S1 and SCS0S0 in PFCR5 to B'10 before other register setting. 3. When using as $\overline{\text{SCS0-C}}$ output, set SCS0S1 and SCS0S0 in PFCR5 to B'10 before other register setting. 4. When using as $\overline{\text{SCS0-C}}$ input/output, set SCS0S1 and SCS0S0 in PFCR5 to B'10 before other register setting.