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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	H8S/2600
Core Size	16-Bit
Speed	32MHz
Connectivity	EBI/EMI, I²C, IrDA, SCI, SSU, UART/USART, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	96
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b; D/A 2x8b
Oscillator Type	External
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r4f24568nvrfqv

Bit	Bit Name	Initial Value	R/W	Description
9	IRQ4SCB	0	R/W	IRQ4 Sense Control B
8	IRQ4SCA	0	R/W	IRQ4 Sense Control A 00: Interrupt request generated at $\overline{\text{IRQ4}}$ input low level 01: Interrupt request generated at falling edge of $\overline{\text{IRQ4}}$ input 10: Interrupt request generated at rising edge of $\overline{\text{IRQ4}}$ input 11: Interrupt request generated at both falling and rising edges of $\overline{\text{IRQ4}}$ input
7	IRQ3SCB	0	R/W	IRQ3 Sense Control B
6	IRQ3SCA	0	R/W	IRQ3 Sense Control A 00: Interrupt request generated at $\overline{\text{IRQ3}}$ input low level 01: Interrupt request generated at falling edge of $\overline{\text{IRQ3}}$ input 10: Interrupt request generated at rising edge of $\overline{\text{IRQ3}}$ input 11: Interrupt request generated at both falling and rising edges of $\overline{\text{IRQ3}}$ input
5	IRQ2SCB	0	R/W	IRQ2 Sense Control B
4	IRQ2SCA	0	R/W	IRQ2 Sense Control A 00: Interrupt request generated at $\overline{\text{IRQ2}}$ input low level 01: Interrupt request generated at falling edge of $\overline{\text{IRQ2}}$ input 10: Interrupt request generated at rising edge of $\overline{\text{IRQ2}}$ input 11: Interrupt request generated at both falling and rising edges of $\overline{\text{IRQ2}}$ input

6.4.2 Bus Specifications

The external address space bus specifications consist of five elements: bus width, number of access states, number of program wait states, read strobe timing, and chip select ($\overline{CS}$) assertion period extension states. The bus width and number of access states for on-chip memory and internal I/O registers are fixed, and are not affected by the bus controller.

(1) Bus Width

A bus width of 8 or 16 bits can be selected with ABWCR. An area for which an 8-bit bus is selected functions as an 8-bit access space, and an area for which a 16-bit bus is selected functions as a 16-bit access space. If all areas are designated as 8-bit access space, 8-bit bus mode is set; if any area is designated as 16-bit access space, 16-bit bus mode is set.

(2) Number of Access States

Two or three access states can be selected with ASTCR. An area for which 2-state access is selected functions as a 2-state access space, and an area for which 3-state access is selected functions as a 3-state access space. With the DRAM or synchronous DRAM interface and burst ROM interface, the number of access states may be determined without regard to the setting of ASTCR.

When 2-state access space is designated, wait insertion is disabled. When 3-state access space is designated, it is possible to insert program waits by means of the WTCRA and WTCRB, and external waits by means of the $\overline{WAIT}$ pin.

Note: The synchronous DRAM interface is not supported by the H8S/2456 Group and H8S/2454 Group.

(3) Number of Program Wait States

When 3-state access space is designated by ASTCR, the number of program wait states to be inserted automatically is selected with WTCRA and WTCRB. From 0 to 7 program wait states can be selected. Table 6.2 shows the bus specifications (bus width, and number of access states and program wait states) for each basic bus interface area.

(2) 8-Bit, 3-State Access Space

Figure 6.11 shows the bus timing for an 8-bit, 3-state access space. When an 8-bit access space is accessed, the upper half (D15 to D8) of the data bus is used. The $\overline{\text{LWR}}$ pin is always fixed high. Wait states can be inserted.

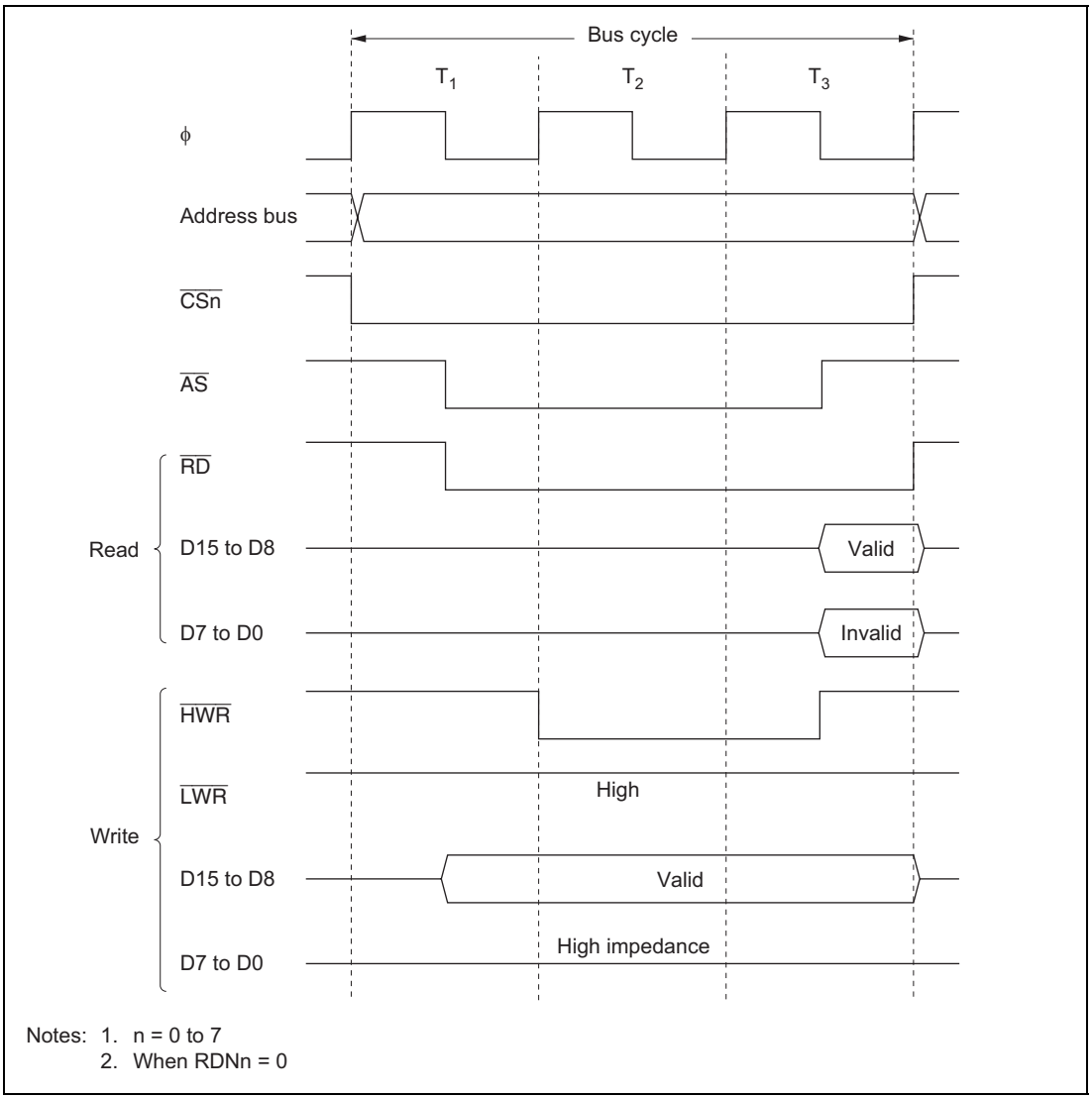


Figure 6.11 Bus Timing for 8-Bit, 3-State Access Space

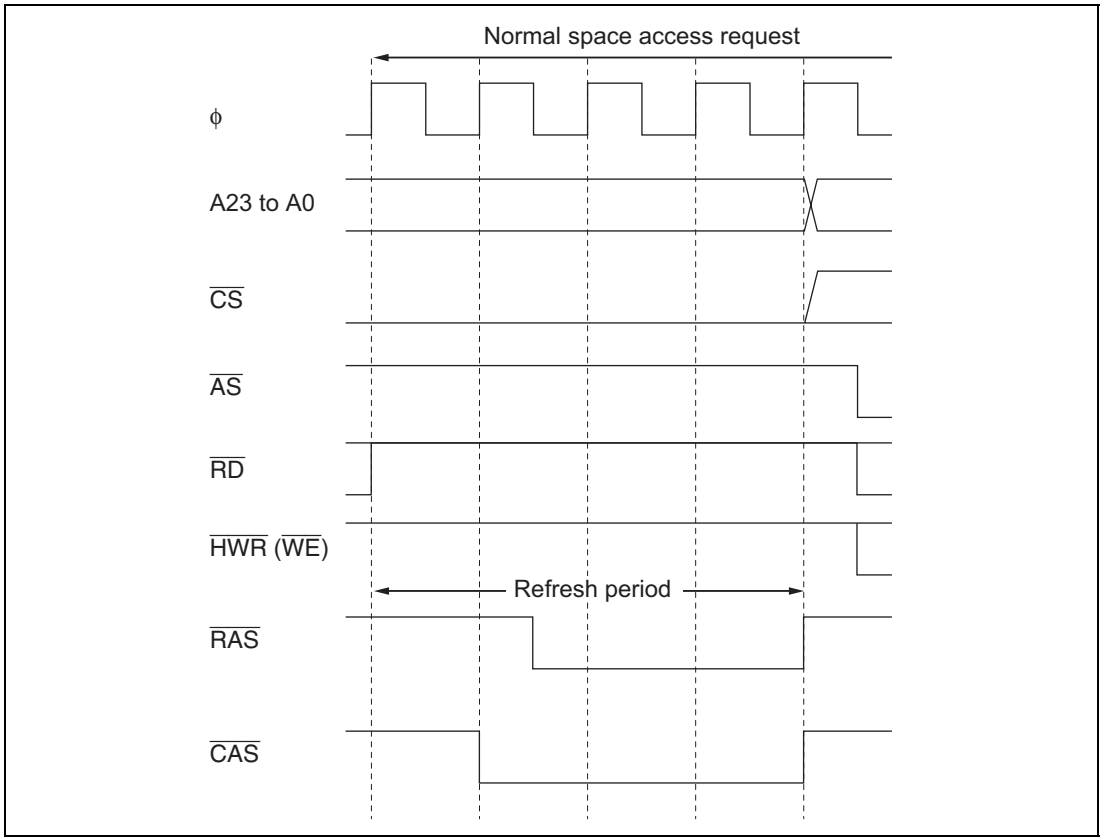


Figure 6.50 Example of CBR Refresh Timing (CBRM = 1)

6.13 Bus Arbitration

This LSI has a bus arbiter that arbitrates bus mastership operations (bus arbitration).

There are four bus masters—the CPU, DTC, DMAC, and EXDMAC*—that perform read/write operations when they have possession of the bus. Each bus master requests the bus by means of a bus request signal. The bus arbiter determines priorities at the prescribed timing, and permits use of the bus by means of a bus request acknowledge signal. The selected bus master then takes possession of the bus and begins its operation.

Note: * The EXDMAC is not supported by the H8S/2454 Group.

6.13.1 Operation

The bus arbiter detects the bus masters' bus request signals, and if the bus is requested, sends a bus request acknowledge signal to the bus master. If there are bus requests from more than one bus master, the bus request acknowledge signal is sent to the one with the highest priority. When a bus master receives the bus request acknowledge signal, it takes possession of the bus until that signal is canceled.

The order of priority of the bus mastership is as follows:

(High) EXDMAC* > DMAC > DTC > CPU (Low)

An internal bus access by internal bus masters except the EXDMAC* and external bus release, a refresh when the CBRM bit is 0, and an external bus access by the EXDMAC* can be executed in parallel.

If an external bus release request, a refresh request, and an external access by an internal bus master occur simultaneously, the order of priority is as follows:

(High) Refresh > EXDMAC* > External bus release (Low)

(High) External bus release > External access by internal bus master except EXDMAC* (Low)

As a refresh when the CBRM bit in REFCR is cleared to 0 and an external access other than to DRAM space by an internal bus master can be executed simultaneously, there is no relative order of priority for these two operations.

Note: * The EXDMAC is not supported by the H8S/2454 Group.

Bit	Bit Name	Initial Value	R/W	Description
12	SAE0	0	R/W	Single Address Enable 0 Specifies whether channel 0B is to be used for transfer in dual address mode or single address mode. This bit is invalid in full address mode. 0: Dual address mode 1: Single address mode
11	DTA1B	0	R/W	Data Transfer Acknowledge 1B
10	DTA1A	0	R/W	Data Transfer Acknowledge 1A
9	DTA0B	0	R/W	Data Transfer Acknowledge 0B
8	DTA0A	0	R/W	Data Transfer Acknowledge 0A These bits enable or disable clearing when DMA transfer is performed for the internal interrupt source selected by the DTF3 to DTF0 bits in DMACR. If the DTA bit is set to 1 when DTE = 1, the internal interrupt source is cleared automatically by DMA transfer. When DTE = 1 and DTA = 1, the internal interrupt source does not issue an interrupt request to the CPU or DTC. If the DTA bit is cleared to 0 when DTE = 1, the internal interrupt source is not cleared when a transfer is performed, and can issue an interrupt request to the CPU or DTC in parallel. In this case, the interrupt source should be cleared by the CPU or DTC transfer. When DTE = 0, the internal interrupt source issues an interrupt request to the CPU or DTC regardless of the DTA bit setting.

(2) Burst Mode

In burst mode, once the EXDMAC acquires the bus it continues transferring data, without releasing the bus, until the transfer end condition is satisfied. There is no burst mode in external request mode.

In burst mode, once transfer is started it is not interrupted even if there is a transfer request from another channel with higher priority. When the burst mode channel finishes its transfer, it releases the bus in the next cycle in the same way as in cycle steal mode.

When the EDA bit is cleared to 0 in EDMDR, EXDMA transfer is halted. However, EXDMA transfer is executed for all transfer requests generated within the EXDMAC up until the EDA bit was cleared to 0.

If a repeat area overflow interrupt is generated, the EDA bit is cleared to 0 and transfer is terminated.

When the BGUP bit is set to 1 in EDMDR, the bus is released if a bus request is issued by another bus master during burst transfer. If there is no bus request, burst transfer is executed even if the BGUP bit is set to 1.

Figure 8.6 shows examples of the timing in burst mode.

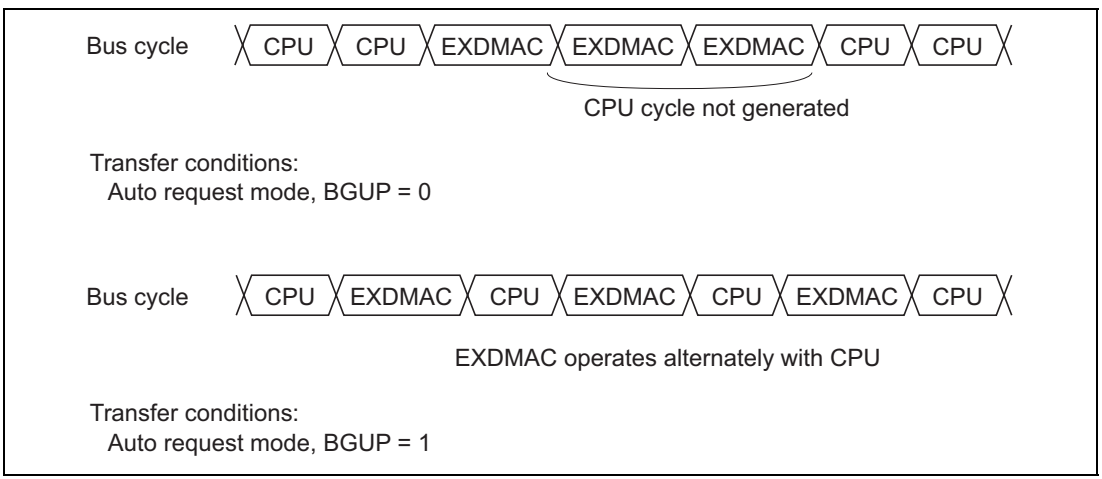


Figure 8.6 Examples of Timing in Burst Mode

- PB3/A11/TIOCD6/TCLKF

  The pin function is switched as shown below according to the combination of the operating mode, bit EXPE, TPU channel 6 settings (by bits MD3 to MD0 in TMDR_6, bits IOD3 to IOD0 in TIORL_6, and bits CCLR2 to CCLR0 in TCR_6), bits TPSC2 to TPSC0 in TCR_6 to TCR_8, and bit PB3DDR.

Operating mode	1, 2	4 3, 7 (EXPE = 1)		3, 7 (EXPE = 0)		
TPU channel 6 settings	—	—		(1) in table below	(2) in table below	
PB3DDR	—	0	1	—	0	1
Pin function	A11 output	PB3 input	A11 output	TIOCD6 output	PB3 input	PB3 output
					TIOCD6 input*1	
				TCLKF input*2		

TPU channel 6 settings	(2)	(1)	(2)	(2)	(1)	(2)
MD3 to MD0	B'0000		B'0010	B'0011		
IOD3 to IOD0	B'0000, B'0100, B'1xxx	B'0001 to B'0011, B'0101 to B'0111	—	B'xx00	Other than B'××00	
CCLR2 to CCLR0	—	—	—	—	Other than B'110	B'110
Output function	—	Output compare output	—	—	PWM mode 2 output	—

[Legend]

x: Don't care

Notes: 1. TIOCD6 input when MD3 to MD0 = B'0000 and IOD3 to IOD0 = B'10xx.

2. TCLKF input when the setting for any of TCR_6 to TCR_8 is TPSC2 to TPSC0 = B'101. TCLKF input when phase counting mode is set for channels 7 and 11.

10.13.6 Pin Functions

Port E pins also function as the pins for data I/Os and address outputs. The correspondence between the register specification and the pin functions is shown below.

- PE7/D7/AD7, PE6/D6/AD6, PE5/D5/AD5, PE4/D4/AD4, PE3/D3/AD3, PE2/D2/AD2, PE1/D1/AD1, PE0/D0/AD0

  The pin function is switched as shown below according to the combination of the operating mode, bus mode, bit EXPE, bit MPXE in MPXCR of the bus controller, and bit PEnDDR.

Operating mode	1, 2, 4				3, 7					
Bus mode	All areas are 8-bit space		At least one area is 16-bit space		—		All areas are 8-bit space		At least one area is 16-bit space	
EXPE	—		—		0		1		1	
MPXE	—		0	1	—		—		0	1
PEnDDR	0	1	—		0	1	0	1	—	
Pin function	PEn input	PEn output	Data I/O	Address output/ data I/O	PEn input	PEn output	PEn input	PEn output	Data I/O	Address output/ data I/O

[Legend]
n = 7 to 0

SSU settings	(1)	(2)	(1)	(3)	(1)	(2)	(1)	(3)
SSUMS	0				1			
MSS	0		1		0		1	
SCKS	0	1	0	1	0	1	0	1
Pin state	—	SSCK input	—	SSCK output	—	SSCK input	—	SSCK output

[Legend]

—: Not used as the SSU pin (can be used as an I/O port).

Note: See tables 20.4 to 20.6.

- PF0/$\overline{\text{WAIT-A}}$/$\overline{\text{ADTRG0-B}}$/$\overline{\text{SCS0-C}}$ (H8S/2456 Group and H8S/2456R Group)

  The pin function is switched as shown below according to the combination of the operating mode, bit EXPE, bit WAITE in BCR of the bus controller, bits MSS, CSS1, and CSS0 in SSCRH and bit SSUMS in SSCRL of SSU, bits TRGS1, TRGS0, and EXTRGS in ADCR_0 of ADC, bits ADTRG0S and WAITS in PFCR4, bits SCS0S1 and SCS0S0 in PFCR5, and bit PF0DDR.

- Modes 1, 2, and 4 Modes 3 and 7 (EXPE = 1)

WAITE	0				
WAITS	—				
SSU settings	(1) in table below		(2) in table below	(4) in table below	(3) in table below
PF0DDR	0	1	0*5	0*5	—
Pin function	PF0 input	PF0 output	$\overline{\text{SCS0-C}}$ input*2*6	$\overline{\text{SCS0-C}}$ I/O*4*6	$\overline{\text{SCS0-C}}$ output*3*6
	$\overline{\text{ADTRG0-B}}$ input*1				

WAITE	1					
WAITS	0	1				
SSU settings	—	(1) in table below	(2) in table below	(4) in table below	(3) in table below	—
PF0DDR	—	0	0*5	0	0	1
Pin function	$\overline{\text{WAIT-A}}$ input	PF0 input	$\overline{\text{SCS0-C}}$ input*2*6	Setting prohibited	Setting prohibited	Setting prohibited
	$\overline{\text{ADTRG0-B}}$ input*1					

10.18.2 Port Function Control Register 1 (PFCR1)

PFCR1 enables or disables address output (A23 to A16).

Bits 7 to 5 are valid in modes 1 and 2 and all the bits are valid in modes 4 and 7.

Bit	Bit Name	Initial Value	R/W	Description
7	A23E	1	R/W	Address 23 Enable Enables or disables output for address output 23 (A23). 0: DR output when PA7DDR = 1 1: A23 output when PA7DDR = 1
6	A22E	1	R/W	Address 22 Enable Enables or disables output for address output 22 (A22). 0: DR output when PA6DDR = 1 1: A22 output when PA6DDR = 1
5	A21E	1	R/W	Address 21 Enable Enables or disables output for address output 21 (A21). 0: DR output when PA5DDR = 1 1: A21 output when PA5DDR = 1
4	A20E	1	R/W	Address 20 Enable Enables or disables output for address output 20 (A20). 0: DR output when PA4DDR = 1 1: A20 output when PA4DDR = 1
3	A19E	1	R/W	Address 19 Enable Enables or disables output for address output 19 (A19). 0: DR output when PA3DDR = 1 1: A19 output when PA3DDR = 1
2	A18E	1	R/W	Address 18 Enable Enables or disables output for address output 18 (A18). 0: DR output when PA2DDR = 1 1: A18 output when PA2DDR = 1

Table 11.12 MD3 to MD0

Bit 3 MD3*1	Bit 2 MD2*2	Bit 1 MD1	Bit 0 MD0	Description
0	0	0	0	Normal operation
			1	Reserved
		1	0	PWM mode 1
			1	PWM mode 2
	1	0	0	Phase counting mode 1
			1	Phase counting mode 2
		1	0	Phase counting mode 3
			1	Phase counting mode 4
1	x	x	x	—

[Legend]

x: Don't care

Notes: 1. MD3 is a reserved bit. In a write, it should always be written with 0.

2. Phase counting mode cannot be set for channels 0 and 3. In this case, 0 should always be written to MD2.

11.6 DTC Activation

The DTC can be activated by the TGR input capture/compare match interrupt for a channel. For details, see section 9, Data Transfer Controller (DTC).

A total of 32 TPU input capture/compare match interrupts can be used as DTC activation sources, four each for channels 0, 3, 6, and 9, and two each for channels 1, 2, 4, 5, 7, 8, 10, and 11.

11.7 DMAC Activation

In unit 0 of the TPU, the DMAC can be activated by the TGRA input capture/compare match interrupt for a channel. For details, see section 7, DMA Controller (DMAC). (The DMAC cannot be activated by unit 1.)

In unit 0 of the TPU, a total of six TGRA input capture/compare match interrupts can be used as DMAC activation sources, one for each channel.

11.8 A/D Converter Activation

The A/D converter can be activated by the TGRA input capture/compare match for a channel.

If the TTGE bit in TIER is set to 1 when the TGFA flag in TSR is set to 1 by the occurrence of a TGRA input capture/compare match on a particular channel, a request to start A/D conversion is sent to the A/D converter. If the TPU conversion start trigger has been selected on the A/D converter side at this time, A/D conversion is started.

In the TPU, a total of 12 TGRA input capture/compare match interrupts can be used as A/D converter conversion start sources, one for each channel.

11.10.9 Contention between TGR Write and Input Capture

If the input capture signal is generated in the T_2 state of a TGR write cycle, the input capture operation takes precedence and the write to TGR is not performed.

Figure 11.51 shows the timing in this case.

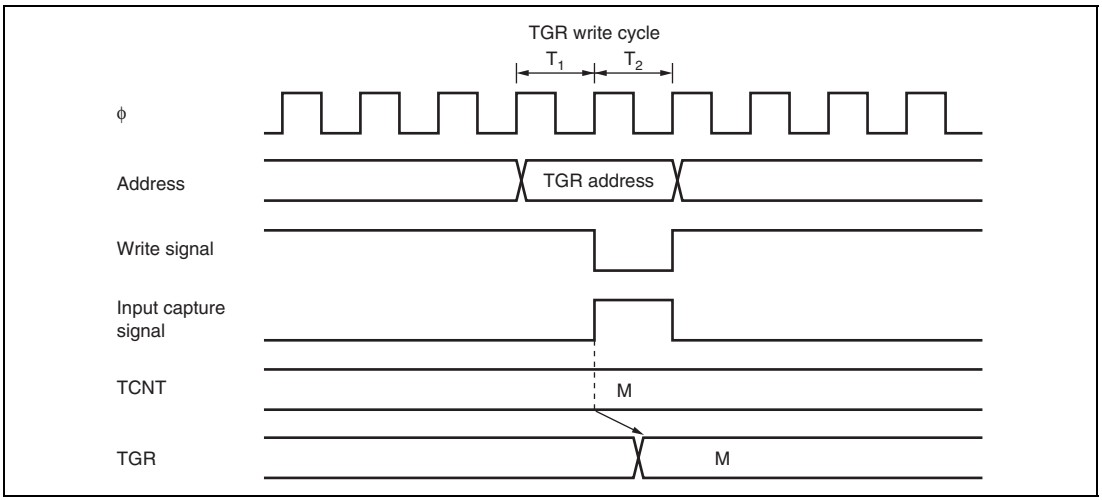


Figure 11.51 Contention between TGR Write and Input Capture

12.4.8 Pulse Output Triggered by Input Capture

Pulse output can be triggered by TPU input capture as well as by compare match. If TGRA functions as an input capture register in the TPU channel selected by PCR, pulse output will be triggered by the input capture signal.

Figure 12.11 shows the timing of this output.

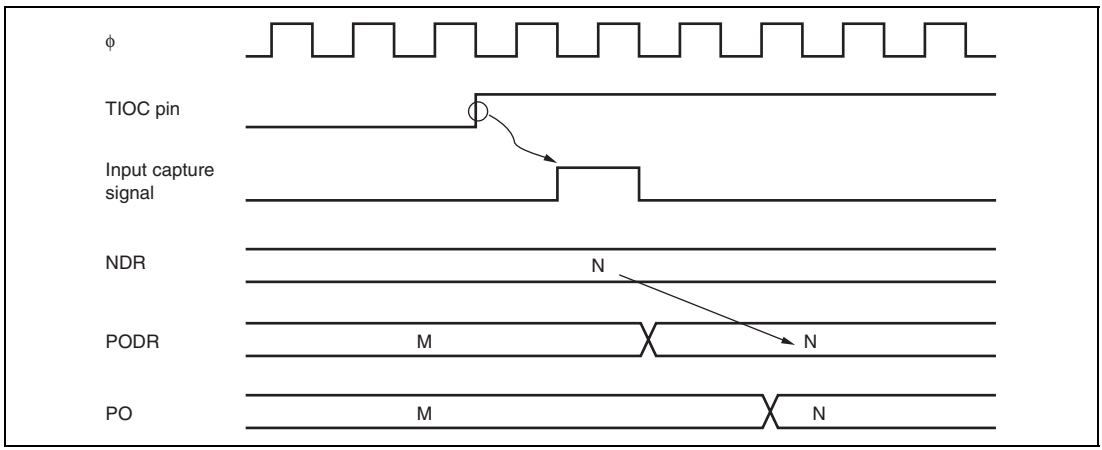
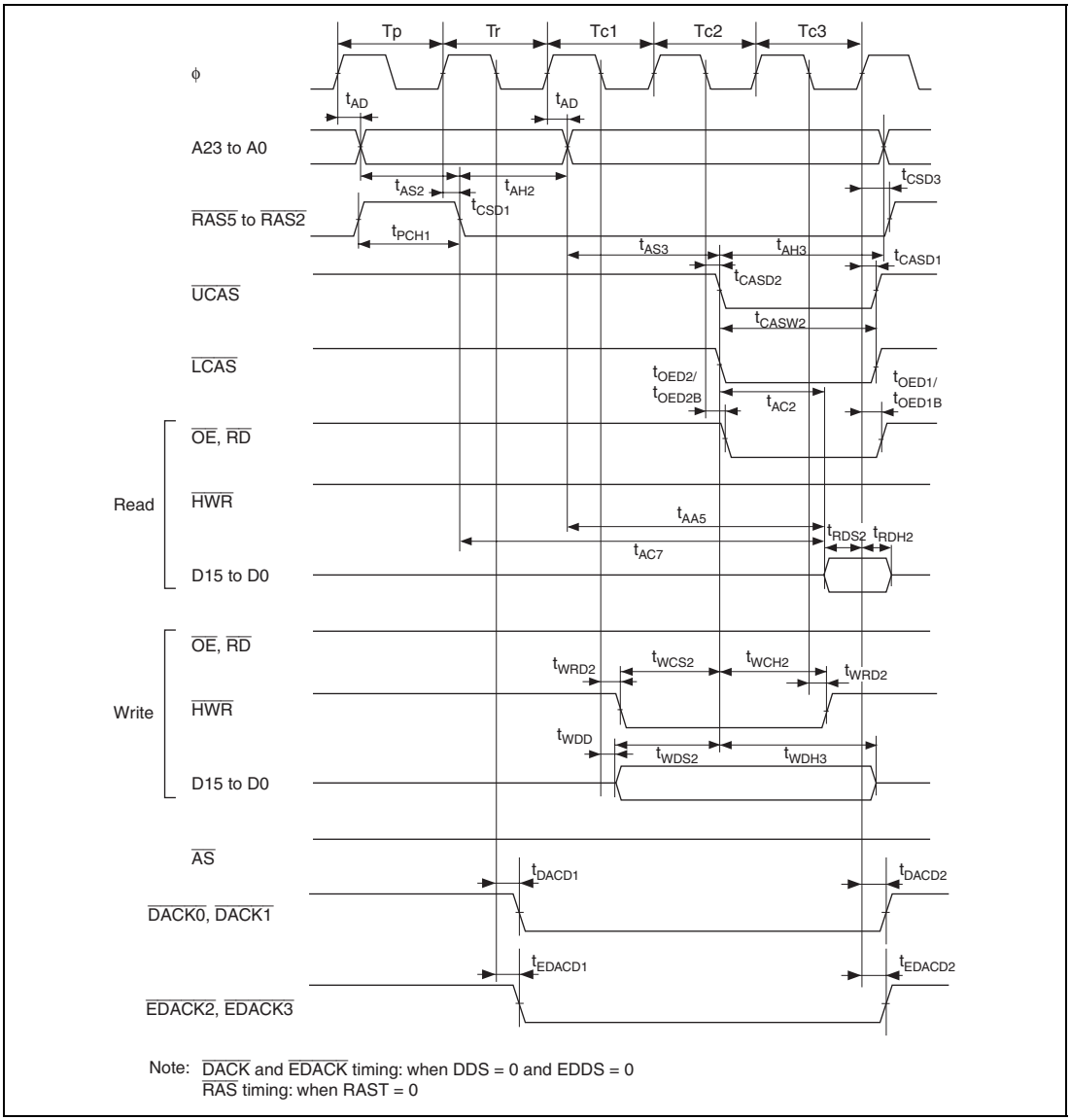


Figure 12.11 Pulse Output Triggered by Input Capture (Example)

17.3.2 I²C Bus Control Register B (ICCRB)

ICCRB is an 8-bit readable/writable register that issues start/stop conditions, manipulates the SDA pin, monitors the SCL pin, and controls reset in I²C control.

Bit	Bit Name	Initial Value	R/W	Description
7	BBSY	0	R/W	Bus Busy This bit enables to confirm whether the I²C bus is occupied or released and to issue start and stop conditions in master mode. This bit is set to 1 when the SDA level changes from high to low under the condition of SCL = high, assuming that the start condition has been issued. This bit is cleared to 0 when the SDA level changes from low to high under the condition of SCL = high, assuming that the stop condition has been issued. Write 1 to BBSY and 0 to SCP to issue a start condition. Follow this procedure when also re-transmitting a start condition. Write 0 to BBSY and 0 to SCP to issue a stop condition. To issue a start/stop condition, use the MOV instruction.
6	SCP	1	R/W	Start Condition/Stop Condition Prohibit The SCP bit controls the issue of start/stop conditions in master mode. To issue a start condition, write 1 in BBSY and 0 in SCP. A retransmit start condition is issued in the same way. To issue a stop condition, write 0 in BBSY and 0 in SCP. This bit is always read as 1. If 1 is written, the data is not stored.
5	SDAO	1	R	This bit monitors SDA output level. When reading and SDA0 is 1, the SDA pin outputs high. When reading and SDA0 is 0, the SDA pin outputs low. The write value should always be 1.
4	—	1	R/W	Reserved The write value should always be 1.
3	SCLO	1	R	This bit monitors SCL output level. When reading and SCLO is 1, the SCL pin outputs high. When reading and SCLO is 0, the SCL pin outputs low.
2	—	1	—	Reserved This bit is always read as 1.



Note: DACK and EDACK timing: when DDS = 0 and EDDS = 0
RAS timing: when RAST = 0

Figure 26.18 DRAM Access Timing: Three-State Access (RAST = 1)

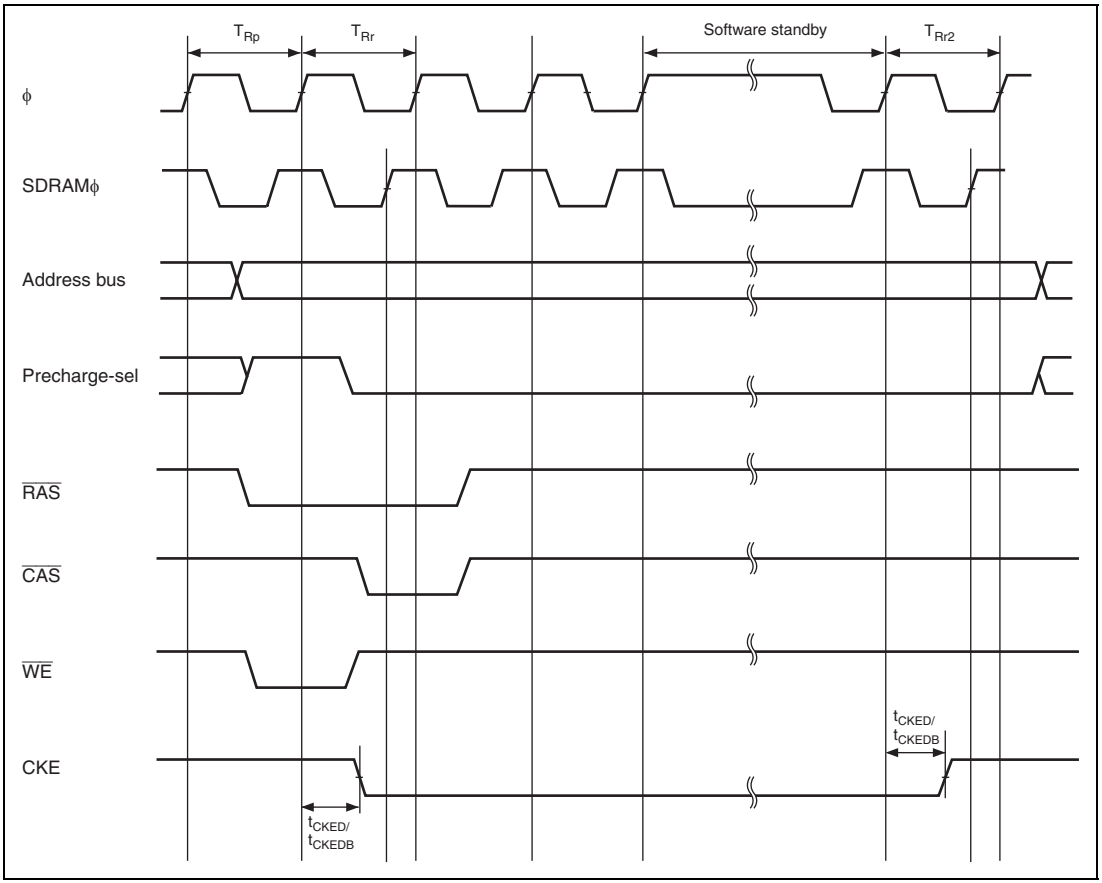


Figure 26.27 Synchronous DRAM Self-Refresh Timing

Port Name Pin Name	MCU Operating Mode	Reset	Hardware Standby Mode	Software Standby Mode	Bus Release State	Program Execution State Sleep Mode
PG3/$\overline{CS3}$/ $\overline{RAS3}$ PG2/$\overline{CS2}$/ $\overline{RAS2}$ PG1/$\overline{CS1}$	1, 2, 3, 4, 7	T	T	[$\overline{CS}$ output, OPE = 0] T [$\overline{CS}$ output, OPE = 1] H [Other than the above] Keep	[$\overline{CS}$ output] T [Other than the above] Keep	[$\overline{CS}$ output] $\overline{CS}$ [Other than the above] I/O port
PG0/$\overline{CS0}$	1, 2	H	T	[$\overline{CS}$ output, OPE = 0] T [$\overline{CS}$ output, OPE = 1] H [Other than the above] Keep	[$\overline{CS}$ output] T [Other than the above] Keep	[$\overline{CS}$ output] $\overline{CS}$ [Other than the above] I/O port
	3, 4, 7	T				
$\overline{WDTOVF}$	1, 2, 3, 4, 7	H	H	H	H	H*
USD+, USD–	1, 2, 3, 4, 7	T	T	T	Keep	USD+, USD–

[Legend]

H: High-level

L: Low-level

Keep: Input ports become high-impedance, and output ports retain their state.

T: High-impedance

DDR: Data direction register

OPE: Output port enable

Note: * Low output if a watchdog timer overflow occurs when WT/$\overline{IT}$ is 1.

Main Revisions and Additions in this Edition

<table>
<tr><th>Item</th><th>Page</th><th>Revision (See Manual for Details)</th></tr>
<tr><td>4.3 Reset</td><td>100</td><td>Amended
A reset has the highest exception priority. When the $\overline{\text{RES}}$ pin goes low, all processing halts and this LSI enters the reset. To ensure that this LSI is reset, hold the $\overline{\text{RES}}$ pin low for at least 15 ms at power-up. To reset this LSI during operation, hold the $\overline{\text{RES}}$ pin low for at least 2 ms.</td></tr>
<tr><td>7.1 Features</td><td>321</td><td>Amended
• Activation sources: internal interrupt, external request, auto-request (depending on transfer mode)
— Six compare match/input capture interrupts of 16-bit timer-pulse unit (TPU0 to TPU5)
— Transmit data empty and receive data full interrupts of serial communication interface (SCI_0, SCI_1)</td></tr>
<tr><td>7.3.4 DMA Control Registers (DMACRA and DMACRB)
(1) Short Address Mode:
• DMACR_0A, DMACR_0B, DMACR_1A, and DMARC_1B</td><td>331, 332</td><td>Amended
<table>
<tr><th>Bit</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>3</td><td>DTF3</td><td>• Channel A</td></tr>
<tr><td>2</td><td>DTF2</td><td>0100: Activated by SCI channel 0 transmit data empty interrupt</td></tr>
<tr><td>1</td><td>DTF1</td><td>0101: Activated by SCI channel 0 receive data full interrupt</td></tr>
<tr><td>0</td><td>DTF0</td><td>0110: Activated by SCI channel 1 transmit data empty interrupt</td></tr>
<tr><td></td><td></td><td>0111: Activated by SCI channel 1 receive data full interrupt</td></tr>
<tr><td></td><td></td><td>• Channel B</td></tr>
<tr><td></td><td></td><td>0100: Activated by SCI channel 0 transmit data empty interrupt</td></tr>
<tr><td></td><td></td><td>0101: Activated by SCI channel 0 receive data full interrupt</td></tr>
<tr><td></td><td></td><td>0110: Activated by SCI channel 1 transmit data empty interrupt</td></tr>
<tr><td></td><td></td><td>0111: Activated by SCI channel 1 receive data full interrupt</td></tr>
</table></td></tr>
<tr><td>(2) Full Address Mode
• DMACR_0B and DMACR_1B</td><td>336</td><td>Amended
<table>
<tr><th>Bit</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>3</td><td>DTF3</td><td>• Block Transfer Mode</td></tr>
<tr><td>2</td><td>DTF2</td><td>0100: Activated by SCI channel 0 transmit data empty interrupt</td></tr>
<tr><td>1</td><td>DTF1</td><td>0101: Activated by SCI channel 0 receive data full interrupt</td></tr>
<tr><td>0</td><td>DTF0</td><td>0110: Activated by SCI channel 1 transmit data empty interrupt</td></tr>
<tr><td></td><td></td><td>0111: Activated by SCI channel 1 receive data full interrupt</td></tr>
</table></td></tr>
</table>