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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	H8S/2600
Core Size	16-Bit
Speed	32MHz
Connectivity	EBI/EMI, I²C, IrDA, SCI, SSU, UART/USART, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	96
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b; D/A 2x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r4f24569dvrfqv

Pin No.		Pin Name					
					Mode 3, 7		Flash Memory Programmer Mode
PLQP0144KA-A	PTLG0145JB-A	Mode 1	Mode 2	Mode 4	EXPE = 1	EXPE = 0	
18	F4	Vss	Vss	Vss	Vss	Vss	Vss
19	G4	A12	A12	PB4/A12	PB4/A12	PB4/TIOCA7	A12
20	H4	A13	A13	PB5/A13	PB5/A13	PB5/TIOCB7/TCLKG	A13
21	G1	A14	A14	PB6/A14	PB6/A14	PB6/TIOCA8	A14
22	H2	A15	A15	PB7/A15	PB7/A15	PB7/TIOCB8/TCLKH	A15
23	G3	A16	A16	PA0/A16	PA0/A16	PA0	A16
24	J4	A17	A17	PA1/A17/TxD4_B	PA1/A17/TxD4_B	PA1/TxD4_B	A17
25	H1	Vss	Vss	Vss	Vss	Vss	Vss
26	J2	A18	A18	PA2/A18/RxD4-B	PA2/A18/RxD4-B	PA2/RxD4-B	A18
27	H3	A19	A19	PA3/A19/SCK4-B	PA3/A19/SCK4-B	PA3/SCK4-B	NC
28	K4	A20/$\overline{\text{IRQ4-A}}$	A20/$\overline{\text{IRQ4-A}}$	PA4/A20/$\overline{\text{IRQ4-A}}$/$\overline{\text{SCS0-B}}$	PA4/A20/$\overline{\text{IRQ4-A}}$/$\overline{\text{SCS0-B}}$	PA4/$\overline{\text{IRQ4-A}}$/$\overline{\text{SCS0-B}}$	NC
29	J1	PA5/A21/$\overline{\text{IRQ5-A}}$/SSCK0-B	PA5/A21/$\overline{\text{IRQ5-A}}$/SSCK0-B	PA5/A21/$\overline{\text{IRQ5-A}}$/SSCK0-B	PA5/A21/$\overline{\text{IRQ5-A}}$/SSCK0-B	PA5/$\overline{\text{IRQ5-A}}$/SSCK0-B	NC
30	K2	PA6/A22/$\overline{\text{IRQ6-A}}$/SSI0-B	PA6/A22/$\overline{\text{IRQ6-A}}$/SSI0-B	PA6/A22/$\overline{\text{IRQ6-A}}$/SSI0-B	PA6/A22/$\overline{\text{IRQ6-A}}$/SSI0-B	PA6/$\overline{\text{IRQ6-A}}$/SSI0-B	NC
31	J3	PA7/A23/$\overline{\text{IRQ7-A}}$/SSO0-B	PA7/A23/$\overline{\text{IRQ7-A}}$/SSO0-B	PA7/A23/$\overline{\text{IRQ7-A}}$/SSO0-B	PA7/A23/$\overline{\text{IRQ7-A}}$/SSO0-B	PA7/$\overline{\text{IRQ7-A}}$/SSO0-B	NC
32	K1	EMLE	EMLE	EMLE	EMLE	EMLE	Vss
33	L2	P81/$\overline{\text{IRQ1-B}}$/PO1-B/TIOCB3-B/TMRI1-B/TxD3/$\overline{\text{EDREQ3}}$	P81/$\overline{\text{IRQ1-B}}$/PO1-B/TIOCB3-B/TMRI1-B/TxD3/$\overline{\text{EDREQ3}}$	P81/$\overline{\text{IRQ1-B}}$/PO1-B/TIOCB3-B/TMRI1-B/TxD3/$\overline{\text{EDREQ3}}$	P81/$\overline{\text{IRQ1-B}}$/PO1-B/TIOCB3-B/TMRI1-B/TxD3/$\overline{\text{EDREQ3}}$	P81/$\overline{\text{IRQ1-B}}$/PO1-B/TIOCB3-B/TMRI1-B/TxD3/$\overline{\text{EDREQ3}}$	NC

Bit	Bit Name	Initial Value	R/W	Description
9	IRQ4SCB	0	R/W	IRQ4 Sense Control B
8	IRQ4SCA	0	R/W	IRQ4 Sense Control A 00: Interrupt request generated at $\overline{\text{IRQ4}}$ input low level 01: Interrupt request generated at falling edge of $\overline{\text{IRQ4}}$ input 10: Interrupt request generated at rising edge of $\overline{\text{IRQ4}}$ input 11: Interrupt request generated at both falling and rising edges of $\overline{\text{IRQ4}}$ input
7	IRQ3SCB	0	R/W	IRQ3 Sense Control B
6	IRQ3SCA	0	R/W	IRQ3 Sense Control A 00: Interrupt request generated at $\overline{\text{IRQ3}}$ input low level 01: Interrupt request generated at falling edge of $\overline{\text{IRQ3}}$ input 10: Interrupt request generated at rising edge of $\overline{\text{IRQ3}}$ input 11: Interrupt request generated at both falling and rising edges of $\overline{\text{IRQ3}}$ input
5	IRQ2SCB	0	R/W	IRQ2 Sense Control B
4	IRQ2SCA	0	R/W	IRQ2 Sense Control A 00: Interrupt request generated at $\overline{\text{IRQ2}}$ input low level 01: Interrupt request generated at falling edge of $\overline{\text{IRQ2}}$ input 10: Interrupt request generated at rising edge of $\overline{\text{IRQ2}}$ input 11: Interrupt request generated at both falling and rising edges of $\overline{\text{IRQ2}}$ input

A setting can be made in bits RCW1 and RCW0 in REFCR to delay $\overline{RAS}$ signal output by one to three cycles. Use bits RLW1 and RLW0 in REFCR to adjust the width of the $\overline{RAS}$ signal. The settings of bits RCW1, RCW0, RLW1, and RLW0 are valid only in refresh operations.

Figure 6.49 shows the timing when bits RCW1 and RCW0 are set.

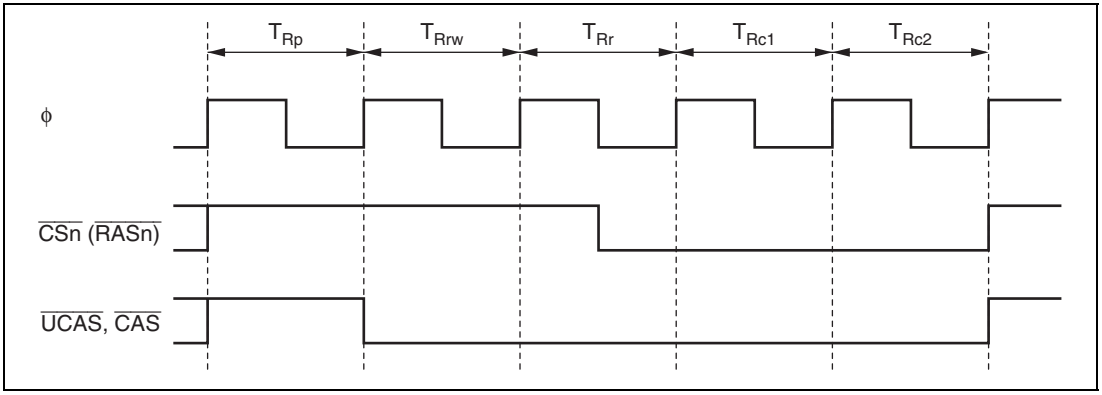

Figure 6.49 CBR Refresh Timing
(RCW1 = 0, RCW0 = 1, RLW1 = 0, RLW0 = 0)

Depending on the DRAM used, modification of the $\overline{WE}$ signal may not be permitted during the refresh period. In this case, the CBRM bit in REFCR should be set to 1. The bus controller will then insert refresh cycles in appropriate breaks between bus cycles. Figure 6.50 shows an example of the timing when the CBRM bit is set to 1. In this case the $\overline{CS}$ signal is not controlled, and retains its value prior to the start of the refresh period.

6.8.15 DMAC and EXDMAC Single Address Transfer Mode and Synchronous DRAM Interface

When burst mode is selected on the synchronous DRAM interface, the $\overline{\text{DACK}}$ and $\overline{\text{EDACK}}$ output timing can be selected with the DDS and EDDS bits in DRAMCR. When continuous synchronous DRAM space is accessed in DMAC/EXDMAC single address mode at the same time, these bits select whether or not burst access is to be performed. The establishment time for the read data can be extended in the clock suspend mode irrespective of the settings of the DDS and EDDS bits.

(1) Output Timing of $\overline{\text{DACK}}$ or $\overline{\text{EDACK}}$

When DDS = 1 or EDDS = 1: Burst access is performed by determining the address only, irrespective of the bus master. With the synchronous DRAM interface, the $\overline{\text{DACK}}$ or $\overline{\text{EDACK}}$ output goes low from the T_{c1} state.

Figure 6.72 shows the $\overline{\text{DACK}}$ or $\overline{\text{EDACK}}$ output timing for the synchronous DRAM interface when DDS = 1 or EDDS = 1.

(2) Write after Read

If an external write occurs after an external read while the ICIS0 bit is set to 1 in BCR, an idle cycle is inserted at the start of the write cycle.

Figure 6.78 shows an example of the operation in this case. In this example, bus cycle A is a read cycle for ROM with a long output floating time, and bus cycle B is a CPU write cycle. In (a), an idle cycle is not inserted, and a collision occurs in bus cycle B between the read data from ROM and the CPU write data. In (b), an idle cycle is inserted, and a data collision is prevented.

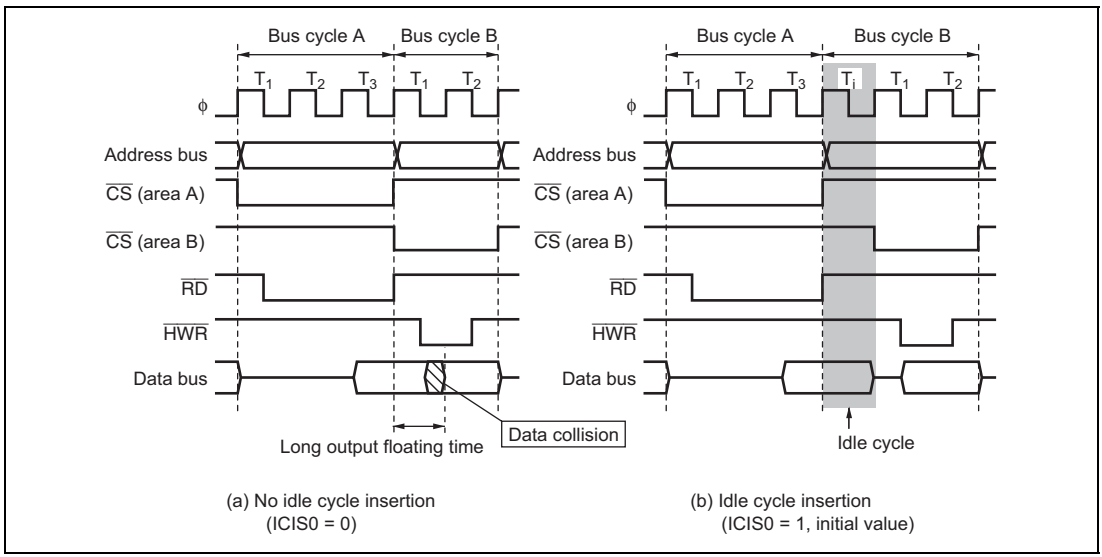

Figure 6.78 Example of Idle Cycle Operation (Write after Read)

6.14 Bus Controller Operation in Reset

In a reset, this LSI, including the bus controller, enters the reset state immediately, and any executing bus cycle is aborted.

6.15 Usage Notes

6.15.1 External Bus Release Function and All-Module-Clocks-Stopped Mode

In this LSI, if the ACSE bit is set to 1 in MSTPCR, and then a SLEEP instruction is executed with the setting for all peripheral module clocks to be stopped (MSTPCR = H'FFFF, EXMSTPCR = H'FFFF) or for operation of the 8-bit timer module alone (MSTPCR = H'FFFE, EXMSTPCR = H'FFFF), and a transition is made to the sleep state, the all-module-clocks-stopped mode is entered in which the clock is also stopped for the bus controller and I/O ports. In this state, the external bus release function is halted. To use the external bus release function in sleep mode, the ACSE bit in MSTPCR must be cleared to 0. Conversely, if a SLEEP instruction to place the chip in all-module-clocks-stopped mode is executed in the external bus released state, the transition to all-module-clocks-stopped mode is deferred and performed until after the bus is recovered.

6.15.2 External Bus Release Function and Software Standby

In this LSI, internal bus master operation does not stop even while the bus is released, as long as the program is running in on-chip ROM, etc., and no external access occurs. If a SLEEP instruction to place the chip in software standby mode is executed while the external bus is released, the transition to software standby mode is deferred and performed after the bus is recovered.

Also, since clock oscillation halts in software standby mode, if $\overline{\text{BREQ}}$ goes low in this mode, indicating an external bus release request, the request cannot be answered until the chip has recovered from the software standby state.

6.15.3 External Bus Release Function and CBR Refreshing/Auto Refreshing

CBR refreshing/auto refreshing cannot be executed while the external bus is released. Setting the BREQOE bit to 1 in BCR beforehand enables the $\overline{\text{BREQO}}$ signal to be output when a CBR refresh/auto refresh request is issued.

Note: The auto refresh control function is not supported by the H8S/2456 Group and H8S/2454 Group.

Figure 8.3 shows the data flow in single address mode, and figure 8.4 shows an example of the timing.

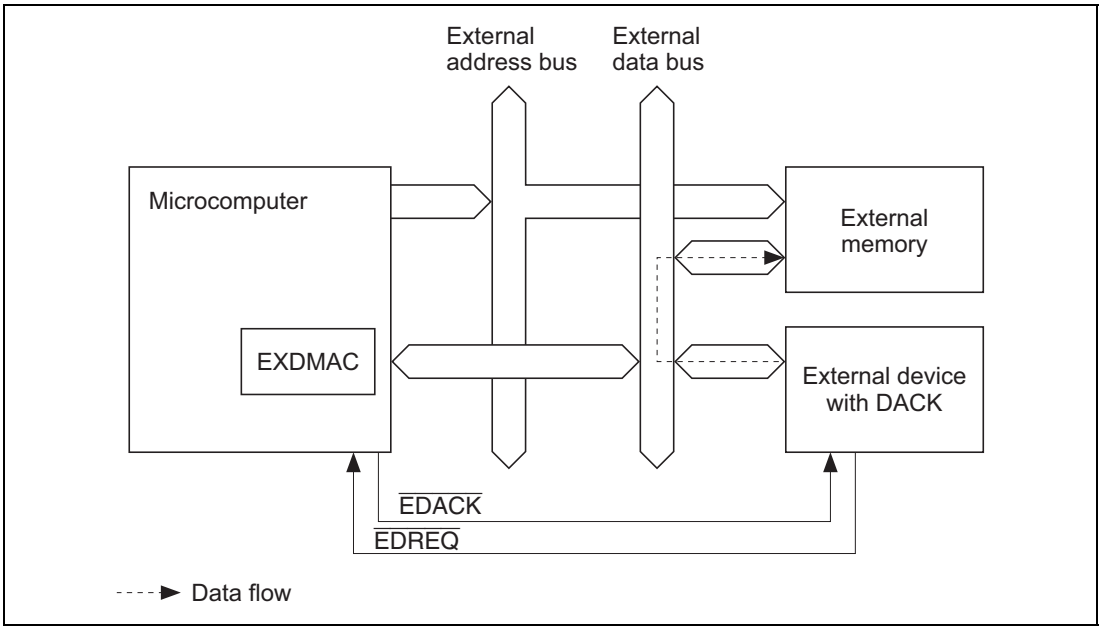

Figure 8.3 Data Flow in Single Address Mode

- P50/TxD2/$\overline{\text{IRQ0-A}}$/SDA3/$\overline{\text{BREQO-B}}$/PO0-B/TIOCA3-B/TMRI0-B

  The pin function is switched as shown below according to the combination of the operating mode, bit EXPE, bit BRLE of the bus controller, bit BREQOE, bit ICE in ICCRA_3 of the I2C, bits MD3 to MD0 in TMDR_3 of TPU, bits IOA3 to IOA0 in TIORH_3, TPU channel 3 settings by bits CCLR2 to CCLR0 in TCR_3, bit NDER0 in NDERL of PPG, bit TE in SCR_2 of the SCI, bits PPGS, TPUS, and TMRS in PFCR3, bit BREQOS in PFCR4, bit P50DDR, and bit ITS0 in ITSR of the interrupt controller.

- Modes 1, 2, and 4 Modes 3 and 7 (EXPE = 1)

<table>
<tr><td>BRLE
BREQOE
BREQOS</td><td colspan="6">BRLE = 0, or BRLE = 1 and BREQOE = 0,
or BRLE = 1, BREQOE = 1 and BREQOS = 0</td><td>BRLE = 1,
BREQOE = 1
and
BREQOS = 1</td></tr>
<tr><td>ICE</td><td colspan="5">0</td><td>1</td><td>—</td></tr>
<tr><td>TPU channel 3 settings</td><td>(1) in table below</td><td colspan="4">(2) in table below</td><td>—</td><td>—</td></tr>
<tr><td>TE</td><td>—</td><td colspan="3">0</td><td>1</td><td>—</td><td>—</td></tr>
<tr><td>P50DDR</td><td>—</td><td>0</td><td>1</td><td>1</td><td>—</td><td>—</td><td>—</td></tr>
<tr><td>NDER0</td><td>—</td><td>—</td><td>0</td><td>1</td><td>—</td><td>—</td><td>—</td></tr>
<tr><td rowspan="3">Pin function</td><td rowspan="2">TIOCA3-B output*7</td><td>P50 input</td><td>P50 output</td><td>PO0-B output*6</td><td>TxD2 output</td><td>SDA3*5 I/O</td><td>$\overline{\text{BREQO-B}}$ output</td></tr>
<tr><td colspan="6">TIOCA3-B input*1*7</td></tr>
<tr><td colspan="7">$\overline{\text{IRQ0-A}}$ interrupt input*2</td></tr>
<tr><td></td><td colspan="7">TMRI0-B input*3*8</td></tr>
</table>

- P82/$\overline{\text{IRQ2-B}}$/$\overline{\text{ETEND2}}$

  The pin function is switched as shown below according to the combination of bit ETENDE in EDMDR_2 of EXDMAC, bit P82DDR, and bit ITS2 in ITSR of the interrupt controller.

Operating mode	1, 2, 4 3, 7 (EXPE = 1)			3, 7 (EXPE = 0)	
ETENDE	0		1	—	
P82DDR	0	1	—	0	1
Pin function	P82 input	P82 output	$\overline{\text{ETEND2}}$ output	P82 input	P82 output
	$\overline{\text{IRQ2-B}}$ interrupt input*				

Note: * $\overline{\text{IRQ2-B}}$ input when the ITS2 bit in ITSR is 1.

- P81/$\overline{\text{EDREQ3}}$/$\overline{\text{IRQ1-B}}$/TxD3/PO1-B/TIOCB3-B/TMRI1-B

  The pin function is switched as shown below according to the combination of bit TE in SCR_3 of SCI, TPU channel 3 settings (by bits MD3 to MD0 in TMDR_3, bits IOB3 to IOB0 in TIORH_3, and bits CCLR2 to CCLR0 in TCR_3), bit NDER1 in NDERL of PPG, bits PPGS, TPUS, and TMRS in PFCR3, bit P81DDR, and bit ITS1 in ITSR of the interrupt controller.

TPU channel 3 settings	(1) in table below	(2) in table below			
TE	—	0			1
P81DDR	—	0	1	1	—
NDER1	—	—	0	1	—
Pin function	TIOCB3-B output*5	P81 input	P81 output	PO1-B output*4	TxD3 output
		TIOCB3-B input*2*5			
	$\overline{\text{EDREQ3}}$ input				
	$\overline{\text{IRQ1-B}}$ interrupt input*1				
	TMRI1-B input*3*6				

Notes: 1. $\overline{\text{IRQ1-B}}$ input when the ITS1 bit in ITSR is 1.
2. TIOCB3-B input when MD3 to MD0 = B'0000 and IOB3 to IOB0 = B'10xx.
3. When used as the counter reset input pin for the TMR, the external reset should be selected using the CCLR1 and CCLR0 bits in TCR_1 and TMRIS bit in TCCR_1 after the TMRS bit in PFCR3 is set to 1.
4. When using as PO1-B output, set PPGS in PFCR3 to 1 before other register setting.
5. When using as TIOCB3-B input/output, set TPUS in PFCR3 to 1 before other register setting.
6. When using as TMRI1-B input, set TMRS in PFCR3 to 1 before other register setting.

- Modes 3 and 7 (EXPE = 0)

WAITE	—				
SSU settings	(1) in table below		(2) in table below	(4) in table below	(3) in table below
PF0DDR	0	1	0*5	0*5	—
Pin function	PF0 input	PF0 output	$\overline{\text{SCS0-C}}$ input*2*6	$\overline{\text{SCS0-C}}$ I/O*4*6	$\overline{\text{SCS0-C}}$ output*3*6
	$\overline{\text{ADTRG0-B}}$ input*1				

Notes: 1. $\overline{\text{ADTRG0-B}}$ input when the ADTRG0S bit in PFCR4 is 1, TRGS1 = TRGS0 = 0, and EXTRGS = 1
2. When using as $\overline{\text{SCS0-C}}$ input, set SCS0S1 and SCS0S0 in PFCR5 to B'10 before other register setting.
3. When using as $\overline{\text{SCS0-C}}$ output, set SCS0S1 and SCS0S0 in PFCR5 to B'10 before other register setting.
4. When using as $\overline{\text{SCS0-C}}$ input/output, set SCS0S1 and SCS0S0 in PFCR5 to B'10 before other register setting.
5. PF0DDR = 0 when the SSU pin is used as input.
6. Do not set up for SSU unless SCS0S1 and SCS0S0 = B'10 in PFCR5. Use as I/O port.

SSU settings	(2)	(1)	(2)	(4)	(3)	(1)
SSUMS	0					1
MSS	0	1				x
CSS1	x	0		1		x
CSS0	x	0	1	0	1	x
Pin state	$\overline{\text{SCS}}$ input	—	$\overline{\text{SCS}}$ input	Automatic $\overline{\text{SCS}}$ I/O	$\overline{\text{SCS}}$ output	—

[Legend]

x: Don't care

—: Not used as the SSU pin (can be used as an I/O port).

Note: See tables 20.4 to 20.6.

Table 11.1 TPU (Unit 0) Functions

Item		Channel 0	Channel 1	Channel 2	Channel 3	Channel 4	Channel 5
Count clock		φ/1 φ/4 φ/16 φ/64 TCLKA TCLKB TCLKC TCLKD	φ/1 φ/4 φ/16 φ/64 φ/256 TCLKA TCLKB	φ/1 φ/4 φ/16 φ/64 φ/1024 TCLKA TCLKB TCLKC	φ/1 φ/4 φ/16 φ/64 φ/256 φ/1024 φ/4096 TCLKA	φ/1 φ/4 φ/16 φ/64 φ/1024 TCLKA TCLKC	φ/1 φ/4 φ/16 φ/64 φ/256 TCLKA TCLKC TCLKD
General registers (TGR)		TGRA_0 TGRB_0	TGRA_1 TGRB_1	TGRA_2 TGRB_2	TGRA_3 TGRB_3	TGRA_4 TGRB_4	TGRA_5 TGRB_5
General registers/ buffer registers		TGRC_0 TGRD_0	—	—	TGRC_3 TGRD_3	—	—
I/O pins		TIOCA0 TIOCB0 TIOCC0 TIOCD0	TIOCA1 TIOCB1	TIOCA2 TIOCB2	TIOCA3 TIOCB3 TIOCC3 TIOCD3	TIOCA4 TIOCB4	TIOCA5 TIOCB5
Counter clear function		TGR compare match or input capture	TGR compare match or input capture	TGR compare match or input capture	TGR compare match or input capture	TGR compare match or input capture	TGR compare match or input capture
Compare match output	0 output	○	○	○	○	○	○
	1 output	○	○	○	○	○	○
	Toggle output	○	○	○	○	○	○
Input capture function		○	○	○	○	○	○
Synchronous operation		○	○	○	○	○	○
PWM mode		○	○	○	○	○	○
Phase counting mode		—	○	○	—	○	○
Buffer operation		○	—	—	○	—	—

(b) Free-running count operation and periodic count operation

Immediately after a reset, the TPU's TCNT counters are all designated as free-running counters. When the relevant bit in TSTR is set to 1 the corresponding TCNT counter starts up-count operation as a free-running counter. When TCNT overflows (changes from H'FFFF to H'0000), the TCFV bit in TSR is set to 1. If the value of the corresponding TCIEV bit in TIER is 1 at this point, the TPU requests an interrupt. After overflow, TCNT starts counting up again from H'0000.

Figure 11.4 illustrates free-running counter operation.

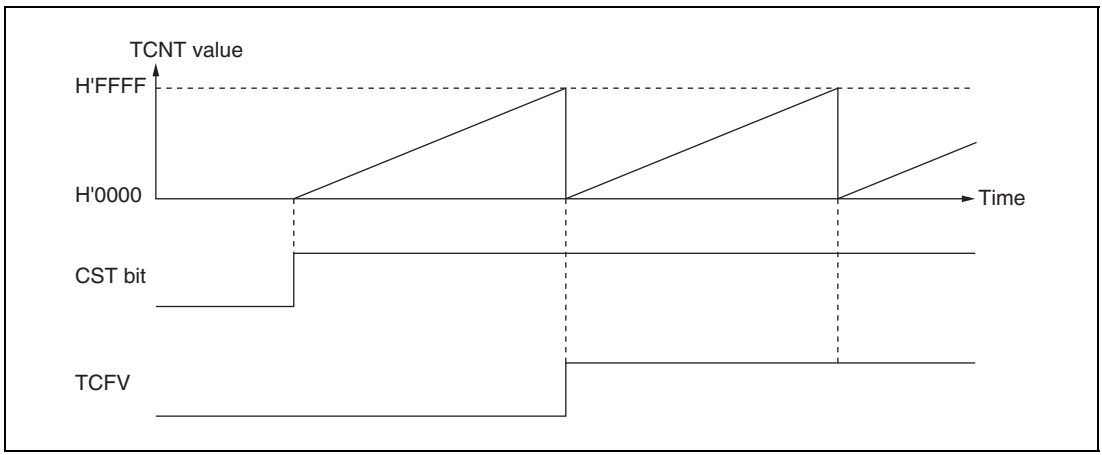

Figure 11.4 Free-Running Counter Operation

(3) Input Capture Function

The TCNT value can be transferred to TGR on detection of the TIOC pin input edge.

Rising edge, falling edge, or both edges can be selected as the detection edge. For channels 0, 1, 3, 4, 6, 7, 9, and 10 it is also possible to specify another channel's counter input clock or compare match signal as the input capture source.

Note: When another channel's counter input clock is used as the input capture input for channels 0, 3, 6, and 9, φ/1 should not be selected as the counter input clock used for input capture input. Input capture will not be generated if φ/1 is selected.

(a) Example of setting procedure for input capture operation

Figure 11.9 shows an example of the setting procedure for input capture operation.

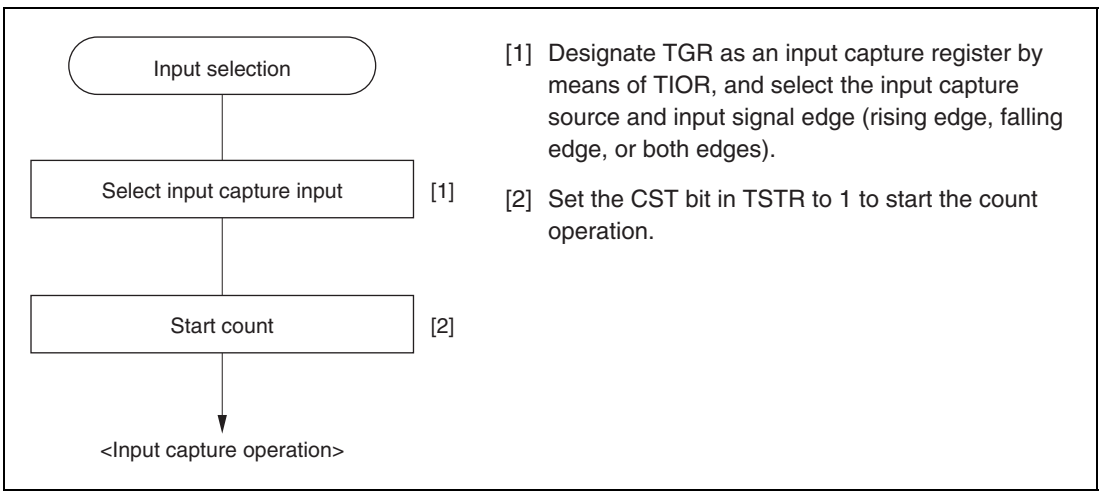

Figure 11.9 Example of Setting Procedure for Input Capture Operation

(2) Examples of Cascaded Operation

Figure 11.19 illustrates the operation when counting upon TCNT_2 overflow/underflow has been set for TCNT_1, TGRA_1 and TGRA_2 have been designated as input capture registers, and the TIOC pin rising edge has been selected.

When a rising edge is input to the TIOCA1 and TIOCA2 pins simultaneously, the upper 16 bits of the 32-bit data are transferred to TGRA_1, and the lower 16 bits to TGRA_2.

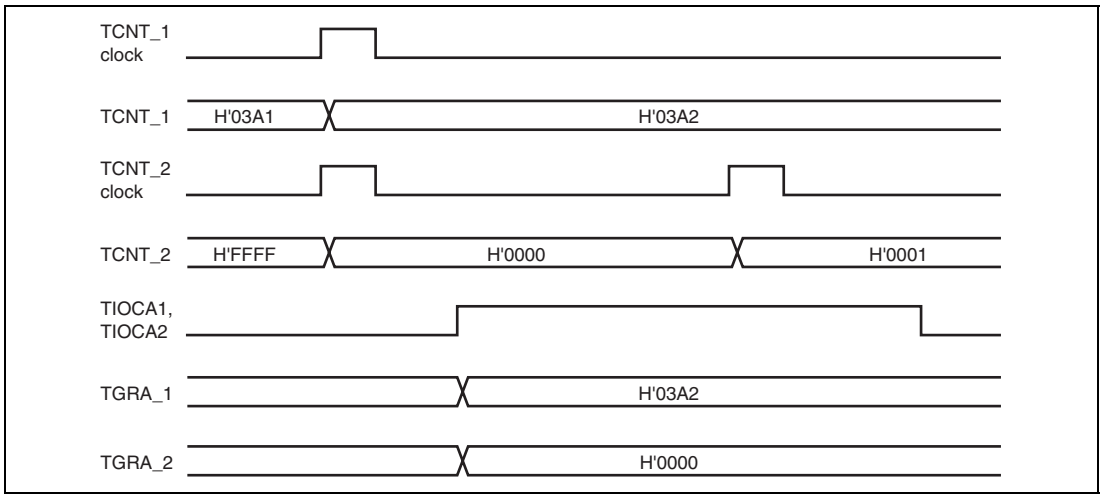

Figure 11.19 Example of Cascaded Operation (1)

Figure 11.20 illustrates the operation when counting upon TCNT_2 overflow/underflow has been set for TCNT_1, and phase counting mode has been designated for channel 2.

TCNT_1 is incremented by TCNT_2 overflow and decremented by TCNT_2 underflow.

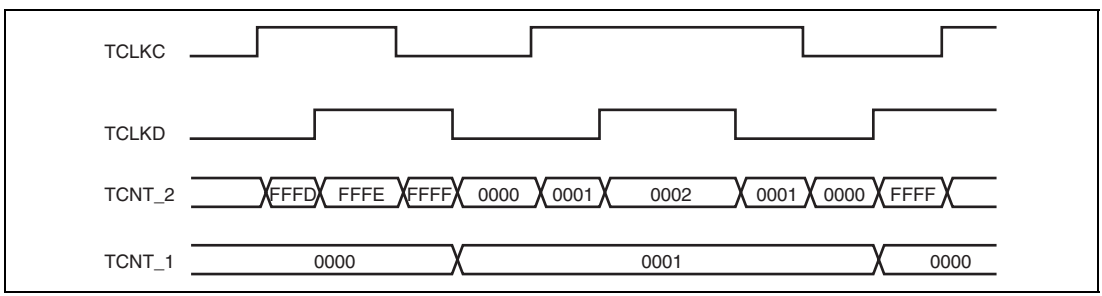

Figure 11.20 Example of Cascaded Operation (2)

14.4.2 Interval Timer Mode

To use the WDT as an interval timer, set the WT/$\overline{IT}$ bit to 0 and TME bit in TCSR to 1.

When the WDT is used as an interval timer, an interval timer interrupt (WOVI) is generated each time the TCNT overflows. Therefore, an interrupt can be generated at intervals.

When the TCNT overflows in interval timer mode, an interval timer interrupt (WOVI) is requested at the same time the OVF bit in the TCSR is set to 1.

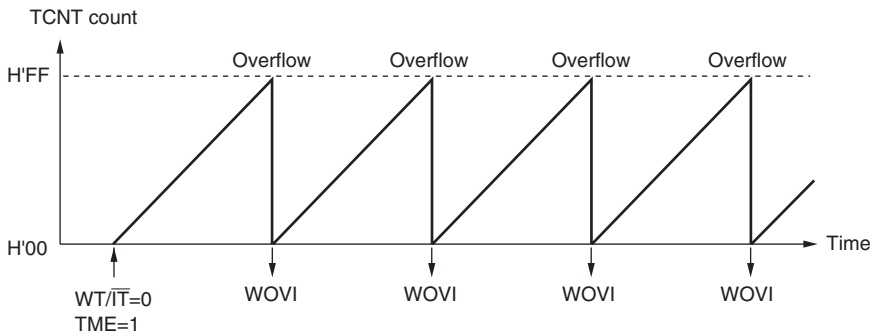

Figure 14.3 Operation in Interval Timer Mode

14.5 Interrupt Source

During interval timer mode operation, an overflow generates an interval timer interrupt (WOVI). The interval timer interrupt is requested whenever the OVF flag is set to 1 in TCSR. OVF must be cleared to 0 in the interrupt handling routine.

Table 14.2 WDT Interrupt Source

Name	Interrupt Source	Interrupt Flag	DTC Activation
WOVI	TCNT overflow	OVF	Impossible

15.7.8 Clock Output Control

When the GM bit in SMR is set to 1, the clock output level can be fixed with bits CKE1 and CKE0 in SCR. At this time, the minimum clock pulse width can be made the specified width.

Figure 15.31 shows the timing for fixing the clock output level. In this example, GM is set to 1, CKE1 is cleared to 0, and the CKE0 bit is controlled.

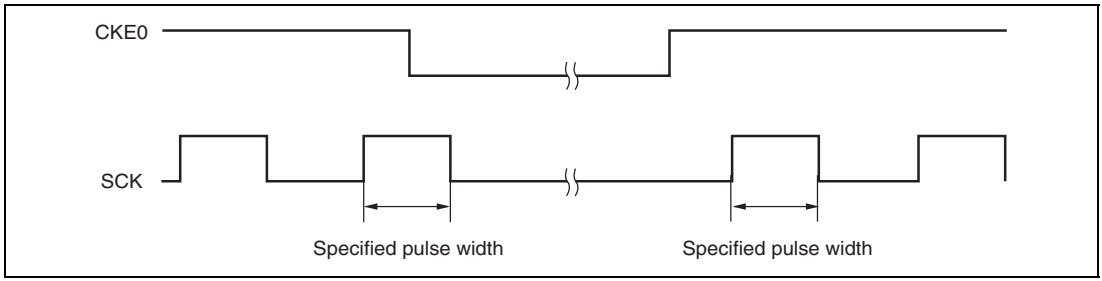

Figure 15.31 Timing for Fixing Clock Output Level

When turning on the power or switching between Smart Card interface mode and software standby mode, the following procedures should be followed in order to maintain the clock duty cycle.

Powering On: To secure the clock duty cycle from power-on, the following switching procedure should be followed.

1. The initial state is port input and high impedance. Use a pull-up resistor or pull-down resistor to fix the potential.
2. Fix the SCK pin to the specified output level with the CKE1 bit in SCR.
3. Set SMR and SCMR, and switch to Smart Card mode operation.
4. Set the CKE0 bit in SCR to 1 to start clock output.

16.3.15 EP3 Data Register (EPDR3)

EPDR3 is a 16-byte transmit FIFO buffer for endpoint 3. EPDR3 holds one packet of transmit data for the interrupt transfer of endpoint 3. Transmit data is fixed by writing one packet of data and setting EP3 PKTE in trigger register 1. This FIFO buffer can be initialized by means of EP3 CLR in FCLR register 1.

Bit	Bit Name	Initial Value	R/W	Description
7 to 0	D7 to D0	Undefined	W	Data register for endpoint 3 transfer

16.3.16 EP0o Receive Data Size Register (EPSZ0o)

EPSZ0o indicates the number of bytes received at endpoint 0 from the host.

Bit	Bit Name	Initial Value	R/W	Description
7 to 5	—	All 0	—	Reserved These bits are always read as 0.
4 to 0	D4 to D0	All 0	R	Number of receive data for endpoint 0

16.3.17 EP1 Receive Data Size Register (EPSZ1)

EPSZ1 is a receive data size resister for endpoint 1. EPSZ1 indicates the number of bytes received from the host. The FIFO for endpoint 1 has a dual-buffer configuration. The size of the received data indicated by this register is the size of the currently selected side (can be read by CPU).

Bit	Bit Name	Initial Value	R/W	Description
7	—	0	—	Reserved This bit is always read as 0.
6 to 0	D6 to D0	All 0	R	Number of received bytes for endpoint 1

24.4 SDRAMϕ Clock Output Control

Output of the SDRAMϕ clock can be controlled by the SDPSTP bit in SCKCR. When the SDPSTP bit is set to 1, the SDRAMϕ clock stops at the end of the bus cycle and the pin can be used as a general port. SDRAMϕ clock output is enabled when the SDPSTP bit is cleared to 0 regardless of the DDR value. Table 24.5 shows the state of the SDRAMϕ pin in each processing state.

Note: The SDRAM interface is not supported by the H8S/2456 Group and H8S/2454 Group.

Table 24.5 SDRAMϕ Pin State in Each Processing State

Register Setting						
SDPSTP	DDR	Normal Operating State	Sleep Mode	Software Standby Mode	Hardware Standby Mode	All Module Clocks Stop Mode
0	X	SDRAMϕ output	SDRAMϕ output	Fixed low	High impedance	SDRAMϕ output
1	0	High impedance	High impedance	High impedance	High impedance	High impedance
1	1	PH1/CS5/RAS5 output	H1/CS5/RAS5 output	H1/CS5/RAS5 output	High impedance	H1/CS5/RAS5 output

Note: SDRAM is not available in the H8S/2456 and H8S/2454 Groups.
In these products, this pin functions as a general pin regardless of the SDPSTP bit setting.

Item	Symbol	Min.	Max.	Unit	Test Conditions
Read command hold time	t_{RCH}	$0.5 \times t_{cyc} - 10$	—	ns	Figures 26.8 to 26.23, 26.29, and 26.30
$\overline{CAS}$ delay time 1	t_{CASD1}	—	15	ns	
$\overline{CAS}$ delay time 2	t_{CASD2}	—	15	ns	
$\overline{CAS}$ setup time 1	t_{CSR1}	$0.5 \times t_{cyc} - 10$	—	ns	
$\overline{CAS}$ setup time 2	t_{CSR2}	$1.5 \times t_{cyc} - 10$	—	ns	
$\overline{CAS}$ pulse width 1	t_{CASW1}	$1.0 \times t_{cyc} - 20$	—	ns	
$\overline{CAS}$ pulse width 2	t_{CASW2}	$1.5 \times t_{cyc} - 20$	—	ns	
$\overline{CAS}$ precharge time 1	t_{CPW1}	$1.0 \times t_{cyc} - 20$	—	ns	
$\overline{CAS}$ precharge time 2	t_{CPW2}	$1.5 \times t_{cyc} - 20$	—	ns	
$\overline{OE}$ delay time 1*[1]	t_{OED1}	—	15	ns	
	t_{OED1B}	—	19	ns	
$\overline{OE}$ delay time 2*[1]	t_{OED2}	—	15	ns	
	t_{OED2B}	—	19	ns	
Precharge time 1	t_{PCH1}	$1.0 \times t_{cyc} - 20$	—	ns	
Precharge time 2	t_{PCH2}	$1.5 \times t_{cyc} - 20$	—	ns	
Self-refresh precharge time 1	t_{RPS1}	$2.5 \times t_{cyc} - 20$	—	ns	Figures 26.22 and 26.23
Self-refresh precharge time 2	t_{RPS2}	$3.0 \times t_{cyc} - 20$	—	ns	
$\overline{WAIT}$ setup time	t_{WTS}	25	—	ns	Figures 26.10, 26.16, and 26.35
$\overline{WAIT}$ hold time	t_{WTH}	1	—	ns	
$\overline{BREQ}$ setup time	t_{BREQS}	30	—	ns	Figure 26.24
$\overline{BACK}$ delay time	t_{BACD}	—	15	ns	
Bus floating time	t_{BZD}	—	40	ns	
$\overline{BREQO}$ delay time	t_{BRQOD}	—	25	ns	Figure 26.25
Address delay time 2*[2]	t_{AD2}	—	16.5	ns	Figure 26.26
$\overline{CS}$ delay time 4*[2]	t_{CSD4}	—	16.5	ns	Figure 26.26
DQM delay time*[2]	t_{DQMD}	—	16.5	ns	Figure 26.26
CKE delay time *[2]*[3]	t_{CKED}	—	16.5	ns	Figures 26.27 and 26.28
	t_{CKEDB}	—	19	ns	
Read data setup time 3*[2]	t_{RDS3}	15	—	ns	Figure 26.26
Read data hold time 3*[2]	t_{RDH3}	0	—	ns	Figure 26.26
Write data delay time 2*[2]	t_{WDD}	—	31.5	ns	Figure 26.26
Write data hold time 4*[2]	t_{WDH4}	2	—	ns	Figure 26.26

Appendix

A. Port States in Each Processing State

Table A.1 Port States in Each Processing State (H8S/2456R Group and H8S/2456 Group)

Port Name Pin Name	MCU Operating Mode	Reset	Hardware Standby Mode	Software Standby Mode	Bus Release State	Program Execution State Sleep Mode
Port 1	1, 2, 3, 4, 7	T	T	Keep	Keep	I/O port
P27 to P26	1, 2, 3, 4, 7	T	T	Keep	Keep	I/O port
P25/$\overline{\text{WAIT}}$	1, 2, 3, 4, 7	T	T	[$\overline{\text{WAIT-B}}$ input] T [Other than the above] Keep	[$\overline{\text{WAIT-B}}$ input] T [Other than the above] Keep	[$\overline{\text{WAIT-B}}$ input] $\overline{\text{WAIT-B}}$ [Other than the above] I/O port
P20	1, 2, 3, 4, 7	T	T	Keep	Keep	I/O port
P34 to P30	1, 2, 3, 4, 7	T	T	Keep	Keep	I/O port
P35/$\overline{\text{OE-B}}$/ CKE-B*[1]	1, 2, 3, 4, 7	T	T	[$\overline{\text{OE-B}}$, CKE-B output, OPE = 0] T [$\overline{\text{OE-B}}$ output, OPE = 1] H [CKE-B output, OPE = 1] L [Other than the above] Keep	[$\overline{\text{OE-B}}$, CKE-B output, OPE = 0] T [Other than the above] Keep	[$\overline{\text{OE-B}}$, CKE-B output, OPE = 0] $\overline{\text{OE-B}}$, CKE-B [Other than the above] I/O port
Port 4	1, 2, 3, 4, 7	T	T	T	T	Input port
P53	1, 2, 3, 4, 7	T	T	Keep	Keep	I/O port
P52/ $\overline{\text{BACK-B}}$	1, 2, 3, 4, 7	T	T	[$\overline{\text{BACK-B}}$ output] $\overline{\text{BACK-B}}$ [Other than the above] Keep	[$\overline{\text{BACK-B}}$ output] $\overline{\text{BACK-B}}$ [Other than the above] Keep	[$\overline{\text{BACK-B}}$ output] $\overline{\text{BACK-B}}$ [Other than the above] I/O port