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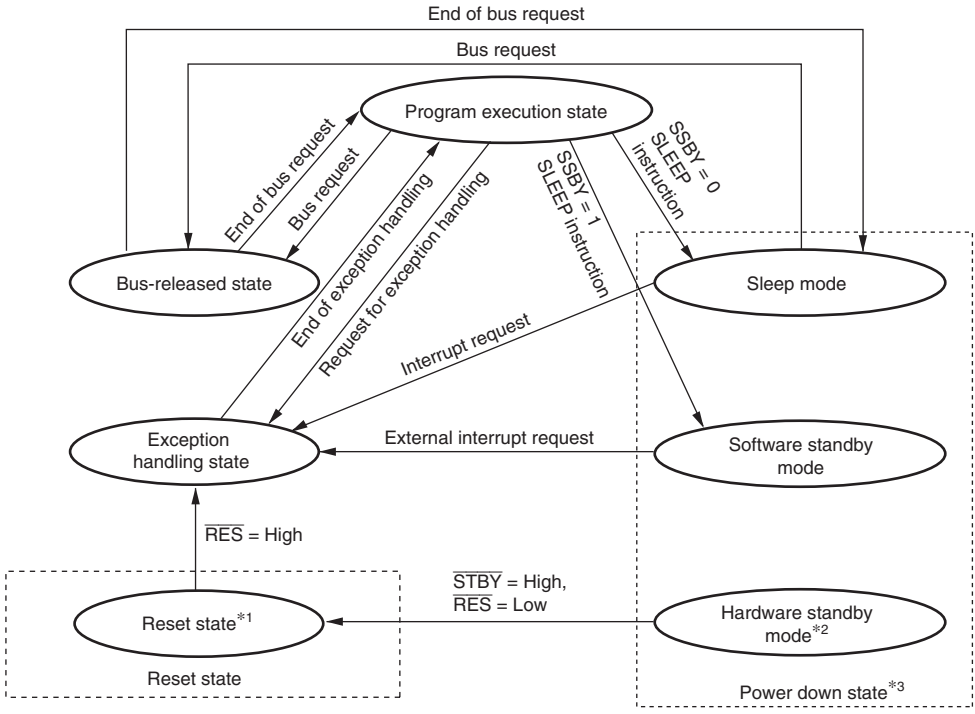
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	H8S/2600
Core Size	16-Bit
Speed	32MHz
Connectivity	EBI/EMI, I²C, IrDA, SCI, SSU, UART/USART, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	96
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b; D/A 2x8b
Oscillator Type	External
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r4f24569nvfqv



Notes: 1. From any state except hardware standby mode, a transition to the reset state occurs whenever the $\overline{RES}$ pin goes low. A transition can also be made to the reset state when the watchdog timer overflows.
2. In every state, when the $\overline{STBY}$ pin becomes low, the hardware standby mode is entered.
3. For details, refer to section 24, Power-Down Modes.

Figure 2.13 State Transitions

6.3.9 DRAM Control Register (DRAMCR)

DRAMCR is used to make DRAM/synchronous DRAM interface settings.

Note: The synchronous DRAM interface is not supported by the H8S/2456 Group and H8S/2454 Group.

Bit	Bit Name	Initial Value	R/W	Description
15	OEE	0	R/W	$\overline{OE}$ Output Enable The $\overline{OE}$ signal used when EDO page mode DRAM is connected can be output. The $\overline{OE}$ signal is common to all areas designated as DRAM space. When the synchronous DRAM is connected, the CKE signal can be output. The CKE signal is common to the continuous synchronous DRAM space. 0: $\overline{OE}$/CKE signal output disabled $\overline{OE}$/CKE pin can be used as an I/O port. 1: $\overline{OE}$/CKE signal output enabled.
14	RAST	0	R/W	$\overline{RAS}$ Assertion Timing Select Selects whether, in DRAM access, the $\overline{RAS}$ signal is asserted from the start of the T_r cycle (rising edge of ϕ) or from the falling edge of ϕ. Figure 6.4 shows the relationship between the RAST bit setting and the $\overline{RAS}$ assertion timing. The setting of this bit applies to all areas designated as DRAM space. 0: $\overline{RAS}$ is asserted from ϕ falling edge in T_r cycle 1: $\overline{RAS}$ is asserted from start of T_r cycle
13	—	0	R/W	Reserved This bit can be read from or written to. However, the write value should always be 0.

Table 6.2 Bus Specifications for Each Area (Basic Bus Interface)

ABWCR	ASTCR	WTCRA, WTCRB			Bus Specifications (Basic Bus Interface)		
ABWn	ASTn	Wn2	Wn1	Wn0	Bus Width	Access States	Program Wait States
0	0	—	—	—	16	2	0
	1	0	0	0		3	0
				1			1
			1	0			2
				1			3
		1	0	0			4
				1			5
			1	0			6
				1			7
1	0	—	—	—	8	2	0
	1	0	0	0		3	0
				1			1
			1	0			2
				1			3
		1	0	0			4
				1			5
			1	0			6
				1			7

(n = 0 to 7)

(4) Read Strobe Timing

RDNCR can be used to select either of two negation timings (at the end of the read cycle or one half-state before the end of the read cycle) for the read strobe ($\overline{RD}$) used in the basic bus interface space.

(5) Chip Select ($\overline{CS}$) Assertion Period Extension States

Some external I/O devices require a setup time and hold time between address and $\overline{CS}$ signals and strobe signals such as $\overline{RD}$, $\overline{HWR}$, and $\overline{LWR}$. CSACR can be used to insert states in which only the $\overline{CS}$, $\overline{AS}$, and address signals are asserted before and after a basic bus space access cycle.

When consecutively reading from the same area connected to a peripheral LSI whose output floating time is long, data outputs from the peripheral LSI may conflict with address outputs from this LSI. The data conflict can be avoided by inserting the $\overline{CS}$ assertion period extension cycle after the access cycle. Figure 6.32 shows an example of the operation. In the figure, both bus cycles A and B are read access cycles to the same area which is address/data multiplexed I/O space. (a) shows an example of conflict occurring between data outputs from the peripheral LSI whose output floating time is long and address outputs from this LSI because the $\overline{CS}$ assertion period extension cycle is not inserted. (b) shows an example of the data conflict being avoided by inserting the $\overline{CS}$ assertion period extension cycle.

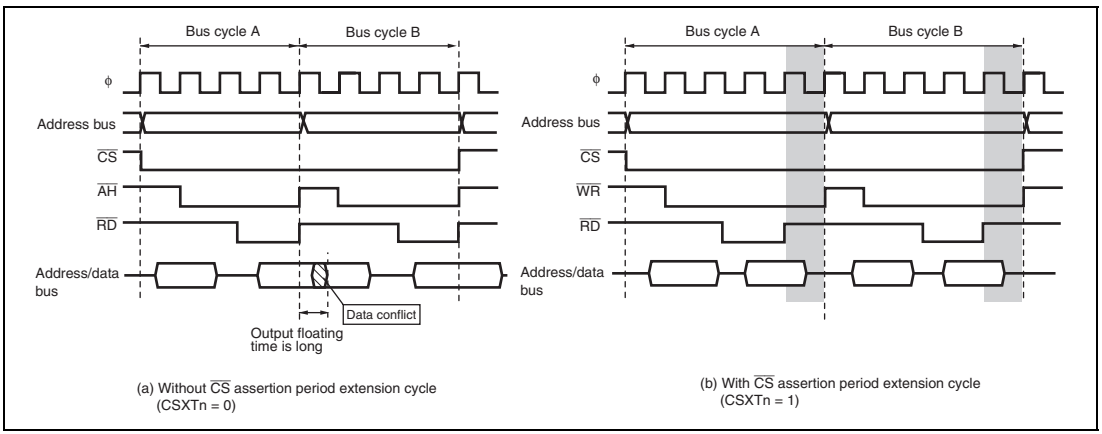


Figure 6.32 Consecutive Read Accesses to Same Area (Address/Data Multiplexed I/O Space)

6.7 DRAM Interface

In this LSI, external space areas 2 to 5 can be designated as DRAM space, and DRAM interfacing performed. The DRAM interface allows DRAM to be directly connected to this LSI. A DRAM space of 2, 4, or 8 Mbytes can be set by means of bits RMTS2 to RMTS0 in DRAMCR. Burst operation is also possible, using fast page mode.

6.7.1 Setting DRAM Space

Areas 2 to 5 are designated as DRAM space by setting bits RMTS2 to RMTS0 in DRAMCR. The relation between the settings of bits RMTS2 to RMTS0 and DRAM space is shown in table 6.5. Possible DRAM space settings are: one area (area 2), two areas (areas 2 and 3), four areas (areas 2 to 5), and continuous area (areas 2 to 5).

Table 6.5 Relation between Settings of Bits RMTS2 to RMTS0 and DRAM Space

RMTS2	RMTS1	RMTS0	Area 5	Area 4	Area 3	Area 2
0	0	1	Normal space	Normal space	Normal space	DRAM space
	1	0	Normal space	Normal space	DRAM space	DRAM space
		1	DRAM space	DRAM space	DRAM space	DRAM space
1	0	0	Continuous synchronous DRAM space*			
		1	Mode register settings of synchronous DRAM*			
	1	0	Reserved (setting prohibited)			
		1	Continuous DRAM space	Continuous DRAM space	Continuous DRAM space	Continuous DRAM space

Note: * Reserved (setting prohibited) in the H8S/2456 Group and H8S/2454 Group.

With continuous DRAM space, $\overline{\text{RAS2}}$ is valid. The bus specifications (bus width, number of wait states, etc.) for continuous DRAM space conform to the settings for area 2.

When DDS = 0 or EDDS = 0: When continuous synchronous DRAM space is accessed in DMAC or EXDMAC single address transfer mode, full access (normal access) is always performed. With the synchronous DRAM interface, the $\overline{\text{DACK}}$ or $\overline{\text{EDACK}}$ output goes low from the T_r state.

In modes other than DMAC or EXDMAC single address transfer mode, burst access can be used when accessing continuous synchronous DRAM space.

Figure 6.73 shows the $\overline{\text{DACK}}$ or $\overline{\text{EDACK}}$ output timing for connecting the synchronous DRAM interface when DDS = 0 or EDDS = 0.

Bit	Bit Name	Initial Value	R/W	Description
3	DTF3	0	R/W	Data Transfer Factor 3 to 0
2	DTF2	0	R/W	These bits select the data transfer factor (activation source). There are some differences in activation sources for channel A and channel B.
1	DTF1	0	R/W	
0	DTF0	0	R/W	• Channel A 0000: Setting prohibited 0001: Activated by conversion end interrupt of A/D converter unit 0 0010: Setting prohibited 0011: Setting prohibited 0100: Activated by SCI channel 0 transmit data empty interrupt 0101: Activated by SCI channel 0 receive data full interrupt 0110: Activated by SCI channel 1 transmit data empty interrupt 0111: Activated by SCI channel 1 receive data full interrupt 1000: Activated by TPU channel 0 compare match/input capture A interrupt 1001: Activated by TPU channel 1 compare match/input capture A interrupt 1010: Activated by TPU channel 2 compare match/input capture A interrupt 1011: Activated by TPU channel 3 compare match/input capture A interrupt 1100: Activated by TPU channel 4 compare match/input capture A interrupt 1101: Activated by TPU channel 5 compare match/input capture A interrupt 1110: Setting prohibited 1111: Setting prohibited

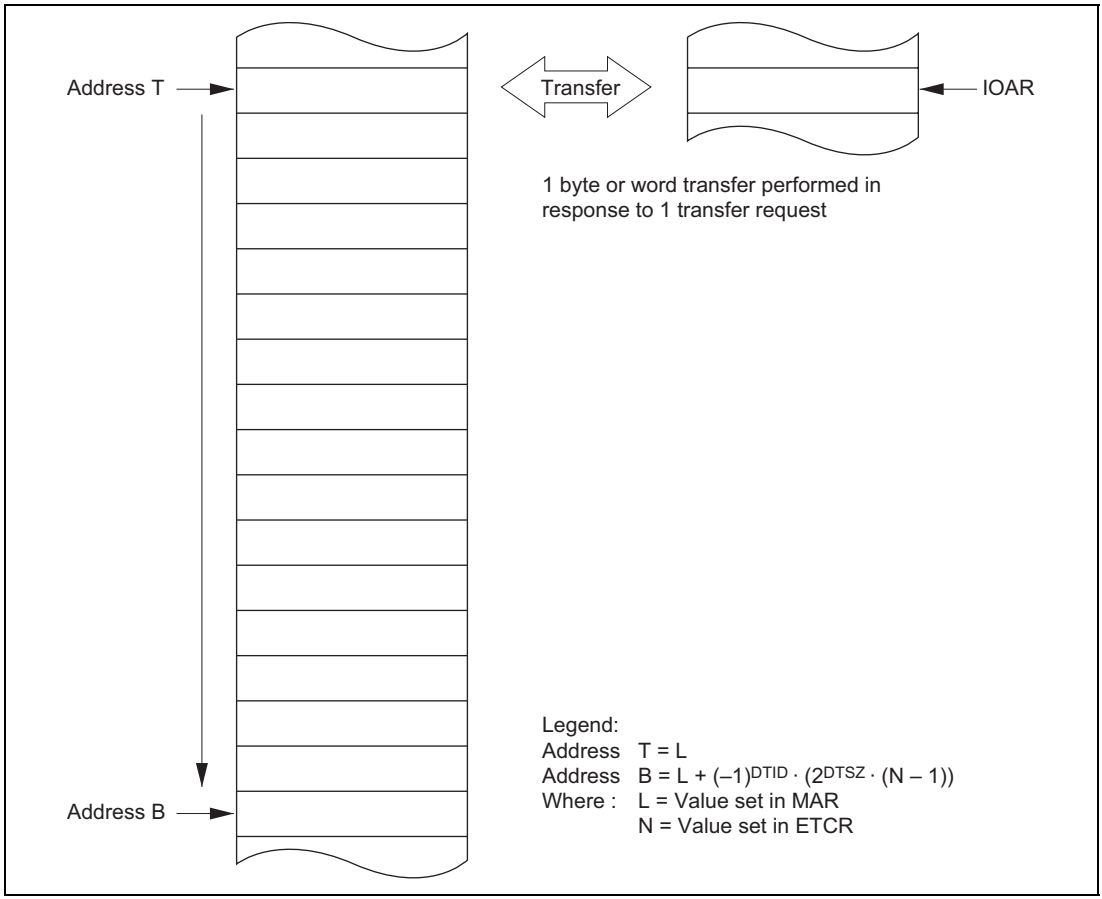


Figure 7.3 Operation in Sequential Mode

The number of transfers is specified as 16 bits in ETCR. ETCR is decremented by 1 each time a data transfer is executed, and when its value reaches H'0000, the DTE bit is cleared and data transfer ends. If the DTIE bit is set to 1 at this time, an interrupt request is sent to the CPU or DTC. The maximum number of transfers, when H'0000 is set in ETCR, is 65,536.

Transfer requests (activation sources) consist of A/D converter conversion end interrupts, external requests, SCI transmit data empty and receive data full interrupts, and TPU channel 0 to 5 compare match/input capture A interrupts. External requests can only be specified for channel B.

Figure 7.4 shows an example of the setting procedure for sequential mode.

$\overline{\text{DREQ}}$ pin sampling is performed every cycle, with the rising edge of the next ϕ cycle after the end of the DMABCR write cycle for setting the transfer enabled state as the starting point.

When the $\overline{\text{DREQ}}$ pin low level is sampled while acceptance by means of the $\overline{\text{DREQ}}$ pin is possible, the request is held in the DMAC. Then, when activation is initiated in the DMAC, the request is cleared, and $\overline{\text{DREQ}}$ pin high level sampling for edge detection is started. If $\overline{\text{DREQ}}$ pin high level sampling has been completed by the time the DMA write cycle ends, acceptance resumes after the end of the write cycle, $\overline{\text{DREQ}}$ pin low level sampling is performed again, and this operation is repeated until the transfer ends.

8.4.5 Transfer Modes

There are two transfer modes: normal transfer mode and block transfer mode. When the activation source is an external request, either normal transfer mode or block transfer mode can be selected. When the activation source is an auto request, normal transfer mode is used.

(1) Normal Transfer Mode

In normal transfer mode, transfer of one transfer unit is processed in response to one transfer request. EDTCR functions as a 24-bit transfer counter.

The $\overline{\text{ETEND}}$ signal is output only for the last EXDMA transfer. The $\overline{\text{EDRAK}}$ signal is output each time a transfer request is accepted and transfer processing is started.

Figure 8.7 shows examples of EXDMA transfer timing in normal transfer mode.

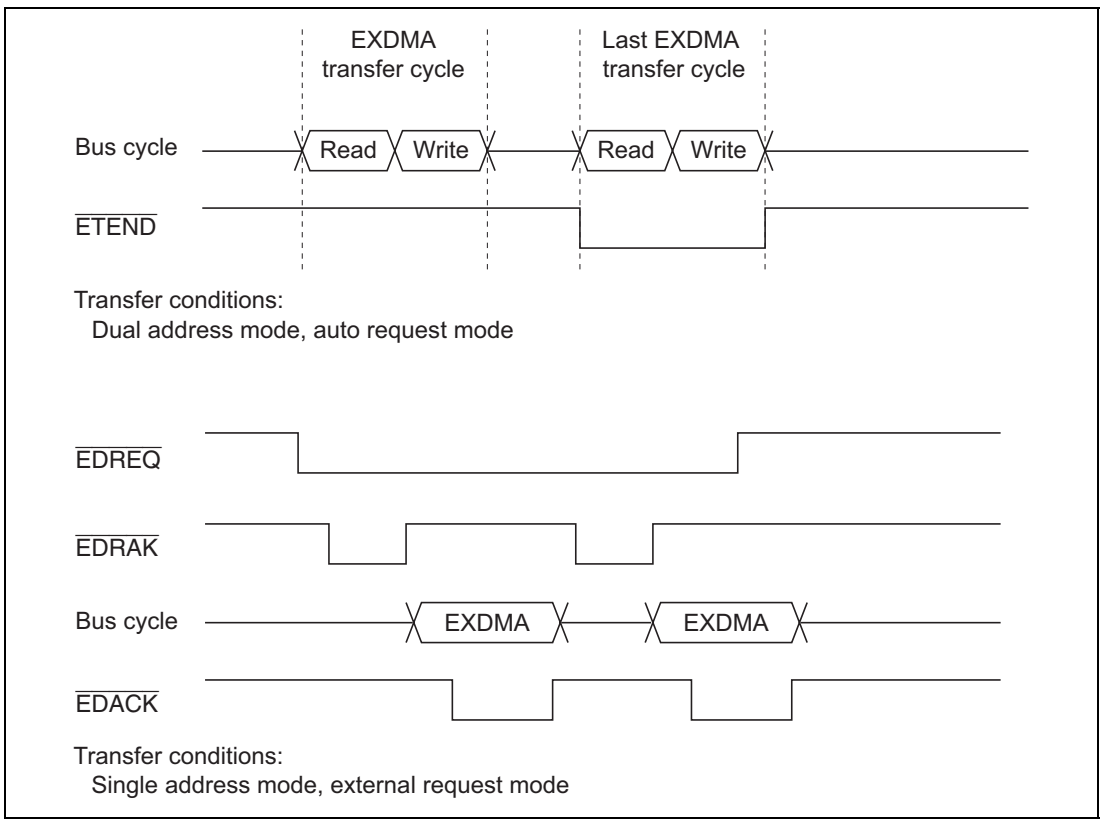
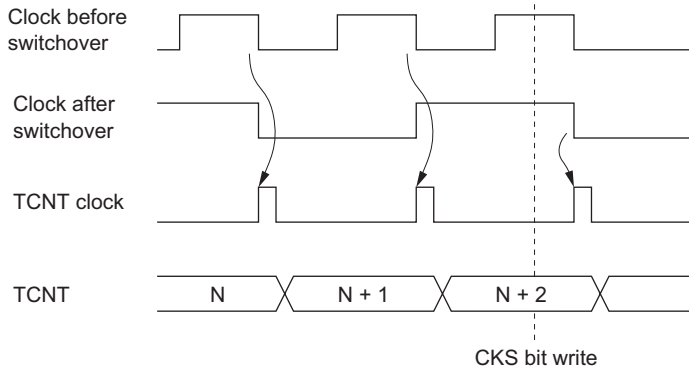


Figure 8.7 Examples of Timing in Normal Transfer Mode

No.	Timing of Switchover by Means of Modifying CKS1, CKS0, ICKS1, and ICKS0 Bits	TCNT Clock Operation
4	Switching from high to high	

Notes: 1. Includes switching from low to stop, and from stop to low.
2. Includes switching from stop to high.
3. Includes switching from high to stop.
4. Generated on the assumption that the switchover is a falling edge; TCNT is incremented.

13.8.6 Mode Setting with Cascaded Connection

If 16-bit counter mode and compare match count mode are specified at the same time, input clocks for TCNT_0 and TCNT_1 are not generated, and the counter stops. Do not specify 16-bit counter and compare match count modes simultaneously.

13.8.7 Module Stop Function Setting

Operation of the TMR can be disabled or enabled using the module stop control register. The initial setting is for operation of the TMR to be halted. Register access is enabled by clearing the module stop state. For details, refer to section 24, Power-Down Modes.

13.8.8 Interrupts in Module Stop State

If a transition is made to the module stop state when an interrupt has been requested, it will not be possible to clear the CPU interrupt source or the DTC and DMAC activation source. Interrupts should therefore be disabled before entering the module stop state.

14.4 Operation

14.4.1 Watchdog Timer Mode

To use the WDT as a watchdog timer mode, set the WT/$\overline{IT}$ and TME bits in TCSR to 1.

If TCNT overflows without being rewritten because of a system crash or other error, the $\overline{WDTOVF}$ signal is output.

This ensures that TCNT does not overflow while the system is operating normally. Software must prevent TCNT overflows by rewriting the TCNT value (normally be writing H'00) before overflow occurs. This $\overline{WDTOVF}$ signal can be used to reset the chip internally in watchdog timer mode.

If TCNT overflows when 1 is set in the RSTE bit in RSTCSR, a signal that resets this LSI internally is generated at the same time as the $\overline{WDTOVF}$ signal. If a reset caused by a signal input to the $\overline{RES}$ pin occurs at the same time as a reset caused by a WDT overflow, the $\overline{RES}$ pin reset has priority and the WOVF bit in RSTCSR is cleared to 0.

The $\overline{WDTOVF}$ signal is output for 132 states when RSTE = 1, and for 130 states when RSTE = 0. The internal reset signal is output for 518 states.

When TCNT overflows in watchdog timer mode, the WOVF bit in RSTCSR is set to 1. If TCNT overflows when 1 is set in the RSTE bit in RSTCSR, an internal reset signal is generated to the entire chip.

15.6.4 Serial Data Reception (Clocked Synchronous Mode)

Figure 15.18 shows an example of SCI operation for reception in clocked synchronous mode. In serial reception, the SCI operates as described below.

1. The SCI performs internal initialization in synchronization with a synchronization clock input or output, starts receiving data, and stores the received data in RSR.
2. If an overrun error (when reception of the next data is completed while the RDRF flag is still set to 1) occurs, the ORER bit in SSR is set to 1. If the RIE bit in SCR is set to 1 at this time, an ERI interrupt request is generated. Receive data is not transferred to RDR. The RDRF flag remains to be set to 1.
3. If reception finishes successfully, the RDRF bit in SSR is set to 1, and receive data is transferred to RDR. If the RIE bit in SCR is set to 1 at this time, an RXI interrupt request is generated. Because the RXI interrupt routine reads the receive data transferred to RDR before reception of the next receive data has finished, continuous reception can be enabled.

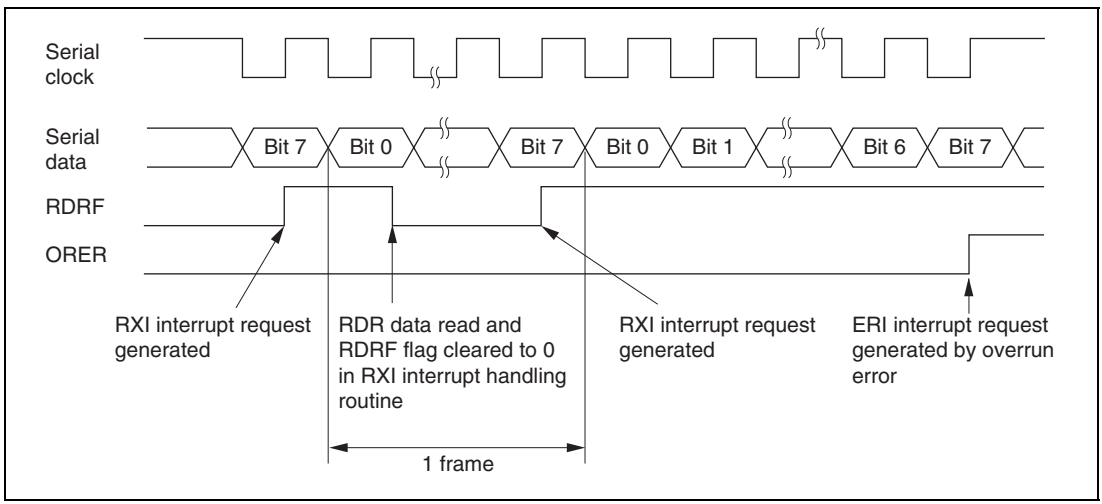


Figure 15.18 Example of SCI Operation in Reception

Transfer cannot be resumed while a receive error flag is set to 1. Accordingly, clear the ORER, FER, PER, and RDRF bits to 0 before resuming reception. Figure 15.19 shows a sample flowchart for serial data reception.

(3) Data Stage (Control-Out)

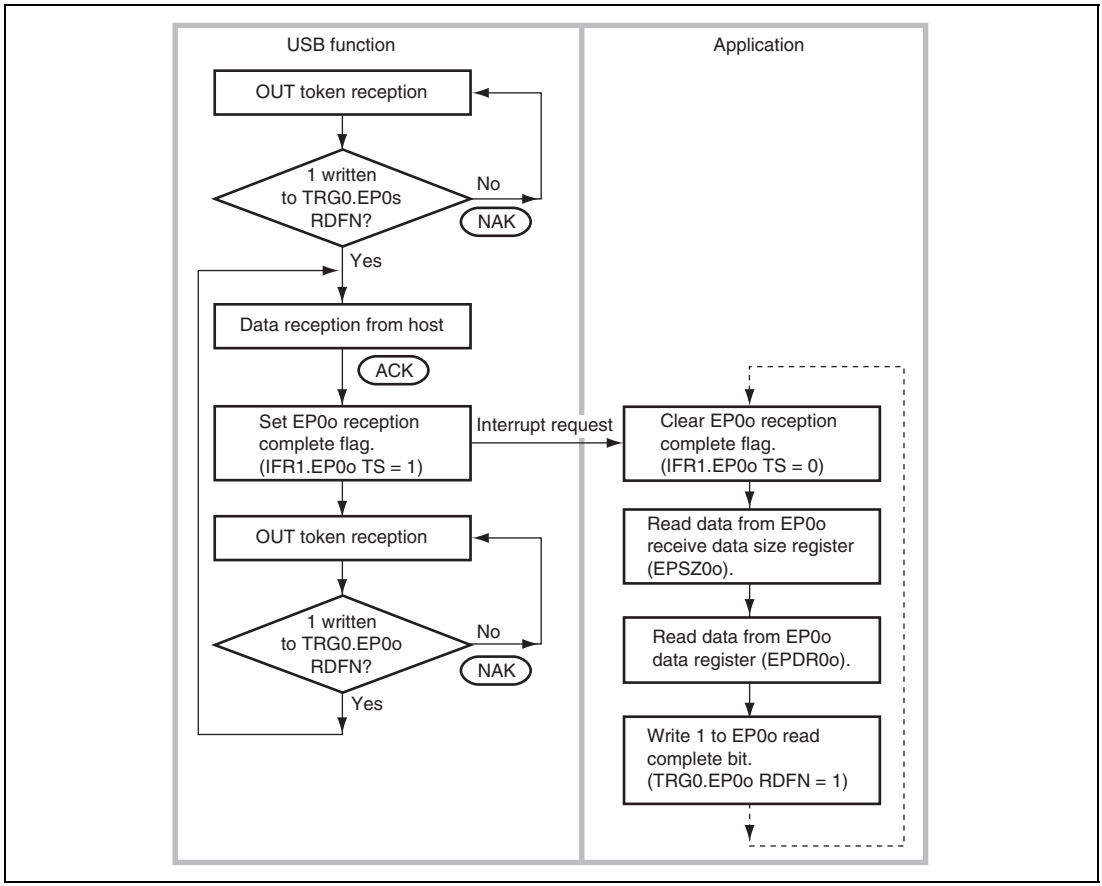


Figure 16.13 Data Stage (Control-Out) Operation

The application first analyzes command data from the host in the setup stage, and determines the subsequent data stage direction. If the result of command data analysis is that the data stage is out-transfer, the application waits for data from the host, and after data is received (EP0o TS bit in IFR1 = 1), reads data from the FIFO. Next, the application writes 1 to the EP0o read complete bit, empties the receive FIFO, and waits for reception of the next data.

The end of the data stage is identified when the host transmits an IN token and the status stage is entered.

- SUM (1 byte): Checksum

Response	H'06

- Response, H'06, (1 byte): Response to selection of a new bit rate
  When it is possible to set the bit rate, the response will be ACK.

Error Response	H'BF	ERROR

- Error response, H'BF, (1 byte): Error response to selection of new bit rate
- ERROR: (1 byte): Error code
  - H'11: Sum check error
  - H'24: Bit-rate selection disable error
    The rate is not available.
  - H'25: Input frequency error
    This input frequency is not within the specified range.
  - H'26: Multiplication-ratio error
    The ratio does not match an available ratio.
  - H'27: Operating frequency error
    The frequency is not within the specified range.

(5) Received Data Check

The methods for checking of received data are listed below.

1. Input frequency

The received value of the input frequency is checked to ensure that it is within the range of minimum to maximum frequencies which matches the clock modes of the specified device. When the value is out of this range, an input-frequency error is generated.

2. Multiplication ratio

The received value of the multiplication ratio or division ratio is checked to ensure that it matches a multiplication or division ratio for the clock modes of the specified device. When the value is out of this range, an input-frequency error is generated.

3. Operating frequency error

The operating frequency is calculated from the received value of the input frequency and the multiplication or division ratio. The input frequency is input to the LSI and the LSI is operated at the operating frequency. The expression is given below.

Operating frequency = Input frequency × Multiplication ratio, or
Operating frequency = Input frequency ÷ Division ratio

(7) Command Error

A command error will occur when a command is undefined, the order of commands is incorrect, or a command is unacceptable. Issuing a clock-mode selection command before a device selection or an inquiry command after the transition to programming/erasing state command, are examples.

Error Response	H'80	H'xx

- Error response, H'80, (1 byte): Command error
- Command, H'xx, (1 byte): Received command

(8) Command Order

The order for commands in the inquiry/selection state is shown below.

1. A supported device inquiry (H'20) should be made to inquire about the supported devices.
2. The device should be selected from among those described by the returned information and set with a device-selection (H'10) command.
3. A clock-mode inquiry (H'21) should be made to inquire about the supported clock modes.
4. The clock mode should be selected from among those described by the returned information and set.
5. After selection of the device and clock mode, inquiries for other required information should be made, such as the multiplication-ratio inquiry (H'22) or operating frequency inquiry (H'23), which are needed for a new bit-rate selection.
6. A new bit rate should be selected with the new bit-rate selection (H'3F) command, according to the returned information on multiplication ratios and operating frequencies.
7. After selection of the device and clock mode, inquiries for the information of programming/erasing to the user ROM should be made by the user ROMs information inquiry (H'25), erased block information inquiry (H'26), and programming unit inquiry (H'27).
8. After making inquiries and selecting a new bit rate, issue the transition to programming/erasing state command (H'40). The boot program will then enter the programming/erasing state.

23.1.3 USB PLL Control Register (USPLLCR)

USPLLCR selects multiplication factor used by the PLL circuit.

Bit	Bit Name	Initial Value	R/W	Description
7 to 2	—	All 0	—	Reserved These bits are always read as 0 and cannot be modified.
1	USSTC1	0	R/W	Frequency Multiplication Factor for USB PLL Circuit Setting
0	USSTC0	0	R/W	The USSTC bits specify the frequency multiplication factor for USB PLL circuit. 00: USB PLL circuit operation halted 01: USB PLL in operation with frequency × 3 10: USB PLL in operation with frequency × 4 11: USB PLL in operation with frequency × 6

Notes: 1. t_{OED1}, and t_{OED2} correspond to the $\overline{\text{OE-A}}$ and $\overline{\text{RD}}$, and, t_{OED1B}, and t_{OED2B} correspond to the $\overline{\text{OE-B}}$.
2. Supported only by the H8S/2456R Group.
3. t_{CKED} corresponds to the CKE-A, t_{CKEDB} corresponds to the CKE-B.

(4) DMAC and EXDMAC Timing

Table 26.9 DMAC and EXDMAC Timing

Conditions: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 8 MHz to 33 MHz

Item	Symbol	Min.	Max.	Unit	Test Conditions
$\overline{\text{DREQ}}$ setup time	t_{DRQS}	25	—	ns	Figure 26.34
$\overline{\text{DREQ}}$ hold time	t_{DRQH}	10	—		
$\overline{\text{TEND}}$ delay time	t_{TED}	—	18	ns	Figure 26.33
$\overline{\text{DACK}}$ delay time 1	t_{DACD1}	—	18		Figures 26.31 and 26.32
$\overline{\text{DACK}}$ delay time 2	t_{DACD2}	—	18		
$\overline{\text{EDREQ}}$ setup time	t_{EDRQS}	25	—	ns	Figure 26.34
$\overline{\text{EDREQ}}$ hold time	t_{EDRQH}	10	—		
$\overline{\text{ETEND}}$ delay time	t_{ETED}	—	18	ns	Figure 26.33
$\overline{\text{EDACK}}$ delay time 1	t_{EDACD1}	—	18	ns	Figures 26.31 and 26.32
$\overline{\text{EDACK}}$ delay time 2	t_{EDACD2}	—	18		
$\overline{\text{EDRAK}}$ delay time	t_{EDRKD}	—	18	ns	Figure 26.35