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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	50
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	104K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc54101j256bd64ql

The LPC5410x LQFP64 package has the following top-side marking:

- First line: LPC5410xJyyy
  - x: 2 = dual core (M4, M0+), 1 = single core (M4)
  - yyy: flash size
- Second line: BD64
- Third line: xxxxxxxxxxxx
- Fourth line: xxxyywwx[R]z
  - yyww: Date code with yy = year and ww = week.
  - xR = boot code version and device revision.

The LPC5410x WLCSP49 package has the following top-side marking:

- First line: LPC5410x
  - x: 2 = dual core (M4, M0+), 1 = single core (M4)
- Second line: JxxxUK49
  - xxx: flash size
- Third line: xxxxxxxx
- Fourth line: xxxyyww
  - yyww: Date code with yy = year and ww = week.
- Fifth line: xxxxx
- Sixth line: NXP x[R]z
  - xR = boot code version and device revision.

Table 3. Device revision table

Revision identifier (R)	Revision description
‘1B’	Initial device revision with boot code version 17.1.
‘1C’	Second device revision with boot code version 17.1.

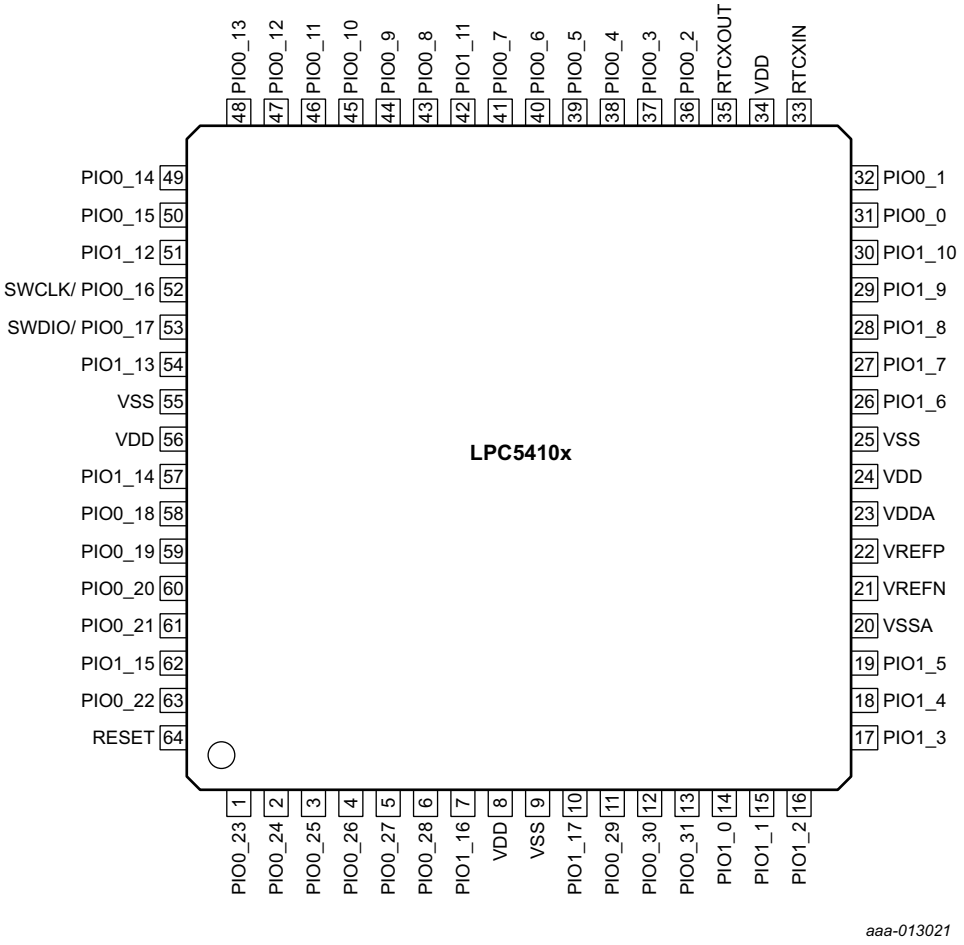


Fig 5. LQFP64 Pin configuration

Table 4. Pin description *…continued*

Symbol	WLCSP49	LQFP64		Reset state [1]	Type [6]	Description
PIO0_12	F7	47	[2]	PU	I/O	**PIO0_12 —** General-purpose digital input/output pin.
					I/O	**SPI0_MOSI —** Master Out Slave in for SPI0.
					O	**U1_TXD —** Transmitter output for USART1.
					O	**CT32B2_MAT3 —** 32-bit CT32B2 match output 3.
					I	**R —** Reserved.
PIO0_13	G7	48	[2]	PU	I/O	**PIO0_13 —** General-purpose digital input/output pin.
					I/O	**SPI0_MISO —** Master In Slave Out for SPI0.
					O	**SCT0_OUT4 —** SCT0 output 4. PWM output 4.
					O	**CT32B2_MAT0 —** 32-bit CT32B2 match output 0.
					I	**R —** Reserved.
PIO0_14/TCK	F6	49	[2]	PU	I/O	**PIO0_14 —** General-purpose digital input/output pin. In boundary scan mode: TCK (Test Clock).
					I/O	**SPI0_SSEL0 —** Slave Select 0 for SPI0.
					O	**SCT0_OUT5 —** SCT0 output 5. PWM output 5.
					O	**CT32B2_MAT1 —** 32-bit CT32B2 match output 1.
					I	**R —** Reserved.
PIO0_15/TDO	G6	50	[2]	PU	I/O	**PIO0_15 —** General-purpose digital input/output pin. In boundary scan mode: TDO (Test Data Out).
					I/O	**SPI0_SSEL1 —** Slave Select 1 for SPI0.
					I/O	**SWO —** Serial wire trace output.
					O	**CT32B2_MAT2 —** 32-bit CT32B2 match output 2.
					I	**R —** Reserved.
SWCLK/ PIO0_16	F5	52	[2]	PU	I/O	**PIO0_16 —** General-purpose digital input/output pin. After booting, this pin is connected to the SWCLK.
					I/O	**SPI0_SSEL2 —** Slave Select 2 for SPI0.
					I	**$\overline{\text{U1\_CTS}}$ —** Clear To Send input for USART1.
					O	**CT32B3_MAT1 —** 32-bit CT32B3 match output 1.
					I	**R —** Reserved.
					I/O	**SWCLK —** Serial Wire Clock. This is the default function after booting.
SWDIO/ PIO0_17	G5	53	[2]	PU	I/O	**PIO0_17 —** General-purpose digital input/output pin. After booting, this pin is connected to SWDIO.
					I/O	**SPI0_SSEL3 —** Slave Select 3 for SPI0.
					O	**$\overline{\text{U1\_RTS}}$ —** Request To Send output for USART1.
					O	**CT32B3_MAT2 —** 32-bit CT32B3 match output 2.
					I	**R —** Reserved.
					I/O	**SWDIO —** Serial Wire Debug I/O. This is the default function after booting.

Table 4. Pin description *…continued*

Symbol	WLCSP49	LQFP64		Reset state [1]	Type [6]	Description
PIO0_18/TRST	G4	58	[2]	PU	I/O	**PIO0_18 —** General-purpose digital input/output pin. In boundary scan mode: TRST (Test Reset).
					O	**U3_TXD —** Transmitter output for USART3.
					O	**SCT0_OUT0 —** SCT0 output 0. PWM output 0.
					O	**CT32B0_MAT0 —** 32-bit CT32B0 match output 0.
					I	**R —** Reserved.
PIO0_19/TDI	G3	59	[2]	PU	I/O	**PIO0_19 —** General-purpose digital input/output pin. In boundary scan mode: TDI (Test Data In).
					I/O	**U3_SCLK —** USART3 clock in synchronous USART mode.
					O	**SCT0_OUT1 —** SCT0 output 1. PWM output 1.
					O	**CT32B0_MAT1 —** 32-bit CT32B0 match output 1.
					I	**R —** Reserved.
PIO0_20/TMS	F3	60	[2]	PU	I/O	**PIO0_20 —** General-purpose digital input/output pin. In boundary scan mode: TMS (Test Mode Select).
					I	**U3_RXD —** Receiver input for USART3.
					I/O	**U0_SCLK —** USART0 clock in synchronous USART mode.
					I	**CT32B3_CAP0 —** 32-bit CT32B3 capture input 0.
					I	**R —** Reserved.
PIO0_21	E3	61	[2]	PU	I/O	**PIO0_21 —** General-purpose digital input/output pin.
					O	**CLKOUT —** Clock output pin.
					O	**U0_TXD —** Transmitter output for USART0.
					O	**CT32B3_MAT0 —** 32-bit CT32B3 match output 0.
					I	**R —** Reserved.
PIO0_22	G2	63	[2]	PU	I/O	**PIO0_22 —** General-purpose digital input/output pin.
					I	**CLKIN —** Clock input.
					I	**U0_RXD —** Receiver input for USART0.
					O	**CT32B3_MAT3 —** 32-bit CT32B3 match output 3.
					I	**R —** Reserved.
PIO0_23	F2	1	[3]	Z	I/O	**PIO0_23 —** General-purpose digital input/output pin.
					I/O	**I2C0_SCL —** I^2C0 clock input/output.
					I	**R —** Reserved.
					I	**CT32B0_CAP0 —** 32-bit CT32B0 capture input 0.
					I	**R —** Reserved.

Table 4. Pin description *…continued*

Symbol	WLCSP49	LQFP64		Reset state [1]	Type [6]	Description
PIO1_3/ ADC0_6	B2	17	[4]	PU	I/O; AI	**PIO1_3/ADC0_6 —** General-purpose digital input/output pin (default). ADC input channel 6 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					I/O	**SPI1_SSEL2 —** Slave Select 2 for SPI1.
					O	**SCT0_OUT6 —** SCT0 output 6.
					I	**R —** Reserved.
					I/O	**SPI0_SCK —** Serial clock for SPI0.
					I	**CT32B0_CAP1 —** 32-bit CT32B0 capture input 1.
PIO1_4/ ADC0_7	A2	18	[4]	PU	I/O; AI	**PIO1_4/ADC0_7 —** General-purpose digital input/output pin (default). ADC input channel 7 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					I/O	**SPI1_SSEL1 —** Slave Select 1 for SPI1.
					O	**SCT0_OUT7 —** SCT0 output 7.
					I	**R —** Reserved.
					I/O	**SPI0_MISO —** Master In Slave Out for SPI0.
					O	**CT32B0_MAT1 —** 32-bit CT32B0 match output 1.
PIO1_5/ ADC0_8	B3	19	[4]	PU	I/O; AI	**PIO1_5/ADC0_8 —** General-purpose digital input/output pin (default). ADC input channel 8 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					I/O	**SPI1_SSEL0 —** Slave Select 0 for SPI1.
					I	**CT32B1_CAP0 —** 32-bit CT32B1 capture input 0.
					I	**R —** Reserved.
					O	**CT32B1_MAT3 —** 32-bit CT32B1 match output 3.
					I	**R —** Reserved.
PIO1_6/ ADC0_9	A5	26	[4]	PU	I/O; AI	**PIO1_6/ADC0_9 —** General-purpose digital input/output pin (default). ADC input channel 9 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					I/O	**SPI1_SCK —** Serial clock for SPI1.
					I	**CT32B1_CAP2 —** 32-bit CT32B1 capture input 2.
					-	**R —** Reserved.
					O	**CT32B1_MAT2 —** 32-bit CT32B1 match output 2.
					I	**R —** Reserved.

Table 4. Pin description *…continued*

Symbol	WLCSP49	LQFP64		Reset state [1]	Type [6]	Description
PIO1_7/ ADC0_10	B5	27	[4]	PU	I/O; AI	**PIO1_7/ADC0_10 —** General-purpose digital input/output pin (default). ADC input channel 10 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					I/O	**SPI1_MOSI —** Master Out Slave in for SPI1.
					O	**CT32B1_MAT2 —** 32-bit CT32B1 match output 2.
					-	**R —** Reserved.
					I	**CT32B1_CAP2 —** 32-bit CT32B1 capture input 2.
					I	**R —** Reserved.
PIO1_8/ ADC0_11	C5	28	[4]	PU	I/O; AI	**PIO1_8/ADC0_11 —** General-purpose digital input/output pin (default). ADC input channel 11 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					I/O	**SPI1_MISO —** Master In Slave Out for SPI1.
					O	**CT32B1_MAT3 —** 32-bit CT32B1 match output 3.
					I	**R —** Reserved.
					I	**CT32B1_CAP3 —** 32-bit CT32B1 capture input 3.
					I	**R —** Reserved.
PIO1_9	-	29	[2]	PU	I/O	**PIO1_9 —** General-purpose digital input/output pin.
					I	**R —** Reserved.
					I/O	**SPI0_MOSI —** Master Out Slave In for SPI0.
					I	**CT32B0_CAP2 —** 32-bit CT32B0 capture input 2.
PIO1_10	-	30	[2]	PU	I/O	**PIO1_10 —** General-purpose digital input/output pin.
					I	**R —** Reserved.
					O	**U1_TXD —** Transmitter output for USART1.
					O	**SCT0_OUT4 —** SCT0 output 4.
PIO1_11	-	42	[2]	PU	I/O	**PIO1_11 —** General-purpose digital input/output pin.
					I	**R —** Reserved.
					O	**$\overline{\text{U1\_RTS}}$ —** Request To Send output for USART1.
					I	**CT32B1_CAP0 —** 32-bit CT32B1 capture input 0.
PIO1_12	-	51	[2]	PU	I/O	**PIO1_12 —** General-purpose digital input/output pin.
					I	**R —** Reserved.
					I	**U3_RXD —** Receiver input for USART3.
					O	**CT32B1_MAT0 —** 32-bit CT32B1 match output 0.
					I/O	**SPI1_SCK —** Serial clock for SPI1.
PIO1_13	-	54	[2]	PU	I/O	**PIO1_13 —** General-purpose digital input/output pin.
					I	**R —** Reserved.
					O	**U3_TXD —** Transmitter output for USART3.
					O	**CT32B1_MAT1 —** 32-bit CT32B1 match output 1.
					I/O	**SPI1_MOSI —** Master Out Slave In for SPI1.

- Pattern match engine:
  - Up to eight pins can be selected from all digital pins on ports 0 and 1 to contribute to a boolean expression. The boolean expression consists of specified levels and/or transitions on various combinations of these pins.
  - Each bit slice minterm (product term) comprising of the specified boolean expression can generate its own, dedicated interrupt request.
  - Any occurrence of a pattern match can also be programmed to generate an RXEV notification to the CPU. The RXEV signal can be connected to a pin.
  - Pattern match can be used in conjunction with software to create complex state machines based on pin inputs.
  - Pattern match engine facilities wake-up only from active and sleep modes.

7.15 AHB peripherals

7.15.1 DMA controller

The DMA controller allows peripheral-to memory, memory-to-peripheral, and memory-to-memory transactions. Each DMA stream provides unidirectional DMA transfers for a single source and destination.

7.15.1.1 Features

- 22 channels, 21 of which are connected to peripheral DMA requests. These come from the USART, SPI, and I^2C peripherals. One spare channels has no DMA request connected, and can be used for functions such as memory-to-memory moves.
- DMA operations can be triggered by on- or off-chip events. Each DMA channel can select one trigger input from 20 sources. Trigger sources include ADC interrupts, Timer interrupts, pin interrupts, and the SCT DMA request lines.
- Priority is user selectable for each channel.
- Continuous priority arbitration.
- Address cache.
- Efficient use of data bus.
- Supports single transfers up to 1,024 words.
- Address increment options allow packing and/or unpacking data.

7.16 Digital serial peripherals

7.16.1 USART

7.16.1.1 Features

- Synchronous mode with master or slave operation. Includes data phase selection and continuous clock option.
- Maximum bit rates of 6.25 Mbit/s in asynchronous mode.
- Maximum supported bit rate of 24 Mbit/s for USART master and slave synchronous modes.
- 7, 8, or 9 data bits and 1 or 2 stop bits.

7.18.2.1 Features

- Two 16-bit counters or one 32-bit counter.
- Counter(s) clocked by bus clock or selected input.
- Up counter(s) or up-down counter(s).
- State variable allows sequencing across multiple counter cycles.
- Event combines input or output condition and/or counter match in a specified state.
- Events control outputs, interrupts, and the SCT states.
  - Match register 0 can be used as an automatic limit.
  - In bi-directional mode, events can be enabled based on the count direction.
  - Match events can be held until another qualifying event occurs.
- Selected event(s) can limit, halt, start, or stop a counter.
- Supports:
  - 8 inputs (6 GPIO pins, ADC0_THCMP_IRQ, DEBUG_HALTED)
  - up to 8 outputs
  - 13 match/capture registers
  - 13 events
  - 13 states
- PWM capabilities including dead time and emergency abort functions

7.18.3 Windowed WatchDog Timer (WWDT)

The purpose of the watchdog is to reset the controller if software fails to periodically service it within a programmable time window.

7.18.3.1 Features

- Internally resets chip if not reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time-out period, both programmable.
- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Programmable 24-bit timer with internal fixed pre-scaler.
- Selectable time period from 1,024 watchdog clocks ($T_{WDCLK} \times 256 \times 4$) to over 67 million watchdog clocks ($T_{WDCLK} \times 2^{24} \times 4$) in increments of 4 watchdog clocks.
- “Safe” watchdog operation. Once enabled, requires a hardware reset or a Watchdog reset to be disabled.
- Incorrect feed sequence causes immediate watchdog event if enabled.
- The watchdog reload value can optionally be protected such that it can only be changed after the “warning interrupt” time is reached.
- Flag to indicate Watchdog reset.
- The Watchdog clock (WDCLK) source is the fixed 500 kHz clock (+/- 40%) provided by the low-power watchdog oscillator.
- The Watchdog timer can be configured to run in deep sleep or power down mode.

- Burst conversion mode for single or multiple inputs.
- Synchronous or asynchronous operation. Asynchronous operation maximizes flexibility in choosing the ADC clock frequency, Synchronous mode minimizes trigger latency and can eliminate uncertainty and jitter in response to a trigger.

7.20 System control

7.20.1 Clock sources

The LPC5410x supports two external and three internal clock sources:

- The Internal RC (IRC).
- Watchdog oscillator (WDOSC).
- External clock source from the digital I/O pin CLKIN.
- External RTC 32 KHz clock.
- Output of the system PLL.

7.20.1.1 Internal RC oscillator (IRC)

The IRC can be used as the clock that drives the system PLL and subsequently the CPU. The nominal IRC frequency is 12 MHz.

Upon power-up or any chip reset, the LPC5410x uses the IRC as the clock source. Software may later switch to one of the other available clock sources.

7.20.1.2 Watchdog oscillator (WDOSC)

The watchdog oscillator is a low-power internal oscillator. The WDOSC can be used to provide a clock to the WWDT and to the entire chip. The nominal output frequency is 500 kHz.

7.20.1.3 Clock input pin (CLKIN)

An external square-wave clock source (up to 25 MHz) can be supplied on the digital I/O pin CLKIN.

7.20.2 System PLL

The system PLL accepts an input clock frequency in the range of 32 kHz to 12 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO).

The PLL can be enabled or disabled by software.

7.20.3 Clock Generation

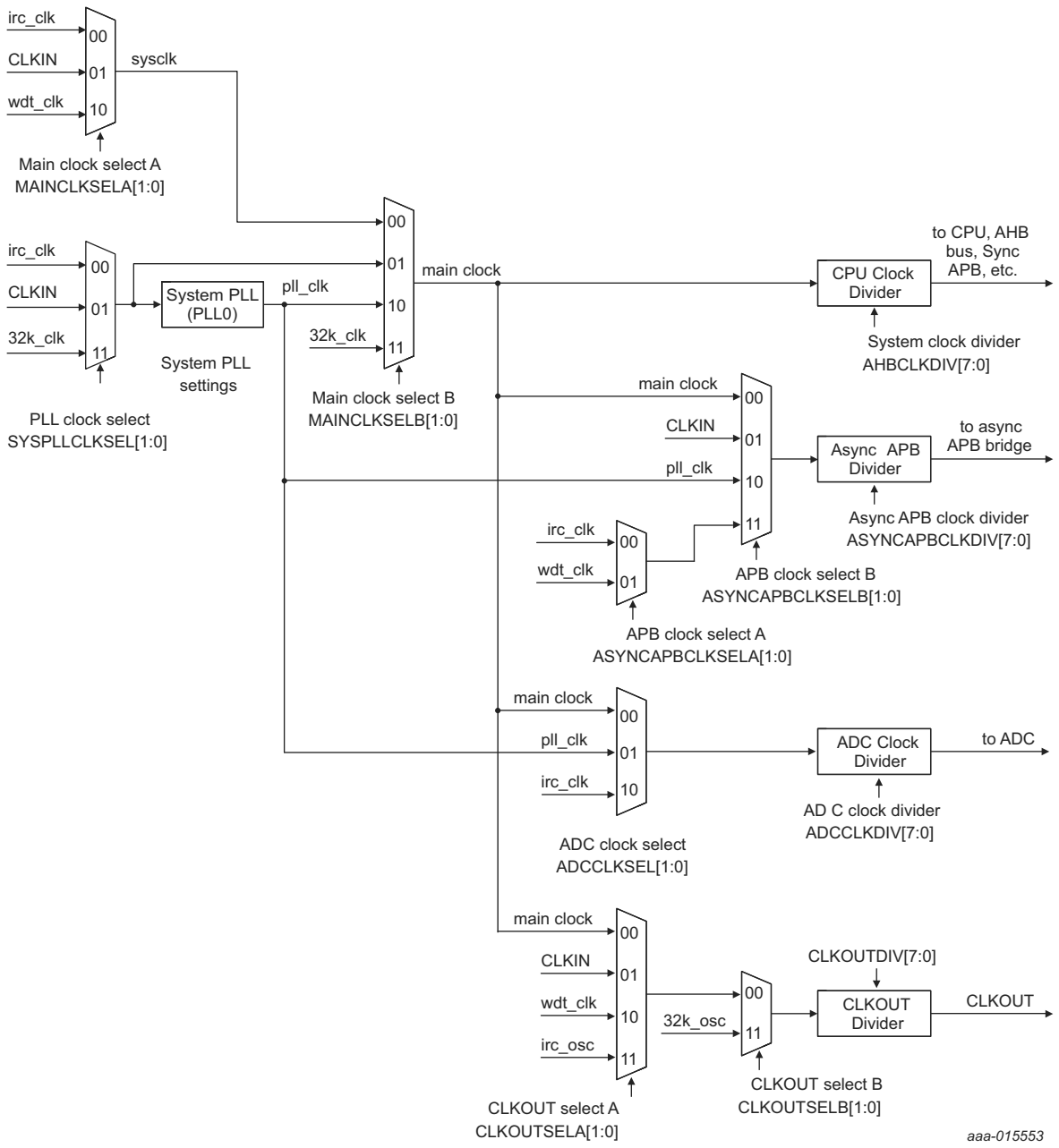


Fig 7. LPC5410x clock generation

7.20.4 Power control

The LPC5410x support a variety of power control features. In Active mode, when the chip is running, power and clocks to selected peripherals can be optimized for power consumption. In addition, there are four special modes of processor power reduction with different peripherals running: Sleep mode, deep sleep mode, power down mode, and deep power-down mode, activated by the power mode configure API.

[8] An ADC input voltage above 3.6 V can be applied for a short time without leading to immediate, unrecoverable failure. Accumulated exposure to elevated voltages at 4.6 V must be less than 10^6 s total over the lifetime of the device. Applying an elevated voltage to the ADC inputs for a long time affects the reliability of the device and reduces its lifetime.

[9] It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

[10] Dependent on package type.

10. Static characteristics

10.1 General operating conditions

Table 9. General operating conditions

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{clk}	clock frequency	internal CPU/system clock		-	-	100	MHz
V_{DD}	supply voltage (core and external rail)			1.62	-	3.6	V
V_{DDA}	analog supply voltage		[1]	1.62	-	3.6	V
V_{refp}	ADC positive reference voltage	$V_{DDA} \geq 2$ V	[2]	2.0	-	V_{DDA}	V
		$V_{DDA} < 2$ V		V_{DDA}	-	V_{DDA}	V
RTC oscillator pins							
$V_{i(rtcx)}$	32 kHz oscillator input voltage	on pin RTCXIN		−0.5	-	+3.6	V
$V_{o(rtcx)}$	32 kHz oscillator output voltage	on pin RTCXOUT		−0.5	-	+3.6	V

[1] The V_{DD} voltage must be equal or lower than the voltage level on V_{DDA}.

[2] The V_{refp} voltage must not exceed the voltage level on V_{DDA}.

10.2 CoreMark data

Table 10. CoreMark score

T_{amb} = 25 °C, V_{DD} = 3.3V

Parameter	Conditions		Typ	Unit
ARM Cortex-M4 in active mode; ARM Cortex-M0+ in sleep mode				
CoreMark score	CoreMark code executed from SRAM; CCLK = 12 MHz	[1][3][4][5]	2.6	(Iterations/s) / MHz
	CCLK = 48 MHz	[2][3][4][5]	2.6	(Iterations/s) / MHz
	CCLK = 84 MHz	[2][3][4][5]	2.6	(Iterations/s) / MHz
	CCLK = 100 MHz	[2][3][4][5]	2.6	(Iterations/s) / MHz
CoreMark score	CoreMark code executed from flash; CCLK = 12 MHz; 1 system clock flash access time.	[1][3][4][6]	2.6	(Iterations/s) / MHz
	CCLK = 48 MHz; 3 system clock flash access time.	[2][3][4][6]	2.4	(Iterations/s) / MHz
	CCLK = 84 MHz; 5 system clock flash access time.	[2][3][4][6]	2.3	(Iterations/s) / MHz
	CCLK = 100 MHz; 6 system clock flash access time.	[2][3][4][6]	2.2	(Iterations/s) / MHz

[1] Clock source 12 MHz IRC. PLL disabled.

[2] Clock source 12 MHz IRC. PLL enabled.

[3] Characterized through bench measurements using typical samples.

[4] Compiler settings: Keil µVision v.5.12, optimization level 3, optimized for time on.

10.3 Power consumption

Power measurements in Active, sleep, deep sleep, and power down modes were performed under the following conditions:

- Configure all pins as GPIO with pull-up resistor disabled in the IOCON block.
- Configure GPIO pins as outputs using the GPIO DIR register.
- Write 1 to the GPIO CLR register to drive the outputs LOW.
- All peripherals disabled.

Table 11. Static characteristics: Power consumption in active and sleep modes

T_{amb} = −40 °C to +105 °C, unless otherwise specified.1.62 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
ARM Cortex-M0+ in active mode; ARM Cortex-M4 in sleep mode							
I_{DD}	supply current	CoreMark code executed from SRAM; flash powered down CCLK = 12 MHz	[2][4][6]	-	1.2	-	mA
		CCLK = 48 MHz	[3][4][6]	-	3.0	-	mA
		CCLK = 84 MHz	[3][4][6]	-	4.5	-	mA
		CCLK = 100 MHz	[3][4][6]	-	5.5	-	mA
I_{DD}	supply current	CoreMark code executed from flash; CCLK = 12 MHz; 1 system clock flash access time.	[2][4][6]	-	1.5	-	mA
		CCLK = 48 MHz; 3 system clock flash access time.	[3][4][6]	-	3.6	-	mA
		CCLK = 84 MHz; 6 system clock flash access time.	[3][4][6]	-	5.4	-	mA
		CCLK = 100 MHz; 7 system clock flash access time.	[3][4][6]	-	6.6	-	mA
I_{DD}	supply current	Calculating Fibonacci numbers executed from flash; CCLK = 12 MHz	[2][4][5]	-	1.5	-	mA
		CCLK = 84 MHz	[3][4][5]	-	6.2	-	mA
		CCLK = 96 MHz	[3][4][5]	-	7.2	-	mA

[2] The wake-up time measured is the time between when a GPIO input pin is triggered to wake the device up from the low power modes and from when a GPIO output pin is set in the interrupt service routine (ISR) wake-up handler. Measurements are based on using the power library provided in the LPC5410x LPCOpen software platform version v.3.04.

[3] IRC enabled, all peripherals off.

[4] RTC disabled. Wake-up from deep power-down causes the part to go through entire reset process. The wake-up time measured is the time between when the $\overline{\text{RESET}}$ pin is triggered to wake the device up and when a GPIO output pin is set in the reset handler.

11.10 SPI interfaces

The actual SPI bit rate depends on the delays introduced by the external trace, the external device, system clock (CCLK), and capacitive loading. Excluding delays introduced by external device and PCB, the maximum supported bit rate for SPI master mode is 48 Mbit/s, and the maximum supported bit rate for SPI slave mode is 21 Mbit/s.

Table 27. SPI dynamic characteristics[1]

T_{amb} = −40 °C to 105 °C; C_L = 30 pF balanced loading on all pins; SLEW = standard mode. Parameters sampled at the 50 % level of the rising or falling edge.

Symbol	Parameter	Conditions		Min	Max	Unit
SPI master 1.62V ≤ VDD ≤ 2.0 V						
t_{DS}	data set-up time	CCLK = 1 MHz to 12 MHz		0	-	ns
		CCLK = 48 MHz to 60 MHz		0	-	ns
		CCLK = 96 MHz		0	-	ns
t_{DH}	data hold time	CCLK = 1 MHz to 12 MHz		14	-	ns
		CCLK = 48 MHz to 60 MHz		12	-	ns
		CCLK = 96 MHz		9	-	ns
$t_{v(Q)}$	data output valid time	CCLK = 1 MHz to 12 MHz		0	7	ns
		CCLK = 48 MHz to 60 MHz		0	2	ns
		CCLK = 96 MHz		0	2	ns
SPI slave 1.62V ≤ VDD ≤ 2.0 V						
t_{DS}	data set-up time	CCLK = 1 MHz to 12 MHz		22	-	ns
		CCLK = 48 MHz to 60 MHz		4	-	ns
		CCLK = 96 MHz		4	-	ns
t_{DH}	data hold time	CCLK = 1 MHz to 12 MHz		0	-	ns
		CCLK = 48 MHz to 60 MHz		0	-	ns
		CCLK = 96 MHz		0	-	ns
$t_{v(Q)}$	data output valid time	CCLK = 1 MHz to 12 MHz		46	70	ns
		CCLK = 48 MHz to 60 MHz		30	37	ns
		CCLK = 96 MHz		30	36	ns
SPI master 2.7 V ≤ VDD ≤ 3.6 V						
t_{DS}	data set-up time	CCLK = 1 MHz to 12 MHz		0	-	ns
		CCLK = 48 MHz to 60 MHz		0	-	ns
		CCLK = 96 MHz		0	-	ns
t_{DH}	data hold time	CCLK = 1 MHz to 12 MHz		10	-	ns
		CCLK = 48 MHz to 60 MHz		8	-	ns
		CCLK = 96 MHz		7	-	ns
$t_{v(Q)}$	data output valid time	CCLK = 1 MHz to 12 MHz		0	6	ns
		CCLK = 48 MHz to 60 MHz		0	1	ns
		CCLK = 96 MHz		0	1	ns
SPI slave 2.7V ≤ VDD ≤ 3.6 V						
t_{DS}	data set-up time	CCLK = 1 MHz to 12 MHz		21	-	ns
		CCLK = 48 MHz to 60 MHz		4	-	ns
		CCLK = 96 MHz		3	-	ns

Table 32. ADC sampling times[1] *...continued*

-40 °C ≤ T_{amb} ≤ 85 °C; 1.62 V ≤ V_{DDA} ≤ 3.6 V; 1.62 V ≤ V_{DD} ≤ 3.6 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
ADC inputs ADC_11 to ADC_6 (slow channels); ADC resolution = 10 bit							
t_s	sampling time	Z_o < 0.05 kΩ	[3]	35	-	-	ns
		0.05 kΩ ≤ Z_o < 0.1 kΩ		38	-	-	ns
		0.1 kΩ ≤ Z_o < 0.2 kΩ		40	-	-	ns
		0.2 kΩ ≤ Z_o < 0.5 kΩ		46	-	-	ns
		0.5 kΩ ≤ Z_o < 1 kΩ		61	-	-	ns
		1 kΩ ≤ Z_o < 5 kΩ		86	-	-	ns
ADC inputs ADC_11 to ADC_6 (slow channels); ADC resolution = 8 bit							
t_s	sampling time	Z_o < 0.05 kΩ	[3]	27	-	-	ns
		0.05 kΩ ≤ Z_o < 0.1 kΩ		29	-	-	ns
		0.1 kΩ ≤ Z_o < 0.2 kΩ		32	-	-	ns
		0.2 kΩ ≤ Z_o < 0.5 kΩ		36	-	-	ns
		0.5 kΩ ≤ Z_o < 1 kΩ		48	-	-	ns
		1 kΩ ≤ Z_o < 5 kΩ		69	-	-	ns
ADC inputs ADC_11 to ADC_6 (slow channels); ADC resolution = 6 bit							
t_s	sampling time	Z_o < 0.05 kΩ	[3]	20	-	-	ns
		0.05 kΩ ≤ Z_o < 0.1 kΩ		22	-	-	ns
		0.1 kΩ ≤ Z_o < 0.2 kΩ		23	-	-	ns
		0.2 kΩ ≤ Z_o < 0.5 kΩ		26	-	-	ns
		0.5 kΩ ≤ Z_o < 1 kΩ		36	-	-	ns
		1 kΩ ≤ Z_o < 5 kΩ		51	-	-	ns

[1] Characterized through simulation. Not tested in production.

[2] The ADC default sampling time is 2.5 ADC clock cycles. To match a given analog source output impedance, the sampling time can be extended by adding up to seven ADC clock cycles for a maximum sampling time of 9.5 ADC clock cycles. See the TSAMP bits in the ADC CTRL register.

[3] Z_o = analog source output impedance.

12.2.1 ADC input impedance

Figure 25 shows the ADC input impedance. In this figure:

- ADCx represents slow ADC input channels 6 to 11.
- ADCy represents fast ADC input channels 0 to 5.
- R_1 and R_{sw} are the switch-on resistance on the ADC input channel.
- If fast channels (ADC inputs 0 to 5) are selected, the ADC input signal goes through R_{sw} to the sampling capacitor (C_{ia}).
- If slow channels (ADC inputs 6 to 11) are selected, the ADC input signal goes through $R_1 + R_{sw}$ to the sampling capacitor (C_{ia}).
- Typical values, R_1 = 487 Ω, R_{sw} = 278 Ω
- See Table 16 for C_{io}.
- See Table 31 for C_{ia}.

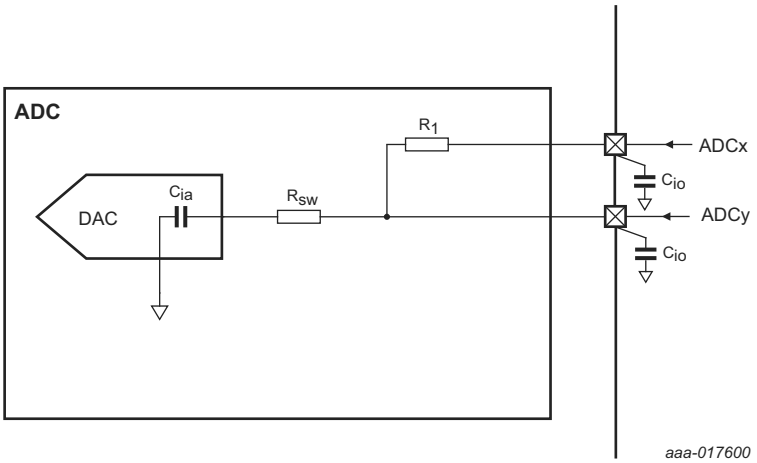
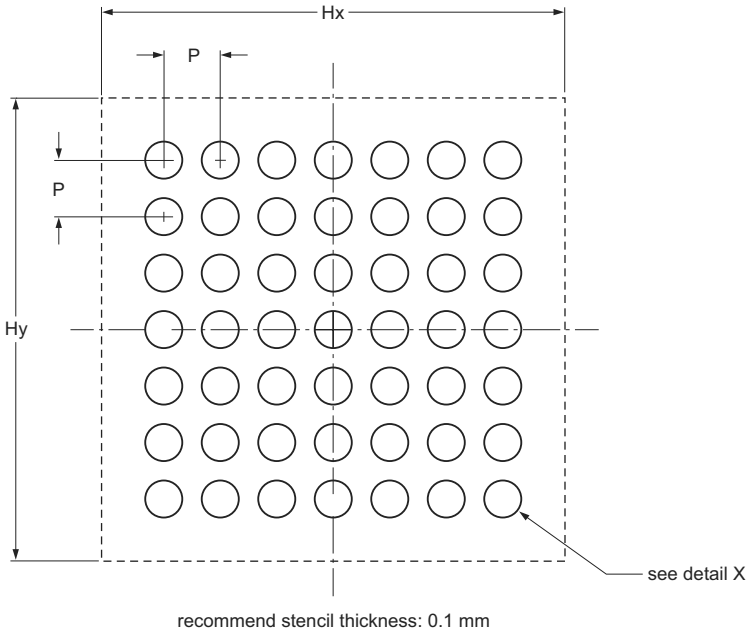
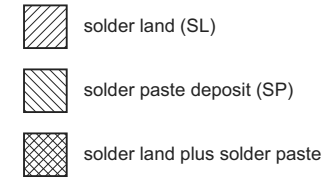


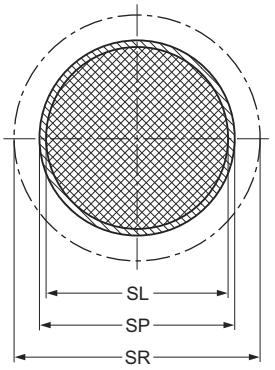
Fig 25. ADC input impedance

15. Soldering

Footprint information for reflow soldering of WLCSP49 package **LPC5410_NSMD**







detail X

Dimensions in mm

P	SL	SP	SR	Hx	Hy
0.4	0.24	0.27	0.31	3.5	3.5

wlcsp49_lpc5410_fr

Fig 32. WLCSP49 Soldering footprint

Table 36. Revision history *…continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
Modification:	• Updated Table 18 “Flash characteristics”: For N_{endu} conditions, removed the row with page erase/program; page in small sector 10000 and removed the word large so that it is "page erase/program;page in a sector". • Updated Section 7.16.1 “USART” features: changed maximum bit rates to 6.25 Mbit/s in asynchronous mode.			
LPC5410x v2.2	20151222	Product data sheet	201512007I	LPC5410x v2.1
Modification:	• Updated Section 11.6 “IRC”, Table 23 “Dynamic characteristic: IRC oscillator” for IRC frequency tolerance improvement over temperature. • Added boot code version and device revision. See Section 4 “Marking”. • Added the abbreviation ISP to the Remark: This pin is also used to force In-System Programming mode (ISP) after device reset. See the LPC5410x User Manual (Boot Process chapter) for details to PIO0_31. See Table 4 “Pin description”. • Removed 164 uA PLL spec in peripheral power consumption table, Table 15 “Typical AHB/APB peripheral power consumption[3][4][5]”. • Added Table 21 “PLL lock times and current”. • Updated Figure 10 “Deep sleep mode: Typical supply current IDD versus temperature for different supply voltages VDD”, Figure 11 “Power down mode: Typical supply current IDD versus temperature for different supply voltages VDD”, and Figure 12 “Deep power-down mode: Typical supply current IDD versus temperature for different supply voltages VDD”. • Updated Table 12 “Static characteristics: Power consumption in deep sleep, power down, and deep power-down modes”: added max values to Deep sleep mode at 25 °C and 105 °C, Power down mode at 25 °C and 105 °C. Changed typ and max values for Deep power-down mode RTC oscillator input grounded (RTC oscillator disabled) at 25 °C; was: typ = 84 nA, max = 240 nA; now: typ = 160 nA, max = 340 nA. • Updated Table 13 “Static characteristics: Power consumption in deep sleep, power down, and deep power-down modes”: added max values to Deep sleep mode at 25 °C and 105 °C, Power down mode at 25 °C and 105 °C. Changed typ and max values for Deep power-down mode RTC oscillator input grounded (RTC oscillator disabled) at 25 °C; was: typ = 135 nA, max = 470 nA; now: typ = 200 nA, max = 570 nA. • Updated Table 7 “Limiting values”; VESD, electrostatic discharge voltage, human body model; all pins value to 4000 V; was 5000 V. • Updated Table 31 “12-bit ADC static characteristics”: ED differential linearity error, VDDA = VREFP = 1.62 V and 3.6 V, typ value ±3 and ±2; $EL_{(adj)}$ integral non-linearity, VDDA = VREFP = 1.62 V, typ value ±5; $V_{err(FS)}$ full-scale error voltage VDDA = VREFP = 1.62 V and 3.6 V, typ value to ±3			
LPC5410x v2.1	20150701	Product data sheet	-	LPC5410x v2.0
Modification:	• Updated Figure 3 “LPC5410x Block diagram”. Corrected Sync APB bridge to Async APB bridge. • Updated external clock input for clock frequencies of up to 24 MHz to 25 MHz in Section 2 “Features and benefits”. • Updated Table 12 “Static characteristics: Power consumption in deep sleep, power down, and deep power-down modes”. Fixed the unit of the max value from nA to μA for IDD in deep power-down mode; RTC oscillator input grounded (RTC oscillator disabled), T_{amb} = 105 °C.			

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