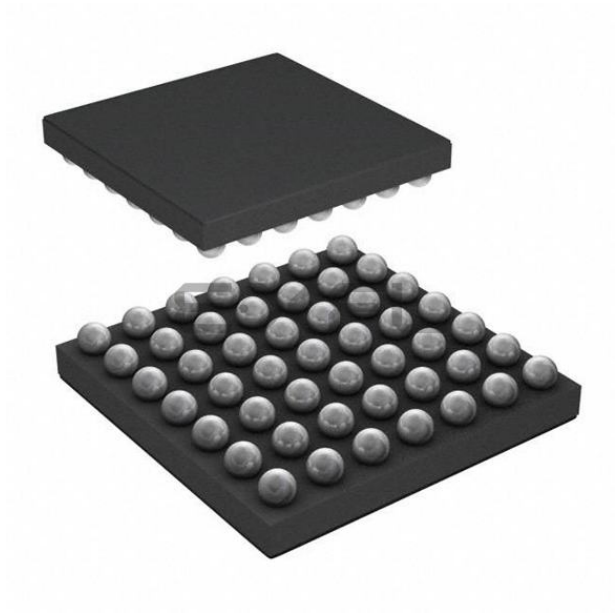

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	39
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	104K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	49-UFBGA, WLCSP
Supplier Device Package	49-WLCSP (3.29x3.29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc54101j256uk49z

Table 4. Pin description *…continued*

Symbol	WLCSP49	LQFP64		Reset state [1]	Type [6]	Description
PIO0_24	F1	2	[3]	Z	I/O	**PIO0_24 —** General-purpose digital input/output pin.
					I/O	**I2C0_SDA —** I^2C0 data input/output.
					I	**R —** Reserved.
					I	**CT32B0_CAP1 —** 32-bit CT32B0 capture input 1.
					I	**R —** Reserved.
					O	**CT32B0_MAT0 —** 32-bit CT32B0 match output 0.
PIO0_25	E2	3	[3]	Z	I/O	**PIO0_25 —** General-purpose digital input/output pin.
					I/O	**I2C1_SCL —** I^2C1 clock input/output.
					I	**$\overline{\text{U1\_CTS}}$ —** Clear To Send input for USART1.
					I	**CT32B0_CAP2 —** 32-bit CT32B0 capture input 2.
					I	**R —** Reserved.
					I	**CT32B1_CAP1 —** 32-bit CT32B1 capture input 1.
PIO0_26	E1	4	[3]	Z	I/O	**PIO0_26 —** General-purpose digital input/output pin.
					I/O	**I2C1_SDA —** I^2C1 data input/output.
					I	**R —** Reserved.
					I	**CT32B0_CAP3 —** 32-bit CT32B0 capture input 3.
					I	**R —** Reserved.
PIO0_27	D2	5	[3]	Z	I/O	**PIO0_27 —** General-purpose digital input/output pin.
					I/O	**I2C2_SCL —** I^2C2 clock input/output.
					I	**R —** Reserved.
					I	**CT32B2_CAP0 —** 32-bit CT32B2 capture input 0.
					I	**R —** Reserved.
PIO0_28	D1	6	[3]	Z	I/O	**PIO0_28 —** General-purpose digital input/output pin.
					I/O	**I2C2_SDA —** I^2C2 data input/output.
					I	**R —** Reserved.
					O	**CT32B2_MAT0 —** 32-bit CT32B2 match output 0.
					I	**R —** Reserved.
PIO0_29/ ADC0_0	D3	11	[4]	PU	I/O; AI	**PIO0_29/ADC0_0 —** General-purpose digital input/output pin (default). ADC input channel 0 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					O	**SCT0_OUT2 —** SCT0 output 2.
					O	**CT32B0_MAT3 —** 32-bit CT32B0 match output 3.
					I	**R —** Reserved.
					I	**CT32B0_CAP1 —** 32-bit CT32B0 capture input 1.
					O	**CT32B0_MAT1 —** 32-bit CT32B0 match output 1.

Table 4. Pin description *…continued*

Symbol	WLCSP49	LQFP64		Reset state [1]	Type [6]	Description
PIO1_7/ ADC0_10	B5	27	[4]	PU	I/O; AI	**PIO1_7/ADC0_10 —** General-purpose digital input/output pin (default). ADC input channel 10 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					I/O	**SPI1_MOSI —** Master Out Slave in for SPI1.
					O	**CT32B1_MAT2 —** 32-bit CT32B1 match output 2.
					-	**R —** Reserved.
					I	**CT32B1_CAP2 —** 32-bit CT32B1 capture input 2.
					I	**R —** Reserved.
PIO1_8/ ADC0_11	C5	28	[4]	PU	I/O; AI	**PIO1_8/ADC0_11 —** General-purpose digital input/output pin (default). ADC input channel 11 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					I/O	**SPI1_MISO —** Master In Slave Out for SPI1.
					O	**CT32B1_MAT3 —** 32-bit CT32B1 match output 3.
					I	**R —** Reserved.
					I	**CT32B1_CAP3 —** 32-bit CT32B1 capture input 3.
					I	**R —** Reserved.
PIO1_9	-	29	[2]	PU	I/O	**PIO1_9 —** General-purpose digital input/output pin.
					I	**R —** Reserved.
					I/O	**SPI0_MOSI —** Master Out Slave In for SPI0.
					I	**CT32B0_CAP2 —** 32-bit CT32B0 capture input 2.
PIO1_10	-	30	[2]	PU	I/O	**PIO1_10 —** General-purpose digital input/output pin.
					I	**R —** Reserved.
					O	**U1_TXD —** Transmitter output for USART1.
					O	**SCT0_OUT4 —** SCT0 output 4.
PIO1_11	-	42	[2]	PU	I/O	**PIO1_11 —** General-purpose digital input/output pin.
					I	**R —** Reserved.
					O	**$\overline{\text{U1\_RTS}}$ —** Request To Send output for USART1.
					I	**CT32B1_CAP0 —** 32-bit CT32B1 capture input 0.
PIO1_12	-	51	[2]	PU	I/O	**PIO1_12 —** General-purpose digital input/output pin.
					I	**R —** Reserved.
					I	**U3_RXD —** Receiver input for USART3.
					O	**CT32B1_MAT0 —** 32-bit CT32B1 match output 0.
					I/O	**SPI1_SCK —** Serial clock for SPI1.
PIO1_13	-	54	[2]	PU	I/O	**PIO1_13 —** General-purpose digital input/output pin.
					I	**R —** Reserved.
					O	**U3_TXD —** Transmitter output for USART3.
					O	**CT32B1_MAT1 —** 32-bit CT32B1 match output 1.
					I/O	**SPI1_MOSI —** Master Out Slave In for SPI1.

6.2.1 Termination of unused pins

Table 5 shows how to terminate pins that are **not** used in the application. In many cases, unused pins should be connected externally or configured correctly by software to minimize the overall power consumption of the part.

Unused pins with GPIO function should be configured as outputs set to LOW with their internal pull-up disabled. To configure a GPIO pin as output and drive it LOW, select the GPIO function in the IOCON register, select output in the GPIO DIR register, and write a 0 to the GPIO PORT register for that pin. Disable the pull-up in the pin's IOCON register.

In addition, it is recommended to configure all GPIO pins that are not bonded out on smaller packages as outputs driven LOW with their internal pull-up disabled.

Table 5. Termination of unused pins

Pin	Default state[1]	Recommended termination of unused pins
$\overline{\text{RESET}}$	I; PU	The $\overline{\text{RESET}}$ pin can be left unconnected if the application does not use it.
all PIOn_m (not open-drain)	I; PU	Can be left unconnected if driven LOW and configured as GPIO output with pull-up disabled by software.
PIOn_m (I2C open-drain)	IA	Can be left unconnected if driven LOW and configured as GPIO output by software.
RTCXIN	-	Connect to ground. When grounded, the RTC oscillator is disabled.
RTCXOUT	-	Can be left unconnected.
VREFP	-	Tie to VDD.
VREFN	-	Tie to VSS.
VDDA	-	Tie to VDD.
VSSA	-	Tie to VSS.

[1] I = Input, IA = Inactive (no pull-up/pull-down enabled), PU = Pull-Up.

6.2.2 Pin states in different power modes

Table 6. Pin states in different power modes

Pin	Active	Sleep	Deep sleep/Power down	Deep power-down
PIOn_m pins (not I2C)	As configured in the IOCON[1]. Default: internal pull-up enabled.			Floating.
PIO0_23 to PIO0_28 (open-drain I2C-bus pins)	As configured in the IOCON[1].			Floating.
$\overline{\text{RESET}}$	Reset function enabled. Default: input, internal pull-up enabled. Reset function disabled.			

[1] Default and programmed pin states are retained in sleep, deep sleep, and power down modes.

7.7.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags.

7.8 System Tick timer (SysTick)

The ARM Cortex-M4 and ARM Cortex-M0+ cores include a system tick timer (SysTick) that is intended to generate a dedicated SYSTICK exception. The clock source for the SysTick can be the system clock or the SYSTICK clock.

7.9 On-chip static RAM

The LPC5410x support 104 kB SRAM with separate bus master access for higher throughput and individual power control for low-power operation.

7.10 On-chip flash

The LPC5410x supports 512 kB of on-chip flash memory.

7.11 On-chip ROM

The 64 kB on-chip ROM contains the boot loader and the following Application Programming Interfaces (API):

- In-System Programming (ISP) and In-Application Programming (IAP) support for flash programming.
- Power control API for configuring power consumption and PLL settings.

- Pattern match engine:
  - Up to eight pins can be selected from all digital pins on ports 0 and 1 to contribute to a boolean expression. The boolean expression consists of specified levels and/or transitions on various combinations of these pins.
  - Each bit slice minterm (product term) comprising of the specified boolean expression can generate its own, dedicated interrupt request.
  - Any occurrence of a pattern match can also be programmed to generate an RXEV notification to the CPU. The RXEV signal can be connected to a pin.
  - Pattern match can be used in conjunction with software to create complex state machines based on pin inputs.
  - Pattern match engine facilities wake-up only from active and sleep modes.

7.15 AHB peripherals

7.15.1 DMA controller

The DMA controller allows peripheral-to memory, memory-to-peripheral, and memory-to-memory transactions. Each DMA stream provides unidirectional DMA transfers for a single source and destination.

7.15.1.1 Features

- 22 channels, 21 of which are connected to peripheral DMA requests. These come from the USART, SPI, and I^2C peripherals. One spare channels has no DMA request connected, and can be used for functions such as memory-to-memory moves.
- DMA operations can be triggered by on- or off-chip events. Each DMA channel can select one trigger input from 20 sources. Trigger sources include ADC interrupts, Timer interrupts, pin interrupts, and the SCT DMA request lines.
- Priority is user selectable for each channel.
- Continuous priority arbitration.
- Address cache.
- Efficient use of data bus.
- Supports single transfers up to 1,024 words.
- Address increment options allow packing and/or unpacking data.

7.16 Digital serial peripherals

7.16.1 USART

7.16.1.1 Features

- Synchronous mode with master or slave operation. Includes data phase selection and continuous clock option.
- Maximum bit rates of 6.25 Mbit/s in asynchronous mode.
- Maximum supported bit rate of 24 Mbit/s for USART master and slave synchronous modes.
- 7, 8, or 9 data bits and 1 or 2 stop bits.

- Burst conversion mode for single or multiple inputs.
- Synchronous or asynchronous operation. Asynchronous operation maximizes flexibility in choosing the ADC clock frequency, Synchronous mode minimizes trigger latency and can eliminate uncertainty and jitter in response to a trigger.

7.20 System control

7.20.1 Clock sources

The LPC5410x supports two external and three internal clock sources:

- The Internal RC (IRC).
- Watchdog oscillator (WDOSC).
- External clock source from the digital I/O pin CLKIN.
- External RTC 32 KHz clock.
- Output of the system PLL.

7.20.1.1 Internal RC oscillator (IRC)

The IRC can be used as the clock that drives the system PLL and subsequently the CPU. The nominal IRC frequency is 12 MHz.

Upon power-up or any chip reset, the LPC5410x uses the IRC as the clock source. Software may later switch to one of the other available clock sources.

7.20.1.2 Watchdog oscillator (WDOSC)

The watchdog oscillator is a low-power internal oscillator. The WDOSC can be used to provide a clock to the WWDT and to the entire chip. The nominal output frequency is 500 kHz.

7.20.1.3 Clock input pin (CLKIN)

An external square-wave clock source (up to 25 MHz) can be supplied on the digital I/O pin CLKIN.

7.20.2 System PLL

The system PLL accepts an input clock frequency in the range of 32 kHz to 12 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO).

The PLL can be enabled or disabled by software.

7.20.4.1 Sleep mode

When sleep mode is entered, the clock to the core is stopped along with any unused peripherals. Waking up from the sleep mode does not need any special sequence other than re-enabling the clock to the ARM core.

In sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, internal buses, and unused peripherals. The processor state and registers, peripheral registers, and internal SRAM values are maintained, and the logic levels of the pins remain static.

7.20.4.2 Deep sleep mode

In deep sleep mode, all peripheral clocks and all clock sources are off with the option of keeping the 32 kHz clock and the WDOSC running. In addition, all analog blocks are shut down and the flash is put in stand-by mode. In deep sleep mode, the application can keep some of the internal clocks and the BOD circuit running for self-timed wake-up and BOD protection.

The LPC5410x can wake up from deep sleep mode via a reset, digital pins selected as inputs to the pin interrupt block, RTC alarm, Micro-tick, a watchdog timer reset interrupt, BOD interrupt/reset, or an interrupt from the USART (in 32 kHz mode or synchronous slave mode), the SPI, or any of the I2C peripherals. For wake-up from deep sleep mode, the SPI, USART, and I2C peripherals must be configured in slave mode.

Any interrupt used for waking up from deep sleep mode must be enabled in one of the SYSCON wake-up enable registers and the NVIC.

In deep sleep mode, the processor state and registers, peripheral registers, and internal SRAM values are maintained, and the logic levels of the pins remain static. deep sleep mode allows for very low quiescent power and fast wake-up options.

7.20.4.3 Power down mode

In power down mode, all peripheral clocks and all clock sources are off with the option of keeping the 32 kHz clock, and the WDOSC running. In addition, all analog blocks and the flash are shut down. In power down mode, the application can keep the BOD circuit running for BOD protection.

The LPC5410x can wake up from power down mode via a reset, digital pins selected as inputs to the pin interrupt block, RTC alarm, Micro-tick, a watchdog timer reset interrupt, BOD interrupt/reset, or an interrupt from the USART (in 32 kHz mode or synchronous slave mode), the SPI, or any of the I2C peripherals. For wake-up from power down mode, the SPI, USART, and I2C peripherals must be configured in slave mode.

In power down mode, the processor state and registers, peripheral registers, and internal SRAM values are maintained, and the logic levels of the pins remain static. Power down mode reduces power consumption compared to deep sleep mode at the expense of longer wake-up times.

7.22 Emulation and debugging

Debug and trace functions are integrated into the ARM Cortex-M4 and ARM Cortex-M0+. Serial wire debug and trace functions are supported. The ARM Cortex-M4 is configured to support up to eight breakpoints and four watch points. The ARM Cortex-M0+ is configured to support up to four breakpoints and two watch points. In addition, JTAG boundary scan mode is provided.

The ARM SYSREQ reset is supported and causes the processor to reset the peripherals, execute the boot code, restart from address 0x0000 0000, and break at the user entry point.

The SWD pins are multiplexed with other digital I/O pins. On reset, the pins assume the SWD functions by default.

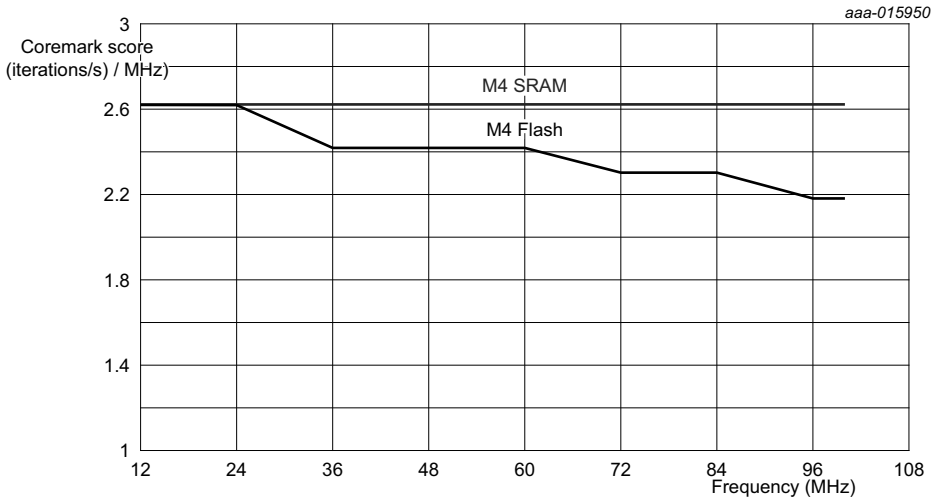
[8] An ADC input voltage above 3.6 V can be applied for a short time without leading to immediate, unrecoverable failure. Accumulated exposure to elevated voltages at 4.6 V must be less than 10^6 s total over the lifetime of the device. Applying an elevated voltage to the ADC inputs for a long time affects the reliability of the device and reduces its lifetime.

[9] It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

[10] Dependent on package type.

[5] SRAM0 and SRAM1 powered, SRAM2 powered down.

[6] See the FLASHCFG register in the LPC5410x User Manual for system clock flash access time settings.



Conditions: V_{DD} = 3.3 V; T_{amb} = 25 °C; active mode; all peripherals except one UART; BOD disabled; SRAM0 and SRAM1 powered, SRAM2 powered down. See the FLASHCFG register in the LPC5410x User Manual for system clock flash access time settings. Measured with Keil uVision 5.12. Optimization level 3, optimized for time on.

12 MHz: IRC enabled; PLL disabled. 24 MHz - 100 MHz: IRC enabled; PLL enabled.

Fig 8. Typical CoreMark score

10.3 Power consumption

Power measurements in Active, sleep, deep sleep, and power down modes were performed under the following conditions:

- Configure all pins as GPIO with pull-up resistor disabled in the IOCON block.
- Configure GPIO pins as outputs using the GPIO DIR register.
- Write 1 to the GPIO CLR register to drive the outputs LOW.
- All peripherals disabled.

Table 11. Static characteristics: Power consumption in active and sleep modes

T_{amb} = −40 °C to +105 °C, unless otherwise specified.1.62 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
ARM Cortex-M0+ in active mode; ARM Cortex-M4 in sleep mode							
I_{DD}	supply current	CoreMark code executed from SRAM; flash powered down CCLK = 12 MHz	[2][4][6]	-	1.2	-	mA
		CCLK = 48 MHz	[3][4][6]	-	3.0	-	mA
		CCLK = 84 MHz	[3][4][6]	-	4.5	-	mA
		CCLK = 100 MHz	[3][4][6]	-	5.5	-	mA
I_{DD}	supply current	CoreMark code executed from flash; CCLK = 12 MHz; 1 system clock flash access time.	[2][4][6]	-	1.5	-	mA
		CCLK = 48 MHz; 3 system clock flash access time.	[3][4][6]	-	3.6	-	mA
		CCLK = 84 MHz; 6 system clock flash access time.	[3][4][6]	-	5.4	-	mA
		CCLK = 100 MHz; 7 system clock flash access time.	[3][4][6]	-	6.6	-	mA
I_{DD}	supply current	Calculating Fibonacci numbers executed from flash; CCLK = 12 MHz	[2][4][5]	-	1.5	-	mA
		CCLK = 84 MHz	[3][4][5]	-	6.2	-	mA
		CCLK = 96 MHz	[3][4][5]	-	7.2	-	mA

Table 11. Static characteristics: Power consumption in active and sleep modes

T_{amb} = −40 °C to +105 °C, unless otherwise specified.1.62 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
ARM Cortex-M4 in active mode; ARM Cortex-M0+ in sleep mode							
I_{DD}	supply current	CoreMark code executed from SRAM; flash powered down					
		CCLK = 12 MHz	[2][4][6]	-	1.5	-	mA
		CCLK = 48 MHz	[3][4][6]	-	4.8	-	mA
		CCLK = 84 MHz	[3][4][6]	-	7.9	-	mA
		CCLK = 100 MHz	[3][4][6]	-	9.9	-	mA
I_{DD}	supply current	CoreMark code executed from flash;					
		CCLK = 12 MHz; 1 system clock flash access time.	[2][4][6]	-	1.9	-	mA
		CCLK = 48 MHz; 3 system clock flash access time.	[3][4][6]	-	5.7	-	mA
		CCLK = 84 MHz; 6 system clock flash access time.	[3][4][6]	-	8.8	-	mA
		CCLK = 100 MHz; 7 system clock flash access time.	[3][4][6]	-	10.7	-	mA
I_{DD}	supply current	Calculating Fibonacci numbers executed from SRAM;					
		CCLK = 12 MHz	[2][4][5]	-	1.7	-	mA
		CCLK = 84 MHz	[3][4][5]	-	8.0	-	mA
		CCLK = 96 MHz	[3][4][5]	-	9.4	-	mA
I_{DD}	supply current	Calculating Fibonacci numbers executed from flash;					
		CCLK = 12 MHz	[2][4][5]	-	1.7	-	mA
		CCLK = 84 MHz	[3][4][5]	-	8.0	-	mA
		CCLK = 96 MHz	[3][4][5]	-	9.4	-	mA

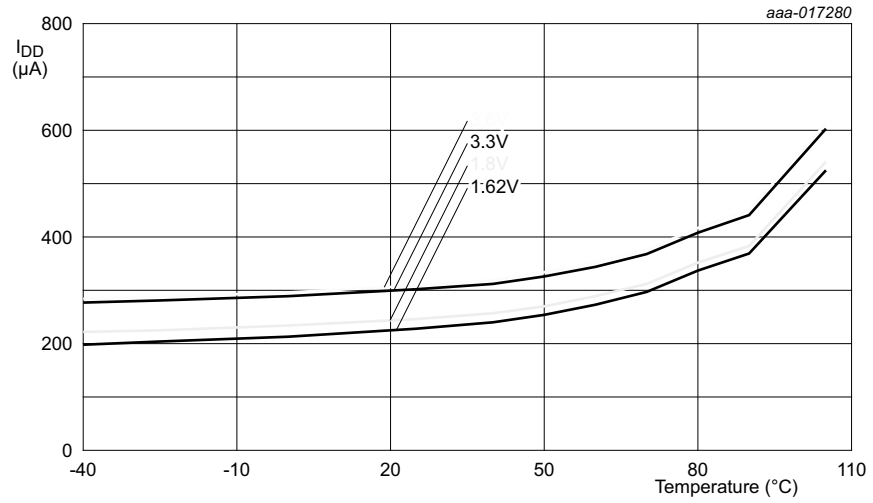
Table 12. Static characteristics: Power consumption in deep sleep, power down, and deep power-down modes
T_{amb} = −40 °C to +105 °C, 1.62 V ≤ V_{DD} ≤ 2.0 V; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1][2]	Max[3]	Unit
I_{DD}	supply current	Deep sleep mode; all SRAM on:	[2]				
		T_{amb} = 25 °C		-	235	380	µA
		T_{amb} = 105 °C		-	-	1.9	mA
		Power down mode;	[2]				
		first 8 kB in SRAM0 powered:					
		T_{amb} = 25 °C		-	4	8	µA
		T_{amb} = 105 °C			-	110	µA
		SRAM0 (64 kB) powered		-	6.7	-	µA
		SRAM0 (64 kB), SRAM1 (32 kB) powered		-	7.8	-	µA
		SRAM0 (64 kB), SRAM1 (32 kB), SRAM2 (8 kB) powered		-	8.2	-	µA
		Deep power-down mode;	[2]	-			
		RTC oscillator input grounded (RTC oscillator disabled)					
		T_{amb} = 25 °C			160	340	nA
		T_{amb} = 105 °C			-	14	µA
		RTC oscillator running with external crystal		-	240	-	nA

[1] Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C).

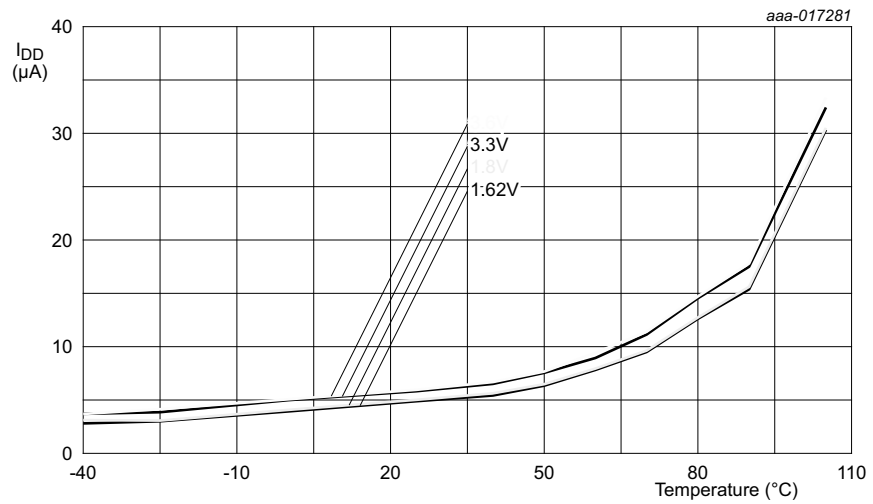
[2] Characterized through bench measurements using typical samples. V_{DD} = 1.62 V

[3] Guaranteed by characterization, not tested in production. V_{DD} = 2.0 V



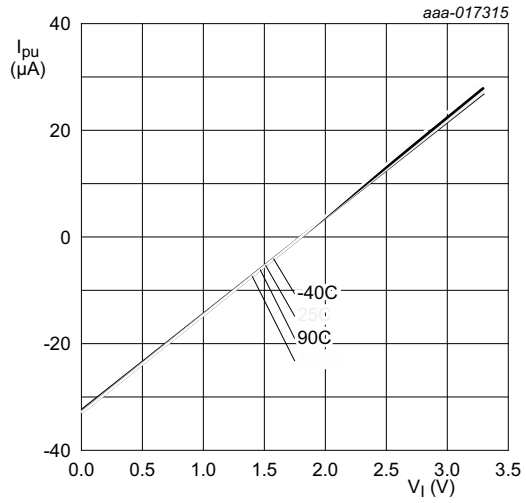
Conditions: BOD disabled; All SRAM blocks enabled.

Fig 10. Deep sleep mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}

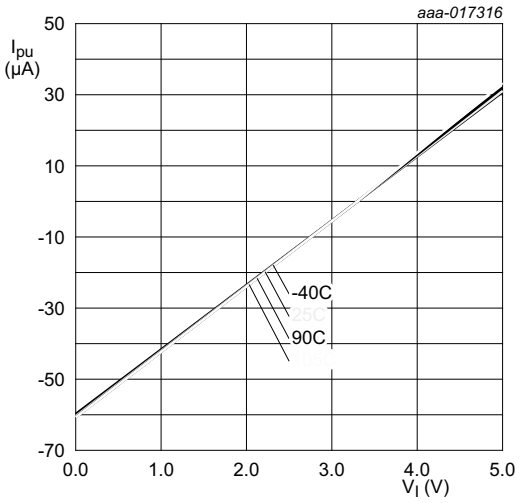


Conditions: BOD disabled; all SRAM disabled except first 8 kB in SRAM0.

Fig 11. Power down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}

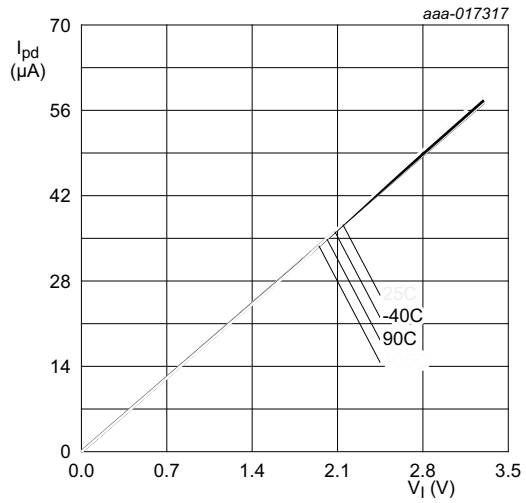


Conditions: V_{DD} = 1.8 V; on standard port pins.

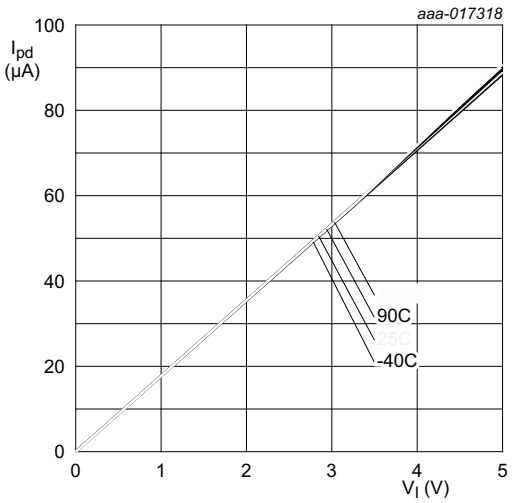


Conditions: V_{DD} = 3.3 V; on standard port pins.

Fig 17. Typical pull-up current I_{PU} versus input voltage V_I



Conditions: V_{DD} = 1.8V; on standard port pins.



Conditions: V_{DD} = 3.3 V; on standard port pins.

Fig 18. Typical pull-down current I_{PD} versus input voltage V_I

Table 27. SPI dynamic characteristics[1]

T_{amb} = −40 °C to 105 °C; C_L = 30 pF balanced loading on all pins; SLEW = standard mode. Parameters sampled at the 50 % level of the rising or falling edge.

Symbol	Parameter	Conditions		Min	Max	Unit
t_{DH}	data hold time	CCLK = 1 MHz to 12 MHz		0	-	ns
		CCLK = 48 MHz to 60 MHz		0	-	ns
		CCLK = 96 MHz		0	-	ns
$t_{v(Q)}$	data output valid time	CCLK = 1 MHz to 12 MHz		36	61	ns
		CCLK = 48 MHz to 60 MHz		21	22	ns
		CCLK = 96 MHz		20	21	ns

[1] *Based on characterization; not tested in production.*

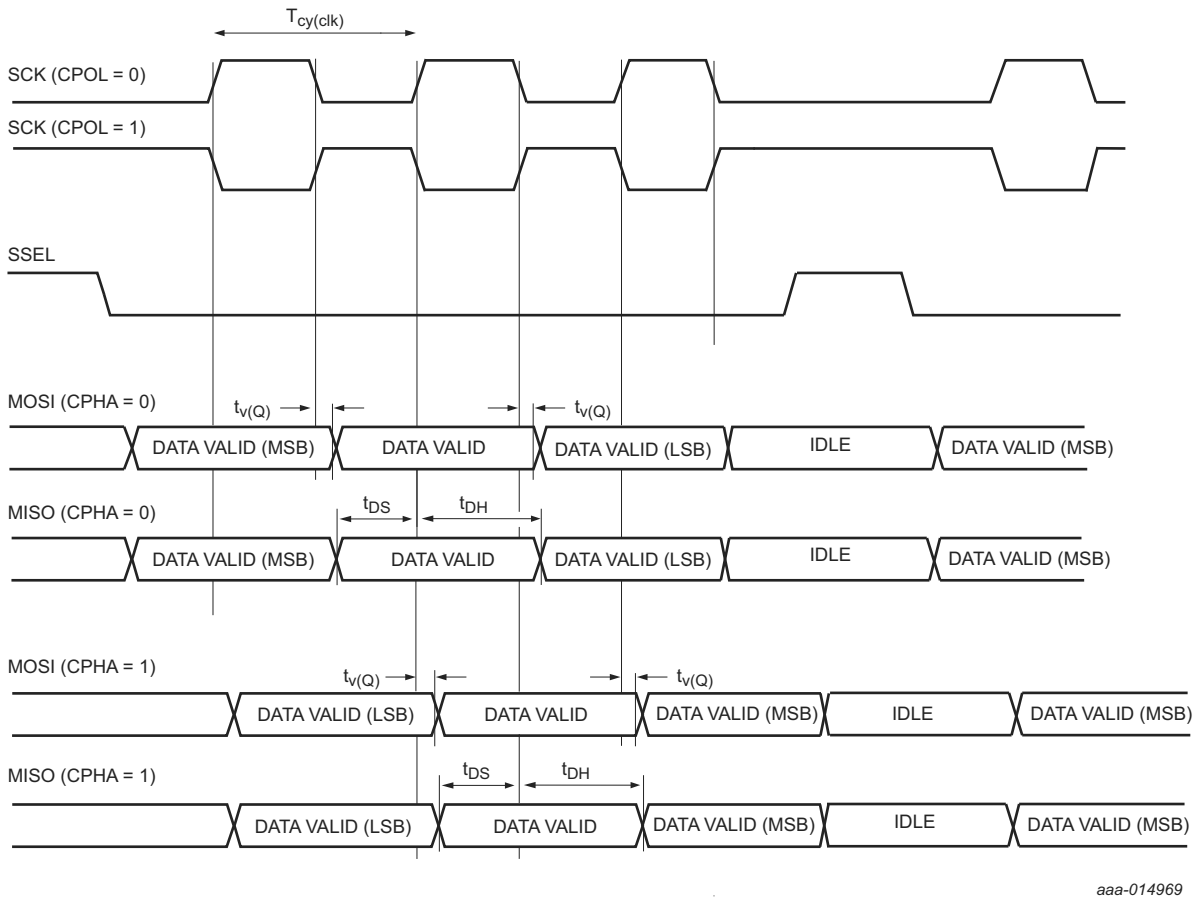


Fig 21. SPI master timing

11.11 USART interface

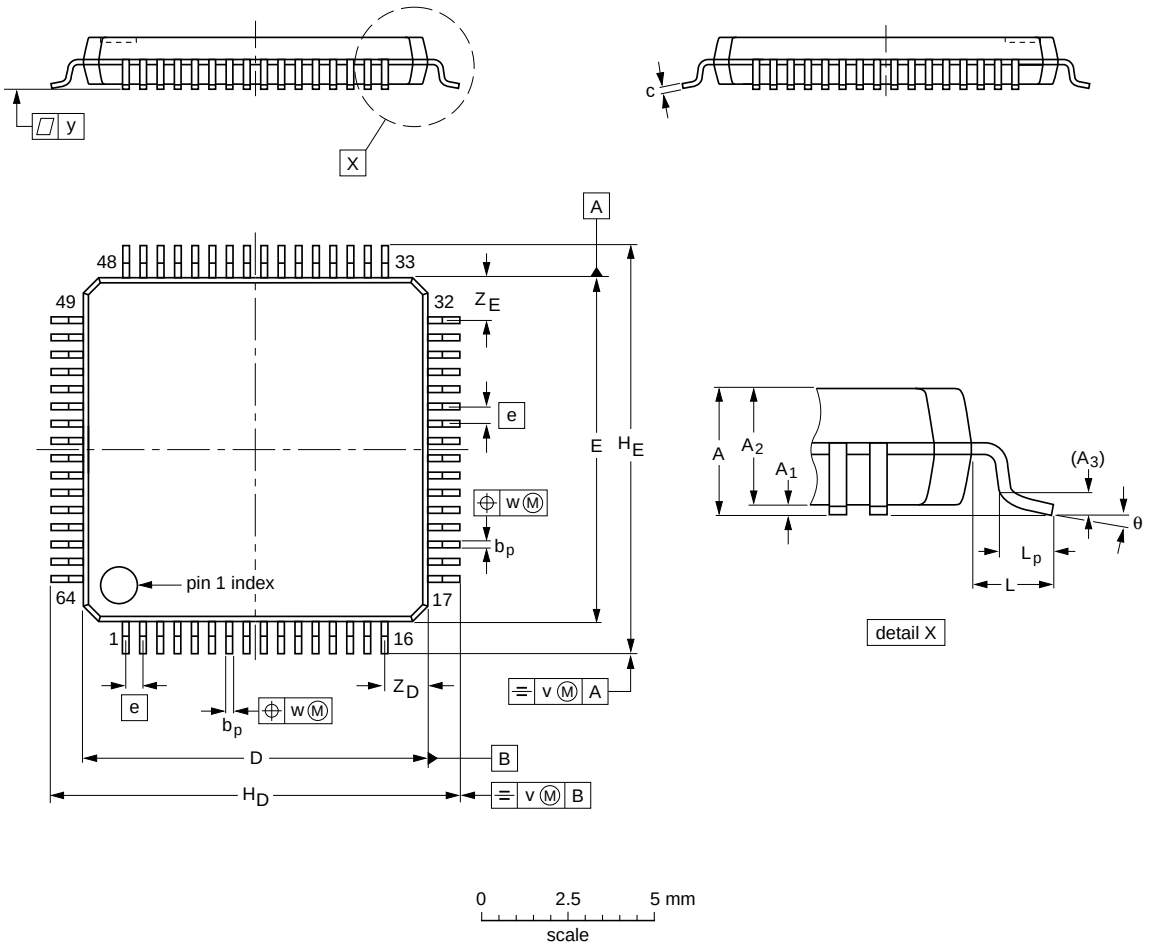
The actual USART bit rate depends on the delays introduced by the external trace, the external device, system clock (CCLK), and capacitive loading. Excluding delays introduced by external device and PCB, the maximum supported bit rate for USART master and slave synchronous modes is 24 Mbit/s.

Table 28. USART dynamic characteristics[1]

T_{amb} = −40 °C to 105 °C; 1.62 V ≤ V_{DD} ≤ 3.6 V; C_L = 30 pF balanced loading on all pins; SLEW = standard mode. Parameters sampled at the 50% level of the falling or rising edge.

Symbol	Parameter	Conditions	Min	Max	Unit
USART master (in synchronous mode) 1.62V ≤ VDD ≤ 2.0 V					
$t_{su(D)}$	data input set-up time	CCLK = 1 MHz to 12 MHz	65	-	ns
		CCLK = 48 MHz to 60 MHz	35	-	ns
		CCLK = 96 MHz	34	-	ns
$t_{h(D)}$	data input hold time	CCLK = 1 MHz to 12 MHz	0	-	ns
		CCLK = 48 MHz to 60 MHz	0	-	ns
		CCLK = 96 MHz	0	-	ns
$t_{v(Q)}$	data output valid time	CCLK = 1 MHz to 12 MHz	0	8	ns
		CCLK = 48 MHz to 60 MHz	0	2	ns
		CCLK = 96 MHz	0	2	ns
USART slave (in synchronous mode) 1.62V ≤ VDD ≤ 2.0 V					
$t_{su(D)}$	data input set-up time	CCLK = 1 MHz to 12 MHz	18	-	ns
		CCLK = 48 MHz to 60 MHz	5	-	ns
		CCLK = 96 MHz	4	-	ns
$t_{h(D)}$	data input hold time	CCLK = 1 MHz to 12 MHz	0	-	ns
		CCLK = 48 MHz to 60 MHz	0	-	ns
		CCLK = 96 MHz	0	-	ns
$t_{v(Q)}$	data output valid time	CCLK = 1 MHz to 12 MHz	50	65	ns
		CCLK = 48 MHz to 60 MHz	35	40	ns
		CCLK = 96 MHz	30	36	ns
USART master (in synchronous mode) 2.7V ≤ VDD ≤ 3.6V					
$t_{su(D)}$	data input set-up time	CCLK = 1 MHz to 12 MHz	61	-	ns
		CCLK = 48 MHz to 60 MHz	22	-	ns
		CCLK = 96 MHz	21	-	ns
$t_{h(D)}$	data input hold time	CCLK = 1 MHz to 12 MHz	0	-	ns
		CCLK = 48 MHz to 60 MHz	0	-	ns
		CCLK = 96 MHz	0	-	ns
$t_{v(Q)}$	data output valid time	CCLK = 1 MHz to 12 MHz	0	7	ns
		CCLK = 48 MHz to 60 MHz	1	2	ns
		CCLK = 96 MHz	1	2	ns

LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm **SOT314-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1	0.75 0.45	0.2	0.12	0.1	1.45 1.05	1.45 1.05	7^o 0^o

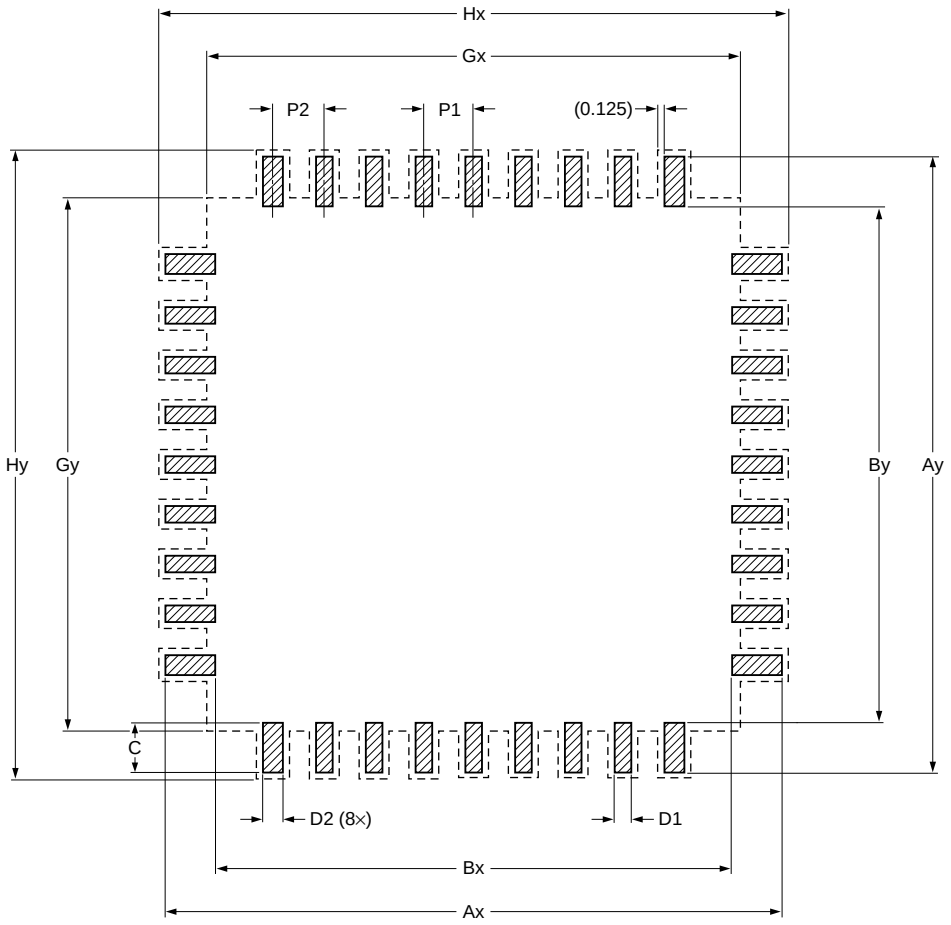
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT314-2	136E10	MS-026				~~00-01-19~~ 03-02-25

Fig 31. LQFP64 Package outline

Footprint information for reflow soldering of LQFP64 package **SOT314-2**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	13.300	13.300	10.300	10.300	1.500	0.280	0.400	10.500	10.500	13.550	13.550

sot314-2_fr

Fig 33. LQFP64 Soldering footprint

16. Abbreviations

Table 35. Abbreviations

Acronym	Description
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
API	Application Programming Interface
DMA	Direct Memory Access
GPIO	General Purpose Input/Output
IRC	Internal RC
LSB	Least Significant Bit
MCU	MicroController Unit
PLL	Phase-Locked Loop
SPI	Serial Peripheral Interface
TTL	Transistor-Transistor Logic
USART	Universal Asynchronous Receiver/Transmitter

17. References

[1] LPC5410x User manual UM10850:
http://www.nxp.com/documents/user_manual/UM10850.pdf

[2] LPC5410x Errata sheet:
http://www.nxp.com/documents/errata_sheet/ES_LPC5410X.pdf

[3] Technical note ADC design guidelines:
http://www.nxp.com/documents/technical_note/TN00009.pdf