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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	50
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	104K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc54101j512bd64ql

Table 4. Pin description *…continued*

Symbol	WLCSP49	LQFP64		Reset state [1]	Type [6]	Description
PIO0_18/TRST	G4	58	[2]	PU	I/O	**PIO0_18 —** General-purpose digital input/output pin. In boundary scan mode: TRST (Test Reset).
					O	**U3_TXD —** Transmitter output for USART3.
					O	**SCT0_OUT0 —** SCT0 output 0. PWM output 0.
					O	**CT32B0_MAT0 —** 32-bit CT32B0 match output 0.
					I	**R —** Reserved.
PIO0_19/TDI	G3	59	[2]	PU	I/O	**PIO0_19 —** General-purpose digital input/output pin. In boundary scan mode: TDI (Test Data In).
					I/O	**U3_SCLK —** USART3 clock in synchronous USART mode.
					O	**SCT0_OUT1 —** SCT0 output 1. PWM output 1.
					O	**CT32B0_MAT1 —** 32-bit CT32B0 match output 1.
					I	**R —** Reserved.
PIO0_20/TMS	F3	60	[2]	PU	I/O	**PIO0_20 —** General-purpose digital input/output pin. In boundary scan mode: TMS (Test Mode Select).
					I	**U3_RXD —** Receiver input for USART3.
					I/O	**U0_SCLK —** USART0 clock in synchronous USART mode.
					I	**CT32B3_CAP0 —** 32-bit CT32B3 capture input 0.
					I	**R —** Reserved.
PIO0_21	E3	61	[2]	PU	I/O	**PIO0_21 —** General-purpose digital input/output pin.
					O	**CLKOUT —** Clock output pin.
					O	**U0_TXD —** Transmitter output for USART0.
					O	**CT32B3_MAT0 —** 32-bit CT32B3 match output 0.
					I	**R —** Reserved.
PIO0_22	G2	63	[2]	PU	I/O	**PIO0_22 —** General-purpose digital input/output pin.
					I	**CLKIN —** Clock input.
					I	**U0_RXD —** Receiver input for USART0.
					O	**CT32B3_MAT3 —** 32-bit CT32B3 match output 3.
					I	**R —** Reserved.
PIO0_23	F2	1	[3]	Z	I/O	**PIO0_23 —** General-purpose digital input/output pin.
					I/O	**I2C0_SCL —** I^2C0 clock input/output.
					I	**R —** Reserved.
					I	**CT32B0_CAP0 —** 32-bit CT32B0 capture input 0.
					I	**R —** Reserved.

6.2.1 Termination of unused pins

Table 5 shows how to terminate pins that are **not** used in the application. In many cases, unused pins should be connected externally or configured correctly by software to minimize the overall power consumption of the part.

Unused pins with GPIO function should be configured as outputs set to LOW with their internal pull-up disabled. To configure a GPIO pin as output and drive it LOW, select the GPIO function in the IOCON register, select output in the GPIO DIR register, and write a 0 to the GPIO PORT register for that pin. Disable the pull-up in the pin's IOCON register.

In addition, it is recommended to configure all GPIO pins that are not bonded out on smaller packages as outputs driven LOW with their internal pull-up disabled.

Table 5. Termination of unused pins

Pin	Default state[1]	Recommended termination of unused pins
$\overline{\text{RESET}}$	I; PU	The $\overline{\text{RESET}}$ pin can be left unconnected if the application does not use it.
all PIOn_m (not open-drain)	I; PU	Can be left unconnected if driven LOW and configured as GPIO output with pull-up disabled by software.
PIOn_m (I2C open-drain)	IA	Can be left unconnected if driven LOW and configured as GPIO output by software.
RTCXIN	-	Connect to ground. When grounded, the RTC oscillator is disabled.
RTCXOUT	-	Can be left unconnected.
VREFP	-	Tie to VDD.
VREFN	-	Tie to VSS.
VDDA	-	Tie to VDD.
VSSA	-	Tie to VSS.

[1] I = Input, IA = Inactive (no pull-up/pull-down enabled), PU = Pull-Up.

6.2.2 Pin states in different power modes

Table 6. Pin states in different power modes

Pin	Active	Sleep	Deep sleep/Power down	Deep power-down
PIOn_m pins (not I2C)	As configured in the IOCON[1]. Default: internal pull-up enabled.			Floating.
PIO0_23 to PIO0_28 (open-drain I2C-bus pins)	As configured in the IOCON[1].			Floating.
$\overline{\text{RESET}}$	Reset function enabled. Default: input, internal pull-up enabled. Reset function disabled.			

[1] Default and programmed pin states are retained in sleep, deep sleep, and power down modes.

7. Functional description

7.1 Architectural overview

The ARM Cortex-M4 includes three AHB-Lite buses, one system bus and the I-code and D-code buses. One bus is dedicated for instruction fetch (I-code), and one bus is dedicated for data access (D-code). The use of two core buses allows for simultaneous operations if concurrent operations target different devices.

A multi-layer AHB matrix connects the CPU buses and other bus masters to peripherals in a flexible manner that optimizes performance by allowing peripherals on different slaves ports of the matrix to be accessed simultaneously by different bus masters. Connections in the multilayer matrix are shown in Figure 3.

APB peripherals are connected to the AHB matrix via two APB buses using separate slave ports from the multilayer AHB matrix. This allows for better performance by reducing collisions between the CPU and the DMA controller, and also for peripherals on the asynchronous bridge to have a fixed clock that does not track the system clock.

7.2 ARM Cortex-M4 processor

The ARM Cortex-M4 is a general purpose, 32-bit microprocessor, which offers high performance and very low power consumption. The ARM Cortex-M4 offers many new features, including a Thumb-2 instruction set, low interrupt latency, hardware multiply and divide, interruptable/continuable multiple load and store instructions, automatic state save and restore for interrupts, tightly integrated interrupt controller with wake-up interrupt controller, and multiple core buses capable of simultaneous accesses.

A 3-stage pipeline is employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

7.3 ARM Cortex-M4 integrated Floating Point Unit (FPU)

The FPU fully supports single-precision add, subtract, multiply, divide, multiply and accumulate, and square root operations. It also provides conversions between fixed-point and floating-point data formats, and floating-point constant instructions.

The FPU provides floating-point computation functionality that is compliant with the ANSI/IEEE Std 754-2008, IEEE Standard for Binary Floating-Point Arithmetic, referred to as the IEEE 754 standard.

7.4 Memory Protection Unit (MPU)

The Cortex-M4 includes a Memory Protection Unit (MPU) which can be used to improve the reliability of an embedded system by protecting critical data within the user application.

The MPU allows separating processing tasks by disallowing access to each other's data, disabling access to memory regions, allowing memory regions to be defined as read-only and detecting unexpected memory accesses that could potentially break the system.

7.7.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags.

7.8 System Tick timer (SysTick)

The ARM Cortex-M4 and ARM Cortex-M0+ cores include a system tick timer (SysTick) that is intended to generate a dedicated SYSTICK exception. The clock source for the SysTick can be the system clock or the SYSTICK clock.

7.9 On-chip static RAM

The LPC5410x support 104 kB SRAM with separate bus master access for higher throughput and individual power control for low-power operation.

7.10 On-chip flash

The LPC5410x supports 512 kB of on-chip flash memory.

7.11 On-chip ROM

The 64 kB on-chip ROM contains the boot loader and the following Application Programming Interfaces (API):

- In-System Programming (ISP) and In-Application Programming (IAP) support for flash programming.
- Power control API for configuring power consumption and PLL settings.

7.13 General Purpose I/O (GPIO)

The LPC5410x provides two GPIO ports with a total of 50 GPIO pins.

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The current level of a port pin can be read back no matter what peripheral is selected for that pin.

See Table 4 for the default state on reset.

7.13.1 Features

- Accelerated GPIO functions:
  - GPIO registers are located on the AHB so that the fastest possible I/O timing can be achieved.
  - Mask registers allow treating sets of port bits as a group, leaving other bits unchanged.
  - All GPIO registers are byte and half-word addressable.
  - Entire port value can be written in one instruction.
- Bit-level set, clear and toggle registers allow a single instruction set, clear or toggle of any number of bits in one port.
- Direction control of individual bits.
- All I/O default to inputs after reset.
- All GPIO pins can be selected to create an edge or level-sensitive GPIO interrupt request.
- One GPIO group interrupt can be triggered by a combination of any pin or pins.

7.14 Pin interrupt/pattern engine

The pin interrupt block configures up to eight pins from all digital pins for providing eight external interrupts connected to the NVIC. The pattern match engine can be used in conjunction with software to create complex state machines based on pin inputs. Any digital pin, independent of the function selected through the switch matrix can be configured through the SYSCON block as an input to the pin interrupt or pattern match engine. The registers that control the pin interrupt or pattern match engine are located on the I/O+ bus for fast single-cycle access.

7.14.1 Features

- Pin interrupts:
  - Up to eight pins can be selected from all GPIO pins on ports 0 and 1 as edge-sensitive or level-sensitive interrupt requests. Each request creates a separate interrupt in the NVIC.
  - Edge-sensitive interrupt pins can interrupt on rising or falling edges or both.
  - Level-sensitive interrupt pins can be HIGH-active or LOW-active.
  - Level-sensitive interrupt pins can be HIGH-active or LOW-active.
  - Pin interrupts can wake up the device from sleep mode, deep sleep mode, and power down mode.

- FIFO support from the System FIFO.
- Activity on the SPI in slave mode allows wake-up from deep sleep and power down modes on any enabled interrupt.

7.17 I²C-bus interface

The I²C-bus is bidirectional for inter-IC control using only two wires: a serial clock line (SCL) and a serial data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (for example, an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I²C is a multi-master bus and can be controlled by more than one bus master connected to it.

7.17.1 Features

- All I²Cs support standard (up to 100 Kbits/s), fast mode (up to 400 Kbits/s), and Fast-mode Plus (up to 1 Mbit/s).
- All I²Cs support high-speed slave mode with data rates of up to 3.4 Mbit/s.
- Independent Master, Slave, and Monitor functions.
- Supports both Multi-master and Multi-master with Slave functions.
- Multiple I²C slave addresses supported in hardware.
- One slave address can be selectively qualified with a bit mask or an address range in order to respond to multiple I²C-bus addresses.
- 10-bit addressing supported with software assist.
- Supports System Management Bus (SMBus).
- No chip clocks are required in order to receive and compare an address as a Slave, so this event can wake up the device from power down mode.
- Supports the I²C-bus specification up to Fast-mode Plus (FM+, up to 1 MHz) in both master and slave modes. High-speed (HS, up to 3.4 MHz) I²C is support in slave mode only.
- Activity on the I²C in slave mode allows wake-up from deep sleep and power down modes on any enabled interrupt.

7.18 Counter/timers

7.18.1 General-purpose 32-bit timers/external event counter

The LPC5410x includes five general-purpose 32-bit timer/counters.

The timer/counter is designed to count cycles of the system derived clock or an externally-supplied clock. It can optionally generate interrupts, generate timed DMA requests, or perform other actions at specified timer values, based on four match registers. Each timer/counter also includes two capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

7.18.1.1 Features

- Each is a 32-bit counter/timer with a programmable 32-bit prescaler. Four of the timers include external capture and match pin connections.

7.20.4.1 Sleep mode

When sleep mode is entered, the clock to the core is stopped along with any unused peripherals. Waking up from the sleep mode does not need any special sequence other than re-enabling the clock to the ARM core.

In sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, internal buses, and unused peripherals. The processor state and registers, peripheral registers, and internal SRAM values are maintained, and the logic levels of the pins remain static.

7.20.4.2 Deep sleep mode

In deep sleep mode, all peripheral clocks and all clock sources are off with the option of keeping the 32 kHz clock and the WDOSC running. In addition, all analog blocks are shut down and the flash is put in stand-by mode. In deep sleep mode, the application can keep some of the internal clocks and the BOD circuit running for self-timed wake-up and BOD protection.

The LPC5410x can wake up from deep sleep mode via a reset, digital pins selected as inputs to the pin interrupt block, RTC alarm, Micro-tick, a watchdog timer reset interrupt, BOD interrupt/reset, or an interrupt from the USART (in 32 kHz mode or synchronous slave mode), the SPI, or any of the I2C peripherals. For wake-up from deep sleep mode, the SPI, USART, and I2C peripherals must be configured in slave mode.

Any interrupt used for waking up from deep sleep mode must be enabled in one of the SYSCON wake-up enable registers and the NVIC.

In deep sleep mode, the processor state and registers, peripheral registers, and internal SRAM values are maintained, and the logic levels of the pins remain static. deep sleep mode allows for very low quiescent power and fast wake-up options.

7.20.4.3 Power down mode

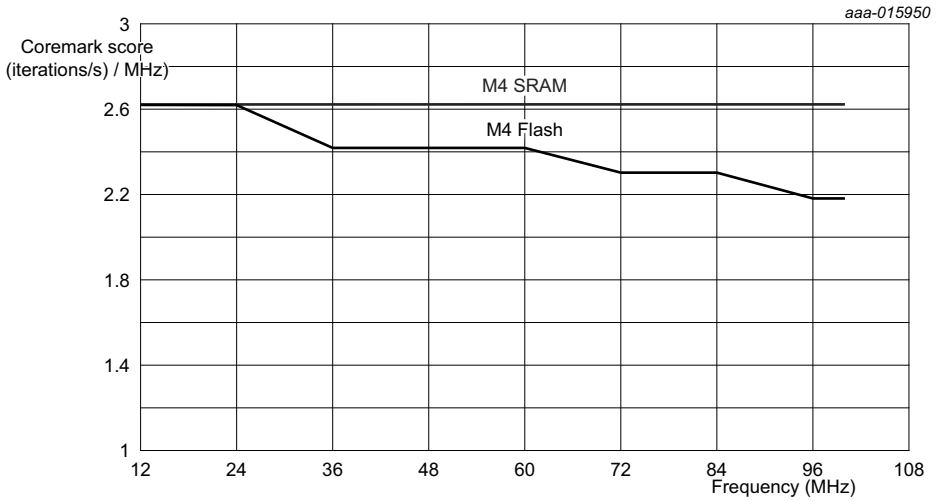
In power down mode, all peripheral clocks and all clock sources are off with the option of keeping the 32 kHz clock, and the WDOSC running. In addition, all analog blocks and the flash are shut down. In power down mode, the application can keep the BOD circuit running for BOD protection.

The LPC5410x can wake up from power down mode via a reset, digital pins selected as inputs to the pin interrupt block, RTC alarm, Micro-tick, a watchdog timer reset interrupt, BOD interrupt/reset, or an interrupt from the USART (in 32 kHz mode or synchronous slave mode), the SPI, or any of the I2C peripherals. For wake-up from power down mode, the SPI, USART, and I2C peripherals must be configured in slave mode.

In power down mode, the processor state and registers, peripheral registers, and internal SRAM values are maintained, and the logic levels of the pins remain static. Power down mode reduces power consumption compared to deep sleep mode at the expense of longer wake-up times.

[5] SRAM0 and SRAM1 powered, SRAM2 powered down.

[6] See the FLASHCFG register in the LPC5410x User Manual for system clock flash access time settings.



Conditions: V_{DD} = 3.3 V; T_{amb} = 25 °C; active mode; all peripherals except one UART; BOD disabled; SRAM0 and SRAM1 powered, SRAM2 powered down. See the FLASHCFG register in the LPC5410x User Manual for system clock flash access time settings. Measured with Keil uVision 5.12. Optimization level 3, optimized for time on.

12 MHz: IRC enabled; PLL disabled. 24 MHz - 100 MHz: IRC enabled; PLL enabled.

Fig 8. Typical CoreMark score

Table 11. Static characteristics: Power consumption in active and sleep modes

T_{amb} = −40 °C to +105 °C, unless otherwise specified.1.62 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
ARM Cortex-M4 in sleep mode; ARM Cortex-M0+ in sleep mode							
I_{DD}	supply current	CCLK = 12 MHz	[2][4][7]	-	990	-	μA
		CCLK = 100 MHz	[3][4][7]	-	4.0	-	mA

[1] Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C), 3.3V.

[2] Clock source 12 MHz IRC. PLL disabled.

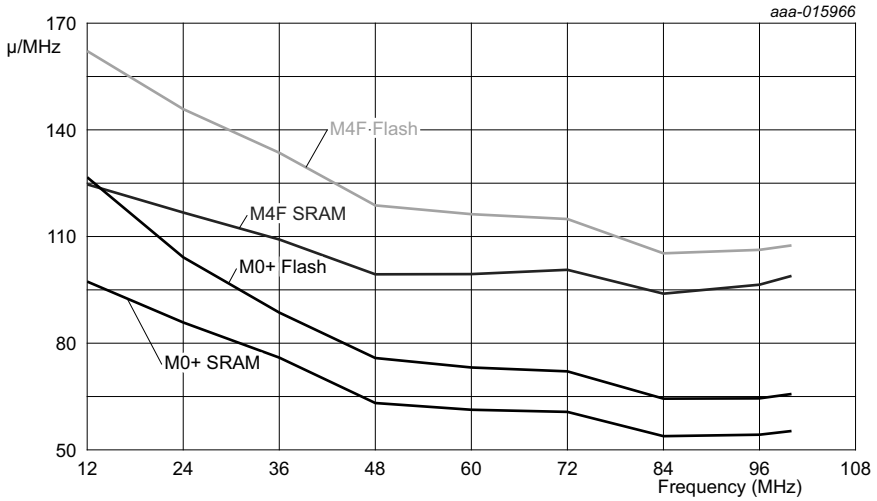
[3] Clock source 12 MHz IRC. PLL enabled.

[4] Characterized through bench measurements using typical samples.

[5] Compiler settings: Keil µVision v.5.10, optimization level 0, optimized for time off.

[6] Prefetch disabled in FLASHCFG register. System clock flash access time set by power API. SRAM0 powered, SRAM1 and SRAM2 powered down.Compiler settings: Keil µVision v.5.12, optimization level 0, optimized for time off.

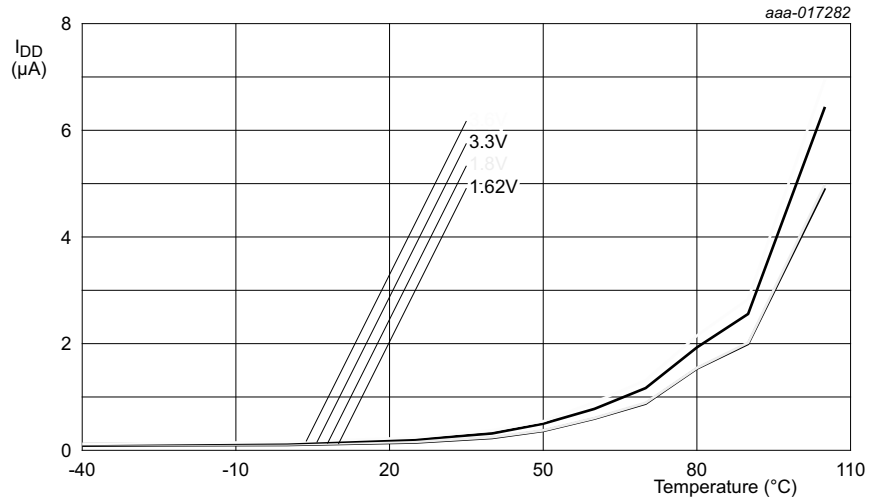
[7] First 8 kB in SRAM0 powered; Flash, SRAM1, and SRAM2 are powered down; all peripheral clocks disabled. Compiler settings: Keil µVision v.5.12, optimization level 0, optimized for time off.



Conditions: V_{DD} = 3.3 V; T_{amb} = 25 °C; active mode; all peripherals disabled; BOD disabled; Prefetch disabled in FLASHCFG register. System clock flash access time set by power API. SRAM0 powered, SRAM1 and SRAM2 powered down. Measured with Keil uVision 5.12. Optimization level 0, optimized for time off.

12 MHz: IRC enabled; PLL disabled. 24 MHz - 100 MHz: IRC enabled; PLL enabled.

Fig 9. CoreMark power consumption: typical µA/MHz for M4 and M0+ cores



RTC disabled (RTC oscillator input grounded)

Fig 12. Deep power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}

Table 14. Typical peripheral power consumption[1][2][3]

V_{DD} = 3.3 V; T_{amb} = 25 °C

Peripheral	I_{DD} in uA
IRC	262
WDT OSC	2.0
Flash	200.0
BOD	2.0
CLKOUT	37

[1] The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled using PDRUNCFG register. All other blocks are disabled and no code accessing the peripheral is executed.

[2] The supply currents are shown for system clock frequencies of 12 MHz.

[3] Typical ratings are not guaranteed. Characterized through bench measurements using typical samples.

Table 15. Typical AHB/APB peripheral power consumption[3][4][5]

V_{DD} = 3.3 V; T = 25 °C

Peripheral		I_{DD} in µA	I_{DD} in µA/MHz	I_{DD} in µA/MHz
AHB peripheral			**CPU: 12 MHz, sync APB bus: 12 MHz**	**CPU: 96MHz, sync APB bus: 96 MHz**
GPIO0	[1]	-	0.50	0.7
GPIO1	[1]	-	0.42	0.52
DMA		-	5.0	6.86
CRC		-	0.42	0.50
MAILBOX		-	0.17	0.20
ADC0		-	2.25	2.92
SCTimer/PWM		-	5.08	7.07

Table 15. Typical AHB/APB peripheral power consumption[3][4][5]

V_{DD} = 3.3 V; T = 25 °C

Peripheral		I_{DD} in μA	I_{DD} in μA/MHz	I_{DD} in μA/MHz
FIFO		-	3.17	4.49
Sync APB peripheral			**CPU: 12 MHz, sync APB bus: 12 MHz**	**CPU: 96MHz, sync APB bus: 96 MHz**
INPUTMUX	[1]	-	0.83	0.96
IOCON	[1]	-	1.25	1.55
PINT		-	0.83	1.05
GINT		-	0.50	0.61
WWDT		-	0.17	0.28
MRT		-	0.50	0.65
RTC		-	0.08	0.09
RIT		-	0.50	0.71
UTICK		-	0.17	0.11
Timer2		-	0.58	0.67
Timer3		-	0.42	0.42
Timer4		-	0.50	0.57
Async APB peripheral			**CPU: 12 MHz, Async APB bus: 12 MHz**	**CPU: 96MHz, Async APB bus: 12 MHz[2]**
USART0		-	0.67	0.11
USART1		-	0.75	0.07
USART2		-	0.67	0.11
USART3		-	0.75	0.07
I2C0		-	0.92	0.10
I2C1		-	0.83	0.26
I2C2		-	0.83	0.25
SPIO0		-	0.92	0.21
SPIO1		-	0.83	0.25
CTimer0		-	0.58	0.18
CTimer1		-	0.42	0.14
Fractional Rate Generator		-	4.17	0.73

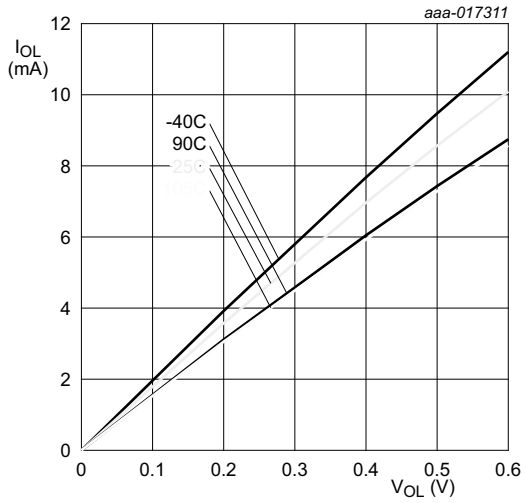
[1] Turn off the peripheral when the configuration is done.

[2] For optimal system power consumption, use fixed low frequency Async APB bus when the CPU is at a higher frequency.

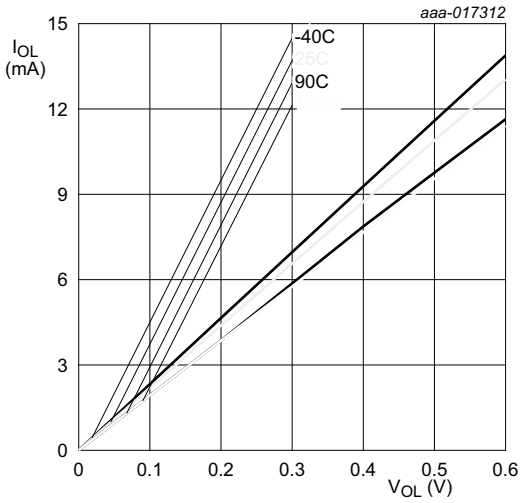
[3] The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled using ASYNCAPBCLKCTRL, AHBCLKCTRL0/1, and PDRUNCFG register. All other blocks are disabled and no code accessing the peripheral is executed.

[4] The supply currents are shown for system clock frequencies of 12 MHz and 96 MHz.

[5] Typical ratings are not guaranteed. Characterized through bench measurements using typical samples.

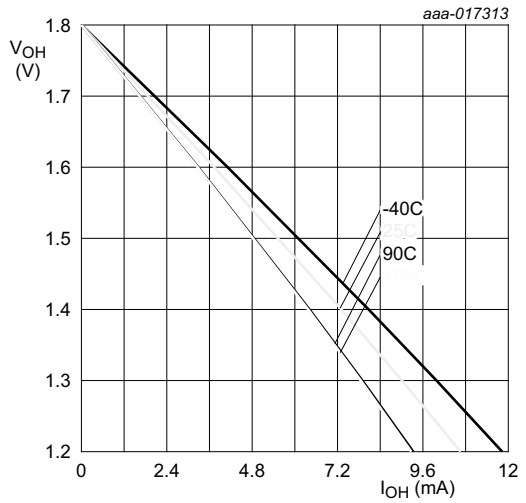


Conditions: V_{DD} = 1.8 V; on standard port pins.

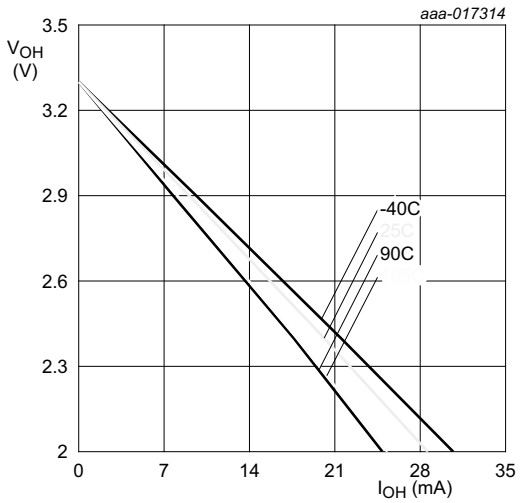


Conditions: V_{DD} = 3.3 V; on standard port pins.

Fig 15. Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}

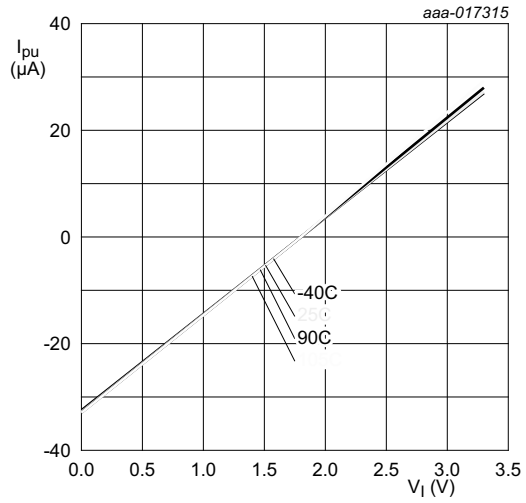


Conditions: V_{DD} = 1.8 V; on standard port pins.

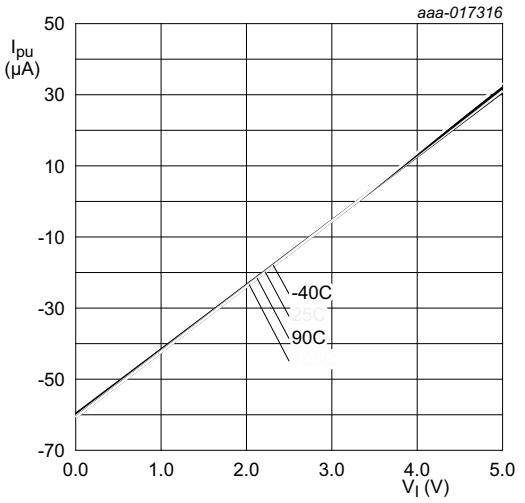


Conditions: V_{DD} = 3.3 V; on standard port pins.

Fig 16. Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}

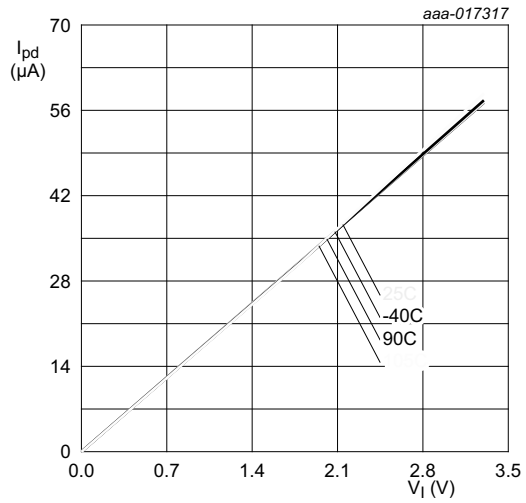


Conditions: V_{DD} = 1.8 V; on standard port pins.

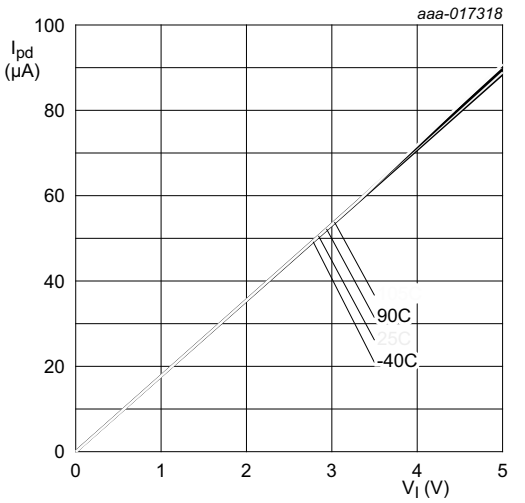


Conditions: V_{DD} = 3.3 V; on standard port pins.

Fig 17. Typical pull-up current I_{PU} versus input voltage V_I



Conditions: V_{DD} = 1.8V; on standard port pins.



Conditions: V_{DD} = 3.3 V; on standard port pins.

Fig 18. Typical pull-down current I_{PD} versus input voltage V_I

[1] Number of erase/program cycles.

[2] Programming times are given for writing 256 bytes from RAM to the flash.

11.3 I/O pins

Table 19. Dynamic characteristic: I/O pins[1]
T_{amb} = −40 °C to +85 °C; 1.62 V ≤ V_{DD} ≤ 3.6 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Standard I/O pins - normal drive strength							
t_r	rise time	pin configured as output; SLEW = 1 (fast mode);	[2][3]				
		2.7 V ≤ V_{DD} ≤ 3.6 V		1.0	-	2.5	ns
		1.62 V ≤ V_{DD} ≤ 1.98 V		1.6	-	3.8	ns
t_f	fall time	pin configured as output; SLEW = 1 (fast mode);	[2][3]				
		2.7 V ≤ V_{DD} ≤ 3.6 V		0.9	-	2.5	ns
		1.62 V ≤V_{DD} ≤ 1.98 V		1.7	-	4.1	ns
t_r	rise time	pin configured as output; SLEW = 0 (standard mode);	[2][3]				
		2.7 V ≤ V_{DD} ≤ 3.6 V		1.9	-	4.3	ns
		1.62 V ≤ V_{DD} ≤ 1.98 V		2.9	-	7.8	ns
t_f	fall time	pin configured as output; SLEW = 0 (standard mode);	[2][3]				
		2.7 V ≤ V_{DD} ≤ 3.6 V		1.9	-	4.0	ns
		1.62 V ≤ V_{DD} ≤ 1.98 V		2.7	-	6.7	ns
t_r	rise time	pin configured as input	[4]	0.3	-	1.3	ns
t_f	fall time	pin configured as input	[4]	0.2	-	1.2	ns

[1] Simulated data.

[2] Simulated using 10 cm of 50 Ω PCB trace with 5 pF receiver input. Rise and fall times measured between 80 % and 20 % of the full output signal level.

[3] The slew rate is configured in the IOCON block the SLEW bit. See the LPC5410x user manual.

[4] C_L = 20 pF. Rise and fall times measured between 90 % and 10 % of the full input signal level.

11.4 Wake-up process

Table 20. Dynamic characteristic: Typical wake-up times from low power modes
V_{DD} = 3.3 V;T_{amb} = 25 °C; using IRC as the system clock.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
t_{wake}	wake-up time	from sleep mode	[2][3]	-	1.6	-	µs
		from deep sleep mode with full SRAM retention: to code executing in flash or SRAM	[2]	-	18	-	µs
		from power down mode	[2]		180	-	µs
		from deep power-down mode; RTC disabled; using $\overline{\text{RESET}}$ pin.	[4]	-	200	-	µs

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

11.5 System PLL

Table 21. PLL lock times and current

T_{amb} = −40 °C to +105 °C, unless otherwise specified. V_{DD} = 1.62 V to 3.6 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
PLL configuration: input frequency 12 MHz; output frequency 75 MHz							
$t_{lock(PLL)}$	PLL lock time	PLL set-up procedure followed	[2]			400	µs
$I_{DD(PLL)}$	PLL current	when locked	[1][3]	-	-	550	µA
PLL configuration: input frequency 12 MHz; output frequency 100 MHz							
$t_{lock(PLL)}$	PLL lock time	PLL set-up procedure followed	[2]	-	-	400	µs
$I_{DD(PLL)}$	PLL current	when locked	[1][3]	-	-	750	µA
PLL configuration: input frequency 32.768 kHz; output frequency 75 MHz							
$t_{lock(PLL)}$	PLL lock time	-	[1]			6250	µs
$I_{DD(PLL)}$	PLL current	when locked	[1][3]	-	-	450	µA
PLL configuration: input frequency 32.768 kHz; output frequency 100 MHz							
$t_{lock(PLL)}$	PLL lock time	-	[1]	-	-	6250	µs
$I_{DD(PLL)}$	PLL current	when locked	[1][3]	-	-	560	µA

[1] Data based on characterization results, not tested in production.

[2] PLL set-up requires high-speed start-up and transition to normal mode. Lock times are only valid when high-speed start-up settings are applied followed by normal mode settings. The procedure for setting up the PLL is described in the LPC5410x user manual.

[3] PLL current measured using lowest CCO frequency to obtain the desired output frequency.

[6] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[7] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[8] The maximum $t_{HD;DAT}$ could be 3.45 μs and 0.9 μs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time. This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[9] tSU;DAT is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

[10] A Fast-mode I^2C-bus device can be used in a Standard-mode I^2C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I^2C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

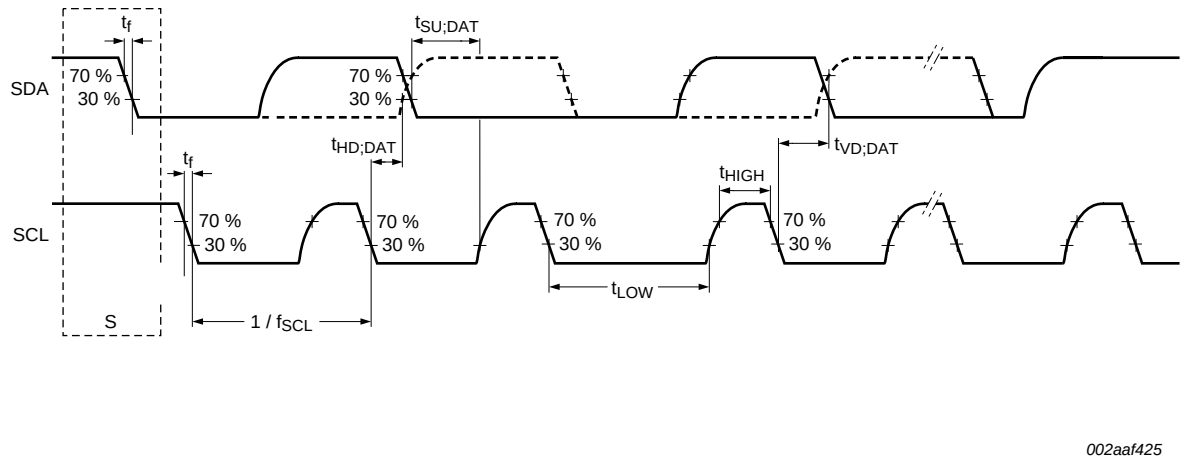


Fig 20. I^2C-bus pins clock timing

C_L - Crystal load capacitance

C_{Pad} - Pad capacitance of the RTCXIN and RTCXOUT pins (~3 pF).

$C_{Parasitic}$ – Parasitic or stray capacitance of external circuit.

Although $C_{Parasitic}$ can be ignored in general, the actual board layout and placement of external components influences the optimal values of external load capacitors. Therefore, it is recommended to fine tune the values of external load capacitors on actual hardware board to get the accurate clock frequency. For fine tuning, output the RTC Clock to one of the GPIOs and optimize the values of external load capacitors for minimum frequency deviation.

Table 34. Recommended values for the RTC external 32.768 kHz oscillator C_L, R_S, D_L, and C_{X1}/C_{X2} components

Crystal load capacitance C_L	Maximum crystal series resistance R_S	Maximum crystal drive level D_L	External load capacitors C_{X1}/C_{X2}
12.5 pF	< 70 kΩ	0.5 μW	22 pF, 22 pF

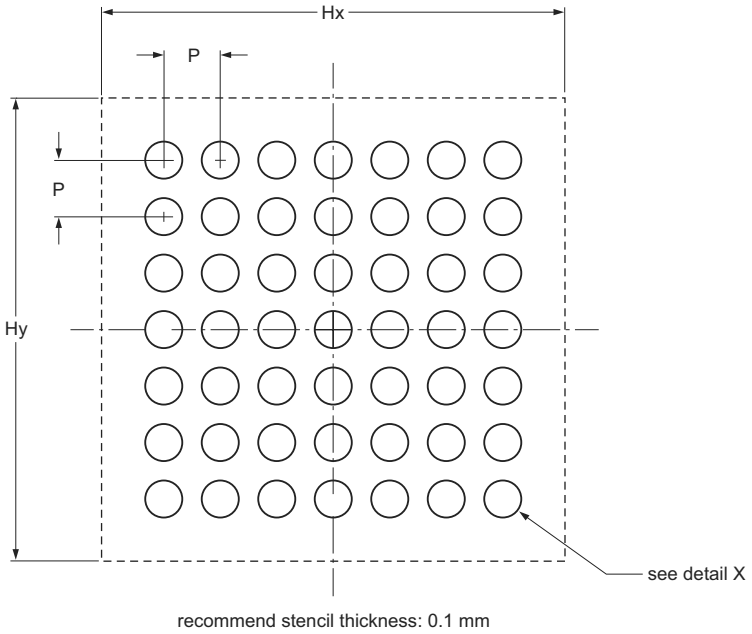
Remark: The crystals with lower CL (< 12.5 pF) values are not recommended.

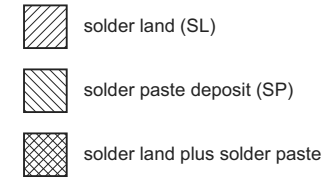
13.5.1 RTC Printed Circuit Board (PCB) design guidelines

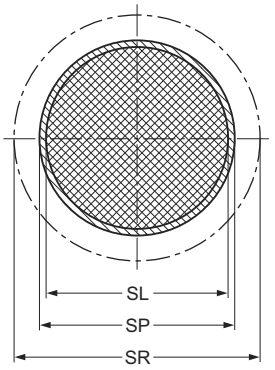
- Connect the crystal and external load capacitors on the PCB as close as possible (within 20 mm) to the oscillator input and output pins of the chip.
- The length of traces in the oscillation circuit should be as short as possible and must not cross other signal lines.
- Ensure that the load capacitors CX1, CX2, and CX3, in case of third overtone crystal usage, have a common ground plane.
- Loops must be made as small as possible to minimize the noise coupled in through the PCB and to keep the parasitics as small as possible.
- Lay out the ground (GND) pattern under crystal unit.
- Do not lay out other signal lines under crystal unit for multi-layered PCB.

15. Soldering

Footprint information for reflow soldering of WLCSP49 package **LPC5410_NSMD**







detail X

Dimensions in mm

P	SL	SP	SR	Hx	Hy
0.4	0.24	0.27	0.31	3.5	3.5

wlcsp49_lpc5410_fr

Fig 32. WLCSP49 Soldering footprint

16. Abbreviations

Table 35. Abbreviations

Acronym	Description
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
API	Application Programming Interface
DMA	Direct Memory Access
GPIO	General Purpose Input/Output
IRC	Internal RC
LSB	Least Significant Bit
MCU	MicroController Unit
PLL	Phase-Locked Loop
SPI	Serial Peripheral Interface
TTL	Transistor-Transistor Logic
USART	Universal Asynchronous Receiver/Transmitter

17. References

[1] LPC5410x User manual UM10850:
http://www.nxp.com/documents/user_manual/UM10850.pdf

[2] LPC5410x Errata sheet:
http://www.nxp.com/documents/errata_sheet/ES_LPC5410X.pdf

[3] Technical note ADC design guidelines:
http://www.nxp.com/documents/technical_note/TN00009.pdf

18. Revision history

Table 36. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC5410x v.2.9	20180126	Product data sheet	-	LPC5410x v2.8
Modification:	• Updated a feature in Section 7.16.2 “SPI serial I/O controller” Maximum supported bit rate for SPI master mode is 48 Mbit/s. Was 71 Mbit/s. • Updated Section 11.10 “SPI interfaces”: the maximum supported bit rate for SPI master mode is 48 Mbit/s. Was 71 Mbit/s.			
LPC5410x v.2.8	20171219	Product data sheet	-	LPC5410x v2.7
Modification:	• Updated Table 20 “Dynamic characteristic: Typical wake-up times from low power modes”.			
LPC5410x v.2.7	20170426	Product data sheet	-	LPC5410x v2.6
Modification:	• Updated Figure 28 “Power, clock, and debug connections”.			
LPC5410x v.2.6	20160926	Product data sheet	-	LPC5410x v2.5
Modification:	• Updated Table 13 “Static characteristics: Power consumption in deep sleep, power down, and deep power-down modes”: in deep power-down mode, the RTC oscillator running with external crystal typical value is 240 nA at: T_{amb} = −40 °C to +105 °C, 1.62 V ≤ V_{DD} ≤ 2.0 V; unless otherwise specified.			
LPC5410x v.2.5	20160913	Product data sheet	-	LPC5410x v2.4
Modification:	• Updated Table 10 “CoreMark score”: changed CoreMark scoreCoreMark code executed from flash; CCLK = 84 MHz; 4 system clock flash access time; CCLK = 100 MHz; 5 system clock flash access time to CCLK = 84 MHz; 5 system clock flash access time; CCLK = 100 MHz; 6 system clock flash access time			
LPC5410x v.2.4	20160711	Product data sheet	-	LPC5410x v2.3
Modification:	• Updated Table 27 “SPI dynamic characteristics[1]”: – Min values of SPI master 1.62V ≤ VDD ≤ 2.0 V, t_{DS} and $t_{v(Q)}$. – Min values of SPI slave 1.62V ≤ VDD ≤ 2.0 V, t_{DS}Hand $t_{v(Q)}$. – Min values of SPI master 2.7 V ≤ VDD ≤ 3.6 V, t_{DS}. – Min values of SPI slave 2.7 V ≤ VDD ≤ 3.6 V, t_{DH}. • Updated Table 28 “USART dynamic characteristics[1]”: – Min values of USART master (in synchronous mode) 1.62V ≤ VDD ≤ 2.0 V, $t_{h(D) \text{ and } tv(Q).}$ – Min values of USART slave (in synchronous mode) 1.62V ≤ VDD ≤ 2.0 V, $t_{h(D).}$ – Min values of USART master (in synchronous mode) 2.7V ≤ VDD ≤ 3.6V, $t_{h(D).}$ – Min values of USART slave (in synchronous mode) 2.7V ≤ VDD ≤ 3.6 V, $t_{h(D).}$ • Updated features of Section 7.16.2 “SPI serial I/O controller”: Maximum supported bit rate for SPI master mode is 71 Mbit/s, and the maximum supported bit rate for SPI slave mode is 21 Mbit/s. • Updated features of Section 7.16.1 “USART”: Maximum supported bit rate of 24 Mbit/s for USART master and slave synchronous modes. • Updated Table 22 “Dynamic characteristics of the PLL[1]”: – f_{ref} changed to F_{in}; reference frequency to input frequency. – removed $f_{refjitter}$. • Updated the description for Section 11.10 “SPI interfaces”.			
LPC5410x v2.3	20160524	Product data sheet	-	LPC5410x v2.2