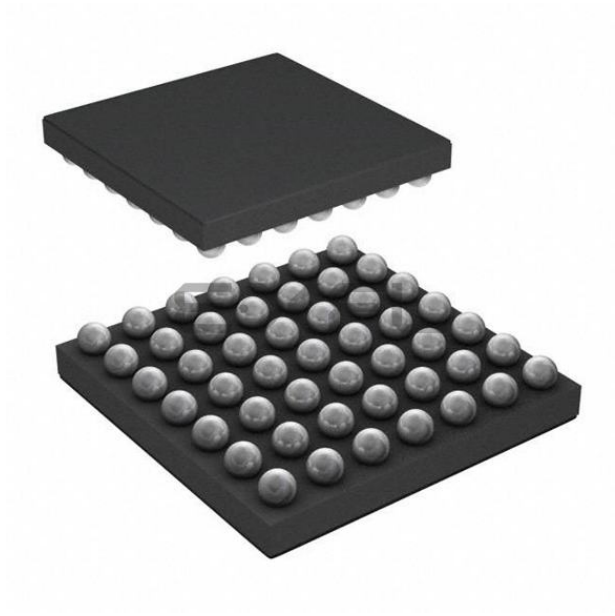

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	39
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	104K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	49-UFBGA, WLCSP
Supplier Device Package	49-WLCSP (3.29x3.29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc54101j512uk49z

The LPC5410x LQFP64 package has the following top-side marking:

- First line: LPC5410xJyyy
  - x: 2 = dual core (M4, M0+), 1 = single core (M4)
  - yyy: flash size
- Second line: BD64
- Third line: xxxxxxxxxxxx
- Fourth line: xxxyywwx[R]z
  - yyww: Date code with yy = year and ww = week.
  - xR = boot code version and device revision.

The LPC5410x WLCSP49 package has the following top-side marking:

- First line: LPC5410x
  - x: 2 = dual core (M4, M0+), 1 = single core (M4)
- Second line: JxxxUK49
  - xxx: flash size
- Third line: xxxxxxxx
- Fourth line: xxxyyww
  - yyww: Date code with yy = year and ww = week.
- Fifth line: xxxxx
- Sixth line: NXP x[R]z
  - xR = boot code version and device revision.

Table 3. Device revision table

Revision identifier (R)	Revision description
‘1B’	Initial device revision with boot code version 17.1.
‘1C’	Second device revision with boot code version 17.1.

Table 4. Pin description *…continued*

Symbol	WLCSP49	LQFP64		Reset state [1]	Type [6]	Description
PIO0_12	F7	47	[2]	PU	I/O	**PIO0_12 —** General-purpose digital input/output pin.
					I/O	**SPI0_MOSI —** Master Out Slave in for SPI0.
					O	**U1_TXD —** Transmitter output for USART1.
					O	**CT32B2_MAT3 —** 32-bit CT32B2 match output 3.
					I	**R —** Reserved.
PIO0_13	G7	48	[2]	PU	I/O	**PIO0_13 —** General-purpose digital input/output pin.
					I/O	**SPI0_MISO —** Master In Slave Out for SPI0.
					O	**SCT0_OUT4 —** SCT0 output 4. PWM output 4.
					O	**CT32B2_MAT0 —** 32-bit CT32B2 match output 0.
					I	**R —** Reserved.
PIO0_14/TCK	F6	49	[2]	PU	I/O	**PIO0_14 —** General-purpose digital input/output pin. In boundary scan mode: TCK (Test Clock).
					I/O	**SPI0_SSEL0 —** Slave Select 0 for SPI0.
					O	**SCT0_OUT5 —** SCT0 output 5. PWM output 5.
					O	**CT32B2_MAT1 —** 32-bit CT32B2 match output 1.
					I	**R —** Reserved.
PIO0_15/TDO	G6	50	[2]	PU	I/O	**PIO0_15 —** General-purpose digital input/output pin. In boundary scan mode: TDO (Test Data Out).
					I/O	**SPI0_SSEL1 —** Slave Select 1 for SPI0.
					I/O	**SWO —** Serial wire trace output.
					O	**CT32B2_MAT2 —** 32-bit CT32B2 match output 2.
					I	**R —** Reserved.
SWCLK/ PIO0_16	F5	52	[2]	PU	I/O	**PIO0_16 —** General-purpose digital input/output pin. After booting, this pin is connected to the SWCLK.
					I/O	**SPI0_SSEL2 —** Slave Select 2 for SPI0.
					I	**$\overline{\text{U1\_CTS}}$ —** Clear To Send input for USART1.
					O	**CT32B3_MAT1 —** 32-bit CT32B3 match output 1.
					I	**R —** Reserved.
					I/O	**SWCLK —** Serial Wire Clock. This is the default function after booting.
SWDIO/ PIO0_17	G5	53	[2]	PU	I/O	**PIO0_17 —** General-purpose digital input/output pin. After booting, this pin is connected to SWDIO.
					I/O	**SPI0_SSEL3 —** Slave Select 3 for SPI0.
					O	**$\overline{\text{U1\_RTS}}$ —** Request To Send output for USART1.
					O	**CT32B3_MAT2 —** 32-bit CT32B3 match output 2.
					I	**R —** Reserved.
					I/O	**SWDIO —** Serial Wire Debug I/O. This is the default function after booting.

Table 4. Pin description *…continued*

Symbol	WLCSP49	LQFP64		Reset state [1]	Type [6]	Description
PIO0_18/TRST	G4	58	[2]	PU	I/O	**PIO0_18 —** General-purpose digital input/output pin. In boundary scan mode: TRST (Test Reset).
					O	**U3_TXD —** Transmitter output for USART3.
					O	**SCT0_OUT0 —** SCT0 output 0. PWM output 0.
					O	**CT32B0_MAT0 —** 32-bit CT32B0 match output 0.
					I	**R —** Reserved.
PIO0_19/TDI	G3	59	[2]	PU	I/O	**PIO0_19 —** General-purpose digital input/output pin. In boundary scan mode: TDI (Test Data In).
					I/O	**U3_SCLK —** USART3 clock in synchronous USART mode.
					O	**SCT0_OUT1 —** SCT0 output 1. PWM output 1.
					O	**CT32B0_MAT1 —** 32-bit CT32B0 match output 1.
					I	**R —** Reserved.
PIO0_20/TMS	F3	60	[2]	PU	I/O	**PIO0_20 —** General-purpose digital input/output pin. In boundary scan mode: TMS (Test Mode Select).
					I	**U3_RXD —** Receiver input for USART3.
					I/O	**U0_SCLK —** USART0 clock in synchronous USART mode.
					I	**CT32B3_CAP0 —** 32-bit CT32B3 capture input 0.
					I	**R —** Reserved.
PIO0_21	E3	61	[2]	PU	I/O	**PIO0_21 —** General-purpose digital input/output pin.
					O	**CLKOUT —** Clock output pin.
					O	**U0_TXD —** Transmitter output for USART0.
					O	**CT32B3_MAT0 —** 32-bit CT32B3 match output 0.
					I	**R —** Reserved.
PIO0_22	G2	63	[2]	PU	I/O	**PIO0_22 —** General-purpose digital input/output pin.
					I	**CLKIN —** Clock input.
					I	**U0_RXD —** Receiver input for USART0.
					O	**CT32B3_MAT3 —** 32-bit CT32B3 match output 3.
					I	**R —** Reserved.
PIO0_23	F2	1	[3]	Z	I/O	**PIO0_23 —** General-purpose digital input/output pin.
					I/O	**I2C0_SCL —** I^2C0 clock input/output.
					I	**R —** Reserved.
					I	**CT32B0_CAP0 —** 32-bit CT32B0 capture input 0.
					I	**R —** Reserved.

Table 4. Pin description *…continued*

Symbol	WLCSP49	LQFP64		Reset state [1]	Type [6]	Description
PIO1_3/ ADC0_6	B2	17	[4]	PU	I/O; AI	**PIO1_3/ADC0_6 —** General-purpose digital input/output pin (default). ADC input channel 6 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					I/O	**SPI1_SSEL2 —** Slave Select 2 for SPI1.
					O	**SCT0_OUT6 —** SCT0 output 6.
					I	**R —** Reserved.
					I/O	**SPI0_SCK —** Serial clock for SPI0.
					I	**CT32B0_CAP1 —** 32-bit CT32B0 capture input 1.
PIO1_4/ ADC0_7	A2	18	[4]	PU	I/O; AI	**PIO1_4/ADC0_7 —** General-purpose digital input/output pin (default). ADC input channel 7 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					I/O	**SPI1_SSEL1 —** Slave Select 1 for SPI1.
					O	**SCT0_OUT7 —** SCT0 output 7.
					I	**R —** Reserved.
					I/O	**SPI0_MISO —** Master In Slave Out for SPI0.
					O	**CT32B0_MAT1 —** 32-bit CT32B0 match output 1.
PIO1_5/ ADC0_8	B3	19	[4]	PU	I/O; AI	**PIO1_5/ADC0_8 —** General-purpose digital input/output pin (default). ADC input channel 8 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					I/O	**SPI1_SSEL0 —** Slave Select 0 for SPI1.
					I	**CT32B1_CAP0 —** 32-bit CT32B1 capture input 0.
					I	**R —** Reserved.
					O	**CT32B1_MAT3 —** 32-bit CT32B1 match output 3.
					I	**R —** Reserved.
PIO1_6/ ADC0_9	A5	26	[4]	PU	I/O; AI	**PIO1_6/ADC0_9 —** General-purpose digital input/output pin (default). ADC input channel 9 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					I/O	**SPI1_SCK —** Serial clock for SPI1.
					I	**CT32B1_CAP2 —** 32-bit CT32B1 capture input 2.
					-	**R —** Reserved.
					O	**CT32B1_MAT2 —** 32-bit CT32B1 match output 2.
					I	**R —** Reserved.

Table 4. Pin description *…continued*

Symbol	WLCSP49	LQFP64		Reset state [1]	Type [6]	Description
PIO1_7/ ADC0_10	B5	27	[4]	PU	I/O; AI	**PIO1_7/ADC0_10 —** General-purpose digital input/output pin (default). ADC input channel 10 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					I/O	**SPI1_MOSI —** Master Out Slave in for SPI1.
					O	**CT32B1_MAT2 —** 32-bit CT32B1 match output 2.
					-	**R —** Reserved.
					I	**CT32B1_CAP2 —** 32-bit CT32B1 capture input 2.
					I	**R —** Reserved.
PIO1_8/ ADC0_11	C5	28	[4]	PU	I/O; AI	**PIO1_8/ADC0_11 —** General-purpose digital input/output pin (default). ADC input channel 11 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					I/O	**SPI1_MISO —** Master In Slave Out for SPI1.
					O	**CT32B1_MAT3 —** 32-bit CT32B1 match output 3.
					I	**R —** Reserved.
					I	**CT32B1_CAP3 —** 32-bit CT32B1 capture input 3.
					I	**R —** Reserved.
PIO1_9	-	29	[2]	PU	I/O	**PIO1_9 —** General-purpose digital input/output pin.
					I	**R —** Reserved.
					I/O	**SPI0_MOSI —** Master Out Slave In for SPI0.
					I	**CT32B0_CAP2 —** 32-bit CT32B0 capture input 2.
PIO1_10	-	30	[2]	PU	I/O	**PIO1_10 —** General-purpose digital input/output pin.
					I	**R —** Reserved.
					O	**U1_TXD —** Transmitter output for USART1.
					O	**SCT0_OUT4 —** SCT0 output 4.
PIO1_11	-	42	[2]	PU	I/O	**PIO1_11 —** General-purpose digital input/output pin.
					I	**R —** Reserved.
					O	**$\overline{\text{U1\_RTS}}$ —** Request To Send output for USART1.
					I	**CT32B1_CAP0 —** 32-bit CT32B1 capture input 0.
PIO1_12	-	51	[2]	PU	I/O	**PIO1_12 —** General-purpose digital input/output pin.
					I	**R —** Reserved.
					I	**U3_RXD —** Receiver input for USART3.
					O	**CT32B1_MAT0 —** 32-bit CT32B1 match output 0.
					I/O	**SPI1_SCK —** Serial clock for SPI1.
PIO1_13	-	54	[2]	PU	I/O	**PIO1_13 —** General-purpose digital input/output pin.
					I	**R —** Reserved.
					O	**U3_TXD —** Transmitter output for USART3.
					O	**CT32B1_MAT1 —** 32-bit CT32B1 match output 1.
					I/O	**SPI1_MOSI —** Master Out Slave In for SPI1.

6.2.1 Termination of unused pins

Table 5 shows how to terminate pins that are **not** used in the application. In many cases, unused pins should be connected externally or configured correctly by software to minimize the overall power consumption of the part.

Unused pins with GPIO function should be configured as outputs set to LOW with their internal pull-up disabled. To configure a GPIO pin as output and drive it LOW, select the GPIO function in the IOCON register, select output in the GPIO DIR register, and write a 0 to the GPIO PORT register for that pin. Disable the pull-up in the pin's IOCON register.

In addition, it is recommended to configure all GPIO pins that are not bonded out on smaller packages as outputs driven LOW with their internal pull-up disabled.

Table 5. Termination of unused pins

Pin	Default state[1]	Recommended termination of unused pins
$\overline{\text{RESET}}$	I; PU	The $\overline{\text{RESET}}$ pin can be left unconnected if the application does not use it.
all PIOn_m (not open-drain)	I; PU	Can be left unconnected if driven LOW and configured as GPIO output with pull-up disabled by software.
PIOn_m (I2C open-drain)	IA	Can be left unconnected if driven LOW and configured as GPIO output by software.
RTCXIN	-	Connect to ground. When grounded, the RTC oscillator is disabled.
RTCXOUT	-	Can be left unconnected.
VREFP	-	Tie to VDD.
VREFN	-	Tie to VSS.
VDDA	-	Tie to VDD.
VSSA	-	Tie to VSS.

[1] I = Input, IA = Inactive (no pull-up/pull-down enabled), PU = Pull-Up.

6.2.2 Pin states in different power modes

Table 6. Pin states in different power modes

Pin	Active	Sleep	Deep sleep/Power down	Deep power-down
PIOn_m pins (not I2C)	As configured in the IOCON[1]. Default: internal pull-up enabled.			Floating.
PIO0_23 to PIO0_28 (open-drain I2C-bus pins)	As configured in the IOCON[1].			Floating.
$\overline{\text{RESET}}$	Reset function enabled. Default: input, internal pull-up enabled. Reset function disabled.			

[1] Default and programmed pin states are retained in sleep, deep sleep, and power down modes.

The MPU separates the memory into distinct regions and implements protection by preventing disallowed accesses. The MPU supports up to eight regions each of which can be divided into eight subregions. Accesses to memory locations that are not defined in the MPU regions, or not permitted by the region setting, will cause the Memory Management Fault exception to take place.

7.5 Nested Vectored Interrupt Controller (NVIC) for Cortex-M4

The NVIC is an integral part of the Cortex-M4. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

7.5.1 Features

- Controls system exceptions and peripheral interrupts.
- 37 vectored interrupts.
- Eight programmable interrupt priority levels, with hardware priority level masking.
- Relocatable vector table.
- Non-Maskable Interrupt (NMI).
- Software interrupt generation.

7.5.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags.

7.6 ARM Cortex-M0+ co-processor

The ARM Cortex-M0+ co-processor offers high performance and very low power consumption. This processor uses a 2-stage pipeline von Neumann architecture and a small but powerful instruction set providing high-end processing hardware. The processor includes an NVIC with 32 interrupts and a separate system tick timer. In LPC5410x, the Cortex-M0 coprocessor hardware multiply is implemented as a 32-cycle iterative multiplier.

7.7 Nested Vectored Interrupt Controller (NVIC) for Cortex-M0+

The NVIC is an integral part of the Cortex-M0+. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

7.7.1 Features

- Controls system exceptions and peripheral interrupts.
- 32 vectored interrupts.
- Four programmable interrupt priority levels, with hardware priority level masking.
- Relocatable vector table.
- Non-Maskable Interrupt (NMI).
- Software interrupt generation.

7.12 Memory mapping

The LPC5410x incorporates several distinct memory regions. The APB peripheral area is 512 kB in size and is divided to allow for up to 32 peripherals.Each peripheral is allocated 16 kB of space simplifying the address decoding. The registers incorporated into the CPU, such as NVIC, SysTick, and sleep mode control, are located on the private peripheral bus.

Figure 6 shows the overall map of the entire address space from the user program viewpoint following reset.

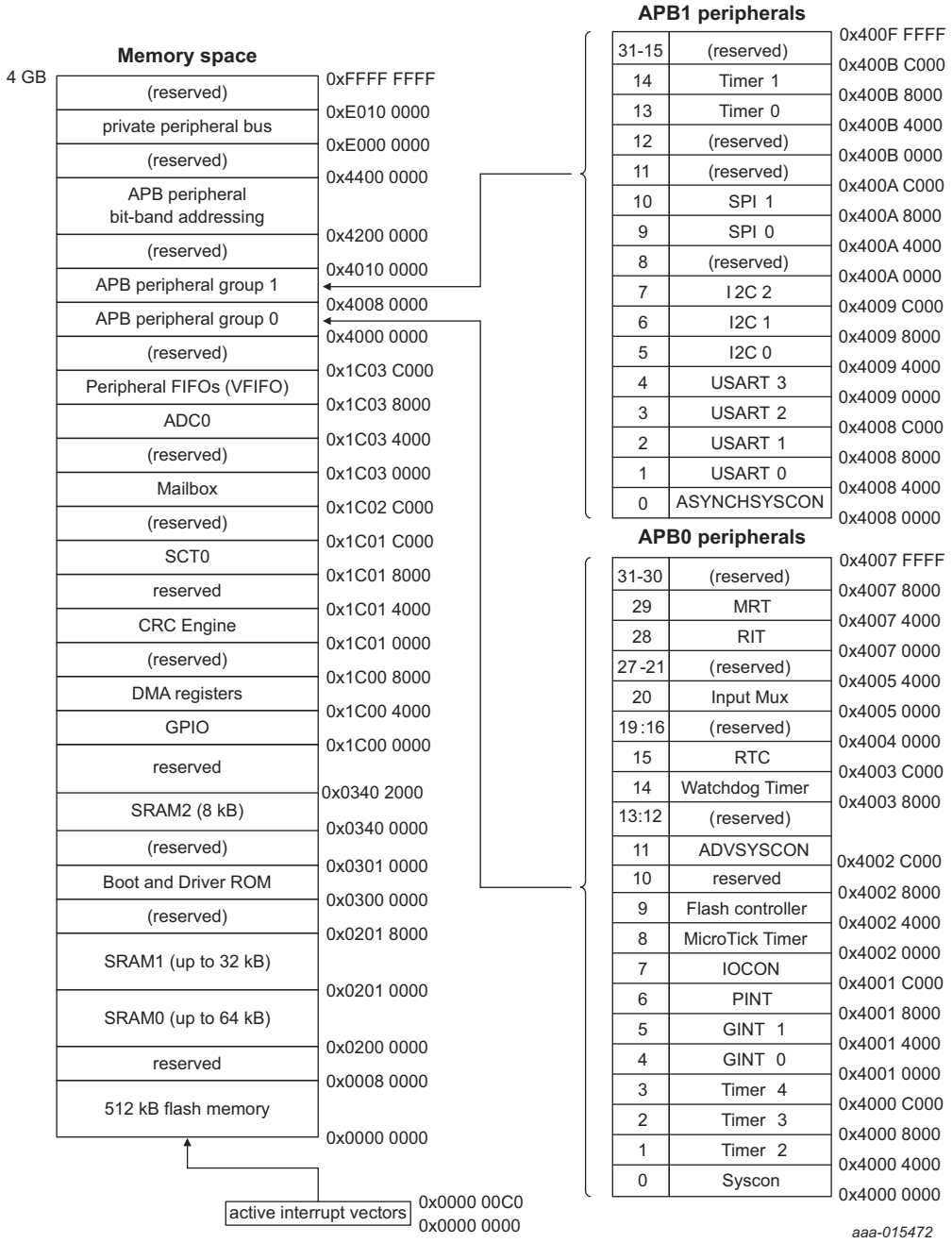


Fig 6. LPC5410x Memory mapping

- Counter or timer operation.
- For each timer with pin connections, up to 4 32-bit capture channels that can take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt.
- The timer and prescaler may be configured to be cleared on a designated capture event. This feature permits easy pulse-width measurement by clearing the timer on the leading edge of an input pulse and capturing the timer value on the trailing edge.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- For each timer with pin connections, up to 4 external outputs corresponding to match registers with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.
- PWM: for each timer with pin connections, up to 3 match outputs can be used as single edge controlled PWM outputs.

7.18.2 State Configurable Timer/PWM (SCTimer/PWM)

The SCTimer/PWM (SCT0) allows a wide variety of timing, counting, output modulation, and input capture operations. The inputs and outputs of the SCTimer/PWM are shared with the capture and match inputs/outputs of the 32-bit general-purpose counter/timers.

The SCTimer/PWM can be configured as two 16-bit counters or a unified 32-bit counter. In the two-counter case, in addition to the counter value the following operational elements are independent for each half:

- State variable
- Limit, halt, stop, and start conditions
- Values of Match/Capture registers, plus reload or capture control values

In the two-counter case, the following operational elements are global to the SCT, but the last three can use match conditions from either counter:

- Clock selection
- Inputs
- Events
- Outputs
- Interrupts

- Burst conversion mode for single or multiple inputs.
- Synchronous or asynchronous operation. Asynchronous operation maximizes flexibility in choosing the ADC clock frequency, Synchronous mode minimizes trigger latency and can eliminate uncertainty and jitter in response to a trigger.

7.20 System control

7.20.1 Clock sources

The LPC5410x supports two external and three internal clock sources:

- The Internal RC (IRC).
- Watchdog oscillator (WDOSC).
- External clock source from the digital I/O pin CLKIN.
- External RTC 32 KHz clock.
- Output of the system PLL.

7.20.1.1 Internal RC oscillator (IRC)

The IRC can be used as the clock that drives the system PLL and subsequently the CPU. The nominal IRC frequency is 12 MHz.

Upon power-up or any chip reset, the LPC5410x uses the IRC as the clock source. Software may later switch to one of the other available clock sources.

7.20.1.2 Watchdog oscillator (WDOSC)

The watchdog oscillator is a low-power internal oscillator. The WDOSC can be used to provide a clock to the WWDT and to the entire chip. The nominal output frequency is 500 kHz.

7.20.1.3 Clock input pin (CLKIN)

An external square-wave clock source (up to 25 MHz) can be supplied on the digital I/O pin CLKIN.

7.20.2 System PLL

The system PLL accepts an input clock frequency in the range of 32 kHz to 12 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO).

The PLL can be enabled or disabled by software.

7.20.4.1 Sleep mode

When sleep mode is entered, the clock to the core is stopped along with any unused peripherals. Waking up from the sleep mode does not need any special sequence other than re-enabling the clock to the ARM core.

In sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, internal buses, and unused peripherals. The processor state and registers, peripheral registers, and internal SRAM values are maintained, and the logic levels of the pins remain static.

7.20.4.2 Deep sleep mode

In deep sleep mode, all peripheral clocks and all clock sources are off with the option of keeping the 32 kHz clock and the WDOSC running. In addition, all analog blocks are shut down and the flash is put in stand-by mode. In deep sleep mode, the application can keep some of the internal clocks and the BOD circuit running for self-timed wake-up and BOD protection.

The LPC5410x can wake up from deep sleep mode via a reset, digital pins selected as inputs to the pin interrupt block, RTC alarm, Micro-tick, a watchdog timer reset interrupt, BOD interrupt/reset, or an interrupt from the USART (in 32 kHz mode or synchronous slave mode), the SPI, or any of the I2C peripherals. For wake-up from deep sleep mode, the SPI, USART, and I2C peripherals must be configured in slave mode.

Any interrupt used for waking up from deep sleep mode must be enabled in one of the SYSCON wake-up enable registers and the NVIC.

In deep sleep mode, the processor state and registers, peripheral registers, and internal SRAM values are maintained, and the logic levels of the pins remain static. deep sleep mode allows for very low quiescent power and fast wake-up options.

7.20.4.3 Power down mode

In power down mode, all peripheral clocks and all clock sources are off with the option of keeping the 32 kHz clock, and the WDOSC running. In addition, all analog blocks and the flash are shut down. In power down mode, the application can keep the BOD circuit running for BOD protection.

The LPC5410x can wake up from power down mode via a reset, digital pins selected as inputs to the pin interrupt block, RTC alarm, Micro-tick, a watchdog timer reset interrupt, BOD interrupt/reset, or an interrupt from the USART (in 32 kHz mode or synchronous slave mode), the SPI, or any of the I2C peripherals. For wake-up from power down mode, the SPI, USART, and I2C peripherals must be configured in slave mode.

In power down mode, the processor state and registers, peripheral registers, and internal SRAM values are maintained, and the logic levels of the pins remain static. Power down mode reduces power consumption compared to deep sleep mode at the expense of longer wake-up times.

Table 11. Static characteristics: Power consumption in active and sleep modes

T_{amb} = −40 °C to +105 °C, unless otherwise specified.1.62 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
ARM Cortex-M4 in active mode; ARM Cortex-M0+ in sleep mode							
I_{DD}	supply current	CoreMark code executed from SRAM; flash powered down					
		CCLK = 12 MHz	[2][4][6]	-	1.5	-	mA
		CCLK = 48 MHz	[3][4][6]	-	4.8	-	mA
		CCLK = 84 MHz	[3][4][6]	-	7.9	-	mA
		CCLK = 100 MHz	[3][4][6]	-	9.9	-	mA
I_{DD}	supply current	CoreMark code executed from flash;					
		CCLK = 12 MHz; 1 system clock flash access time.	[2][4][6]	-	1.9	-	mA
		CCLK = 48 MHz; 3 system clock flash access time.	[3][4][6]	-	5.7	-	mA
		CCLK = 84 MHz; 6 system clock flash access time.	[3][4][6]	-	8.8	-	mA
		CCLK = 100 MHz; 7 system clock flash access time.	[3][4][6]	-	10.7	-	mA
I_{DD}	supply current	Calculating Fibonacci numbers executed from SRAM;					
		CCLK = 12 MHz	[2][4][5]	-	1.7	-	mA
		CCLK = 84 MHz	[3][4][5]	-	8.0	-	mA
		CCLK = 96 MHz	[3][4][5]	-	9.4	-	mA
I_{DD}	supply current	Calculating Fibonacci numbers executed from flash;					
		CCLK = 12 MHz	[2][4][5]	-	1.7	-	mA
		CCLK = 84 MHz	[3][4][5]	-	8.0	-	mA
		CCLK = 96 MHz	[3][4][5]	-	9.4	-	mA

[6] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[7] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[8] The maximum $t_{HD;DAT}$ could be 3.45 μs and 0.9 μs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time. This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[9] tSU;DAT is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

[10] A Fast-mode I^2C-bus device can be used in a Standard-mode I^2C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I^2C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

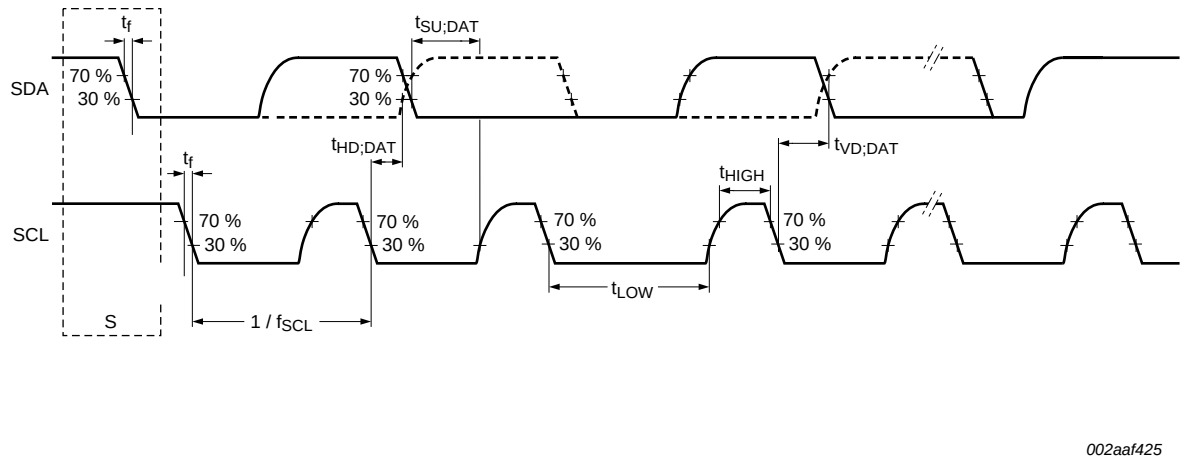


Fig 20. I^2C-bus pins clock timing

11.10 SPI interfaces

The actual SPI bit rate depends on the delays introduced by the external trace, the external device, system clock (CCLK), and capacitive loading. Excluding delays introduced by external device and PCB, the maximum supported bit rate for SPI master mode is 48 Mbit/s, and the maximum supported bit rate for SPI slave mode is 21 Mbit/s.

Table 27. SPI dynamic characteristics[1]

T_{amb} = −40 °C to 105 °C; C_L = 30 pF balanced loading on all pins; SLEW = standard mode. Parameters sampled at the 50 % level of the rising or falling edge.

Symbol	Parameter	Conditions		Min	Max	Unit
SPI master 1.62V ≤ VDD ≤ 2.0 V						
t_{DS}	data set-up time	CCLK = 1 MHz to 12 MHz		0	-	ns
		CCLK = 48 MHz to 60 MHz		0	-	ns
		CCLK = 96 MHz		0	-	ns
t_{DH}	data hold time	CCLK = 1 MHz to 12 MHz		14	-	ns
		CCLK = 48 MHz to 60 MHz		12	-	ns
		CCLK = 96 MHz		9	-	ns
$t_{v(Q)}$	data output valid time	CCLK = 1 MHz to 12 MHz		0	7	ns
		CCLK = 48 MHz to 60 MHz		0	2	ns
		CCLK = 96 MHz		0	2	ns
SPI slave 1.62V ≤ VDD ≤ 2.0 V						
t_{DS}	data set-up time	CCLK = 1 MHz to 12 MHz		22	-	ns
		CCLK = 48 MHz to 60 MHz		4	-	ns
		CCLK = 96 MHz		4	-	ns
t_{DH}	data hold time	CCLK = 1 MHz to 12 MHz		0	-	ns
		CCLK = 48 MHz to 60 MHz		0	-	ns
		CCLK = 96 MHz		0	-	ns
$t_{v(Q)}$	data output valid time	CCLK = 1 MHz to 12 MHz		46	70	ns
		CCLK = 48 MHz to 60 MHz		30	37	ns
		CCLK = 96 MHz		30	36	ns
SPI master 2.7 V ≤ VDD ≤ 3.6 V						
t_{DS}	data set-up time	CCLK = 1 MHz to 12 MHz		0	-	ns
		CCLK = 48 MHz to 60 MHz		0	-	ns
		CCLK = 96 MHz		0	-	ns
t_{DH}	data hold time	CCLK = 1 MHz to 12 MHz		10	-	ns
		CCLK = 48 MHz to 60 MHz		8	-	ns
		CCLK = 96 MHz		7	-	ns
$t_{v(Q)}$	data output valid time	CCLK = 1 MHz to 12 MHz		0	6	ns
		CCLK = 48 MHz to 60 MHz		0	1	ns
		CCLK = 96 MHz		0	1	ns
SPI slave 2.7V ≤ VDD ≤ 3.6 V						
t_{DS}	data set-up time	CCLK = 1 MHz to 12 MHz		21	-	ns
		CCLK = 48 MHz to 60 MHz		4	-	ns
		CCLK = 96 MHz		3	-	ns

12.2 12-bit ADC characteristics

Table 31. 12-bit ADC static characteristics

T_{amb} = −40 °C to +105 °C; 1.62 V ≤ V_{DD} ≤ 3.6 V; VREFP = V_{DDA}; V_{SSA} = VREFN = GND. ADC calibrated at T_{amb} = 25 °C.

Symbol	Parameter	Conditions		Min	Typ[2]	Max	Unit
V_{IA}	analog input voltage		[3]	0	-	V_{DDA}	V
C_{ia}	analog input capacitance		[4]	-	5	-	pF
$f_{clk(ADC)}$	ADC clock frequency				-	80	MHz
f_s	sampling frequency			-	-	5.0	Msamples/s
E_D	differential linearity error	V_{DDA} = VREFP = 1.62 V	[1][5]	-	±3	-	LSB
		V_{DDA} = VREFP = 3.6 V			±2		LSB
$E_{L(adj)}$	integral non-linearity	V_{DDA} = VREFP = 1.62 V	[1][6]	-	±5	-	LSB
		V_{DDA} = VREFP = 3.6 V		-	±2	-	LSB
E_O	offset error	calibration enabled	[1][7]	-	±5.6	-	mV
$V_{err(FS)}$	full-scale error voltage	V_{DDA} = VREFP = 1.62 V	[1][8]	-	±3		LSB
		V_{DDA} = VREFP = 3.6 V		-	±3		LSB
Z_i	input impedance	f_s = 5.0 Msamples/s	[9][10]	17.0	-	-	kΩ

[1] Based on characterization; not tested in production.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[3] The input resistance of ADC channels 6 to 11 is higher than ADC channels 0 to 5.

[4] C_{ia} represents the external capacitance on the analog input channel for sampling speeds of 5.0 Msamples/s. No parasitic capacitances included.

[5] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 24.

[6] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 24.

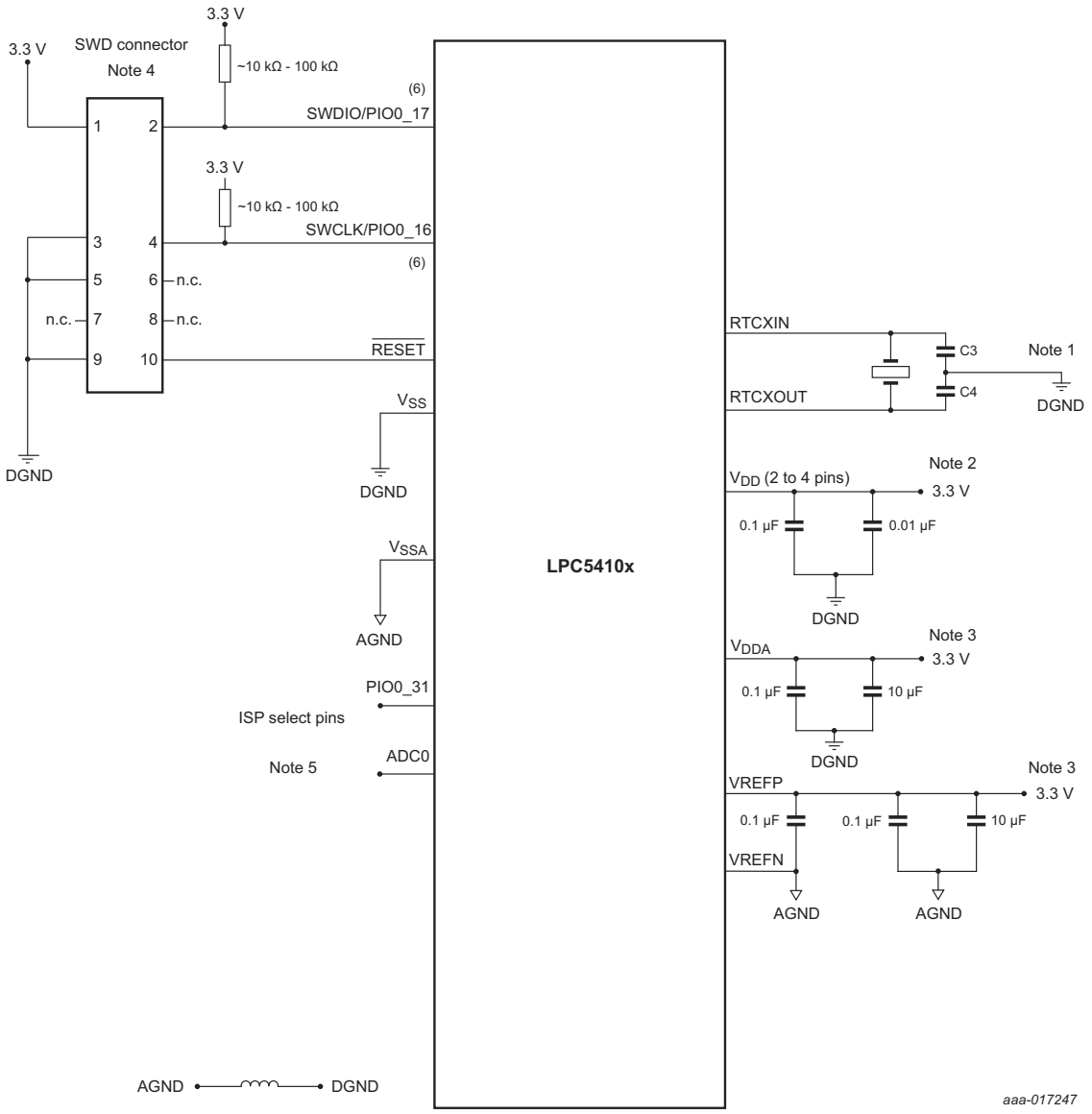
[7] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 24.

[8] The full-scale error voltage or gain error (E_G) is the difference between the straight-line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 24.

[9] T_{amb} = 25 °C; maximum sampling frequency f_s = 5.0 Msamples/s and analog input capacitance C_{ia} = 5 pF.

[10] Input impedance Z_i is inversely proportional to the sampling frequency and the total input capacity including C_{ia} and C_{io}: $Z_i \propto 1 / (f_s \times C_i)$. See Table 16 for C_{io}. See Figure 25.

13.3 Connecting power, clocks, and debug functions



(1) See Section 13.5 “RTC oscillator” for the values of C3 and C4.

(2) Position the decoupling capacitors of 0.1 µF and 0.01 µF as close as possible to the V_{DD} pin. Add one set of decoupling capacitors to each V_{DD} pin.

(3) Position the decoupling capacitors of 0.1 µF as close as possible to the VREFN and V_{DDA} pins. The 10 µF bypass capacitor filters the power line. Tie V_{DDA} and VREFP to V_{DD} if the ADC is not used. Tie VREFN to V_{SS} if ADC is not used.

(4) Uses the ARM 10-pin interface for SWD.

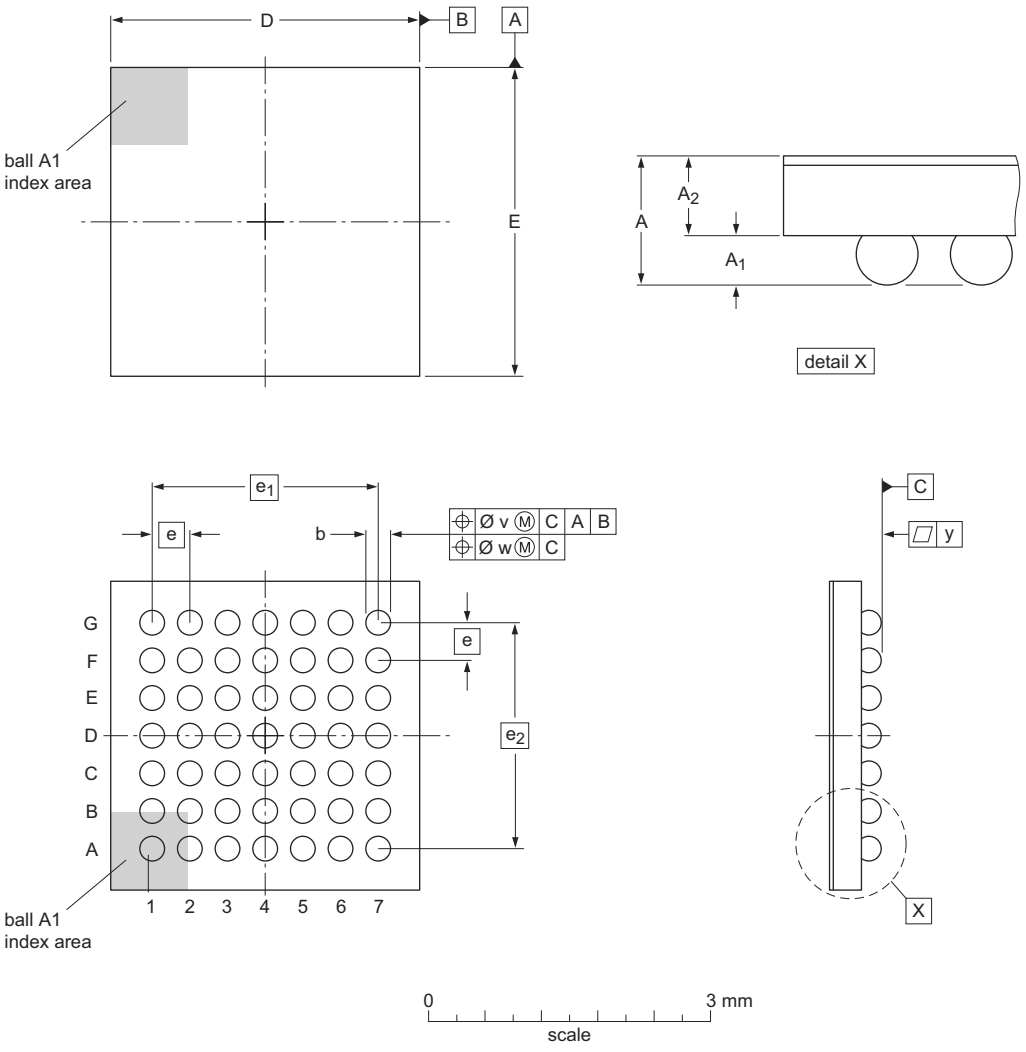
(5) When measuring signals of low frequency, use a low-pass filter to remove noise and to improve ADC performance. Also see Ref. 3.

(6) External pull-up resistors on SWDIO and SWCLK pins are optional because these pins have an internal pull-up enabled by default.

Fig 28. Power, clock, and debug connections

14. Package outline

WLCSP49: wafer level chip-scale package; 49 bumps; 3.29 x 3.29 x 0.54 mm (backside coating included) **LPC5410**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y
mm	max	0.58	0.23	0.37	0.29	3.318	3.318	0.4	2.4	2.4	0.05	0.015	0.03
	nom	0.54	0.20	0.34	0.26	3.288	3.288						
	min	0.50	0.17	0.31	0.23	3.258	3.258						

Note
Backside coating 40 µm

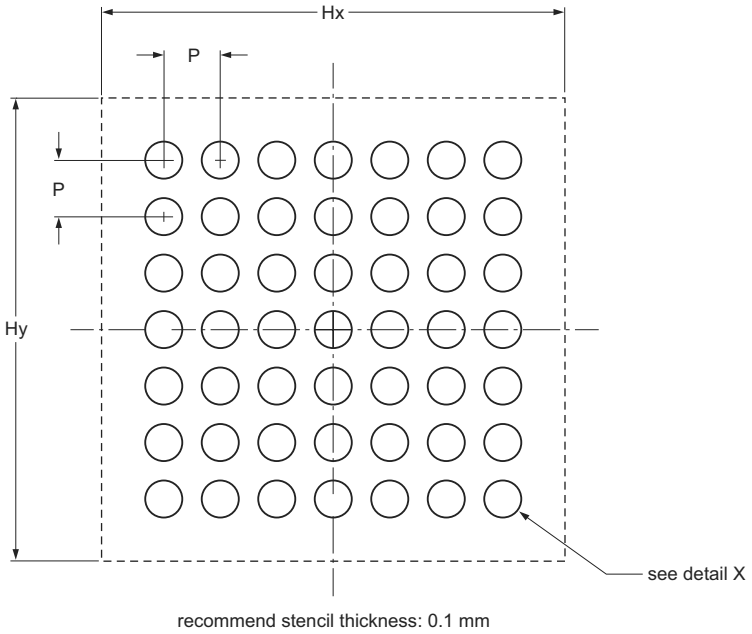
wlcsp49_lpc5410_po

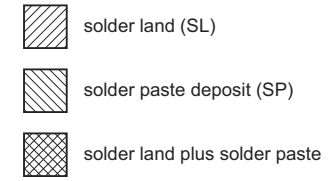
Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
LPC5410		- - -				~~13-09-16~~ 14-11-03

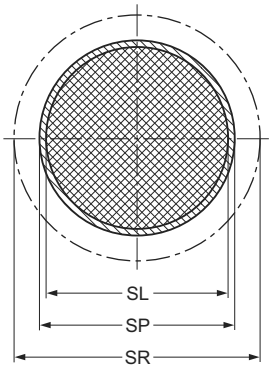
Fig 30. WLCSP49 Package outline

15. Soldering

Footprint information for reflow soldering of WLCSP49 package **LPC5410_NSMD**







detail X

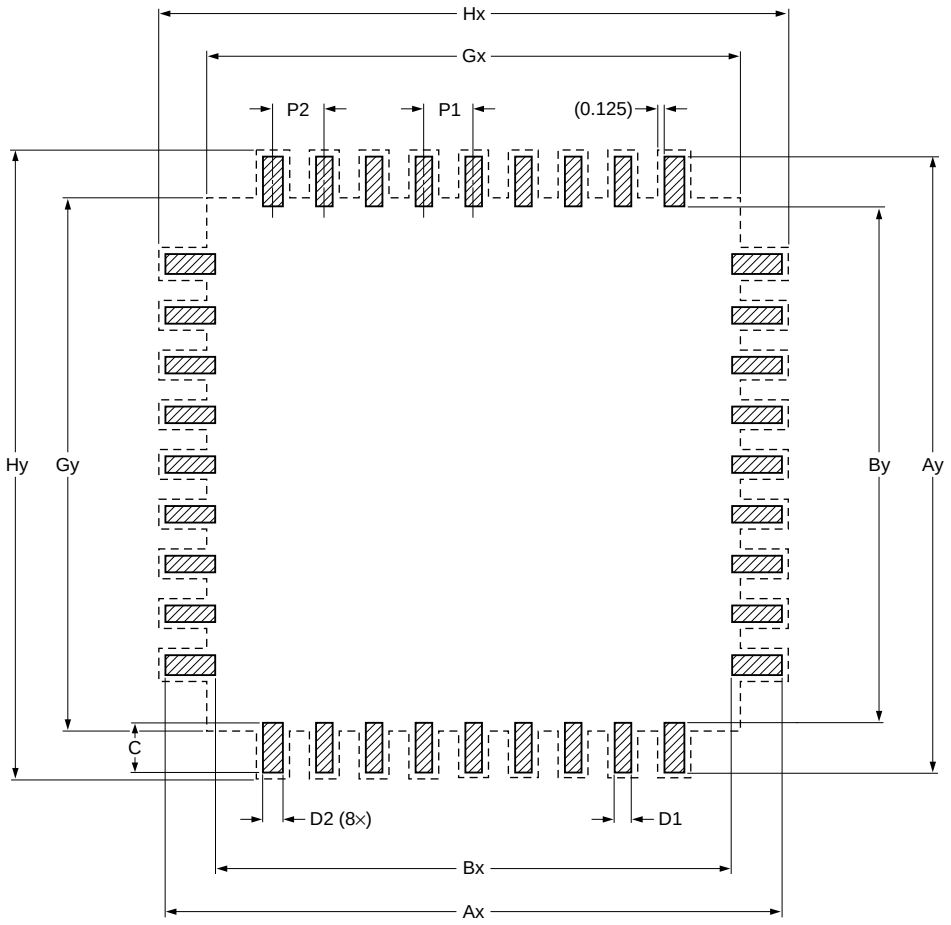
Dimensions in mm

P	SL	SP	SR	Hx	Hy
0.4	0.24	0.27	0.31	3.5	3.5

wlcsp49_lpc5410_fr

Fig 32. WLCSP49 Soldering footprint

Footprint information for reflow soldering of LQFP64 package **SOT314-2**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	13.300	13.300	10.300	10.300	1.500	0.280	0.400	10.500	10.500	13.550	13.550

sot314-2_fr

Fig 33. LQFP64 Soldering footprint

21. Contents

continued >>