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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4/M0+ |
| Core Size | 32-Bit Dual-Core |
| Speed | 100MHz |
| Connectivity | I²C, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 50 |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 104K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.62V ~ 3.6V |
| Data Converters | A/D 12x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP |
| Supplier Device Package | 64-LQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc54102j256bd64ql |

- ARM Cortex-M0+ core (version r0p1):
  - ARM Cortex-M0+ processor, running at a frequency of up to 100 MHz.
  - ARM Cortex-M0+ built-in Nested Vectored Interrupt Controller (NVIC).
  - Non-maskable Interrupt (NMI) input with a selection of sources.
  - Serial Wire Debug with four breakpoints and two watch points.
  - System tick timer.
- On-chip memory:
  - Up to 512 kB on-chip flash program memory with flash accelerator and 256 byte page erase and write.
  - 104 kB total SRAM composed of:
  - Up to 96 kB contiguous main SRAM.
  - An additional 8 kB SRAM.
- ROM API support:
  - Flash In-Application Programming (IAP) and In-System Programming (ISP).
  - Power control API.
- Serial interfaces:
  - Four USART interfaces with synchronous mode and 32 kHz mode for wake-up from deep sleep and power down modes. The USARTs have FIFO support from the System FIFO and share a fractional baud-rate generator.
  - Two SPI interfaces, each with four slave selects and flexible data configuration. The SPIs have FIFO support from the System FIFO. The slave function is able to wake up the device from deep sleep and power down modes.
  - Three $I^2C$-bus interfaces supporting fast mode and Fast-mode Plus with data rates of up to 1Mbit/s and with multiple address recognition and monitor mode. Each $I^2C$-bus interface also supports High Speed Mode (3.4 Mbit/s) as a slave. The slave function is able to wake up the device from deep sleep and power down modes.
- Digital peripherals:
  - DMA controller with 22 channels and 20 programmable triggers, able to access all memories and DMA-capable peripherals.
  - Up to 50 General-Purpose Input/Output (GPIO) pins. Most GPIOs have configurable pull-up/pull-down resistors, programmable open-drain mode, and input inverter.
  - GPIO registers are located on the AHB for fast access. The DMA supports GPIO ports.
  - Up to eight GPIOs (pin interrupts) can be selected as edge-sensitive (rising or falling edges or both) interrupt requests or level-sensitive (active low or active high) interrupt requests. In addition, up to eight GPIOs can be selected to contribute a boolean expression and interrupt generation using the pattern match engine block.
  - Two GPIO grouped interrupts (GINT) enable an interrupt based on a logical (AND/OR) combination of input states.
  - CRC engine.
- Timers:
  - Five 32-bit standard general purpose timers/counters, four of which support up to 4 capture inputs and 4 compare outputs, PWM mode, and external count input. Specific timer events can be selected to generate DMA requests. The fifth timer does not have external pin connections and may be used for internal timing operations.

- One State Configurable Timer/PWM (SCT/PWM) with 8 inputs (6 external inputs and 2 internal inputs) and 8 output functions (including capture and match). Inputs and outputs can be routed to/from external pins and internally to/from selected peripherals. Internally, the SCT supports 13 captures/matches, 13 events and 13 states.
- 32-bit Real-time clock (RTC) with 1 s resolution running in the always-on power domain. A timer in the RTC can be used for wake-up from all low power modes including deep power-down, with 1 ms resolution.
- Multiple-channel multi-rate 24-bit timer (MRT) for repetitive interrupt generation at up to four programmable, fixed rates.
- Windowed Watchdog Timer (WWDT).
- Ultra-low power Micro-tick Timer, running from the Watchdog oscillator, that can be used to wake up the device from low power modes.
- Repetitive Interrupt Timer (RIT) for debug time-stamping and general-purpose use.

- Analog peripheral: 12-bit, 12-channel, Analog-to-Digital Converter (ADC) supporting 5.0 Msamples/s. The ADC supports two independent conversion sequences.
- Clock generation:
  - 12 MHz internal RC oscillator.
  - External clock input for clock frequencies of up to 25 MHz.
  - Internal low-power, watchdog oscillator (WDOSC) with a nominal frequency of 500 kHz.
  - 32 kHz low-power RTC oscillator.
  - System PLL allows CPU operation up to the maximum CPU rate. May be run from the internal RC oscillator, the external clock input CLKIN, or the RTC oscillator.
  - Clock output function for monitoring internal clocks.
  - Frequency measurement unit for measuring the frequency of any on-chip or off-chip clock signal.
- Power-saving modes and wake-up:
  - Integrated PMU (Power Management Unit) to minimize power consumption.
  - Reduced power modes: sleep, deep sleep, power down, and deep power-down.
  - Wake-up from deep sleep and power down modes via activity on the USART, SPI, and $I^2C$ peripherals.
  - Wake-up from sleep, deep sleep, power down, and deep power-down modes using the RTC alarm.
- Single power supply 1.62 V to 3.6 V.
- Power-On Reset (POR).
- Brown-Out Detect (BOD) with separate thresholds for interrupt and forced reset.
- JTAG boundary scan supported.
- Unique device serial number (128 bit) for identification.
- Operating temperature range −40 °C to 105 °C.
- Available in a 3.288 x 3.288 mm WLCSP49 package and LQFP64 package.

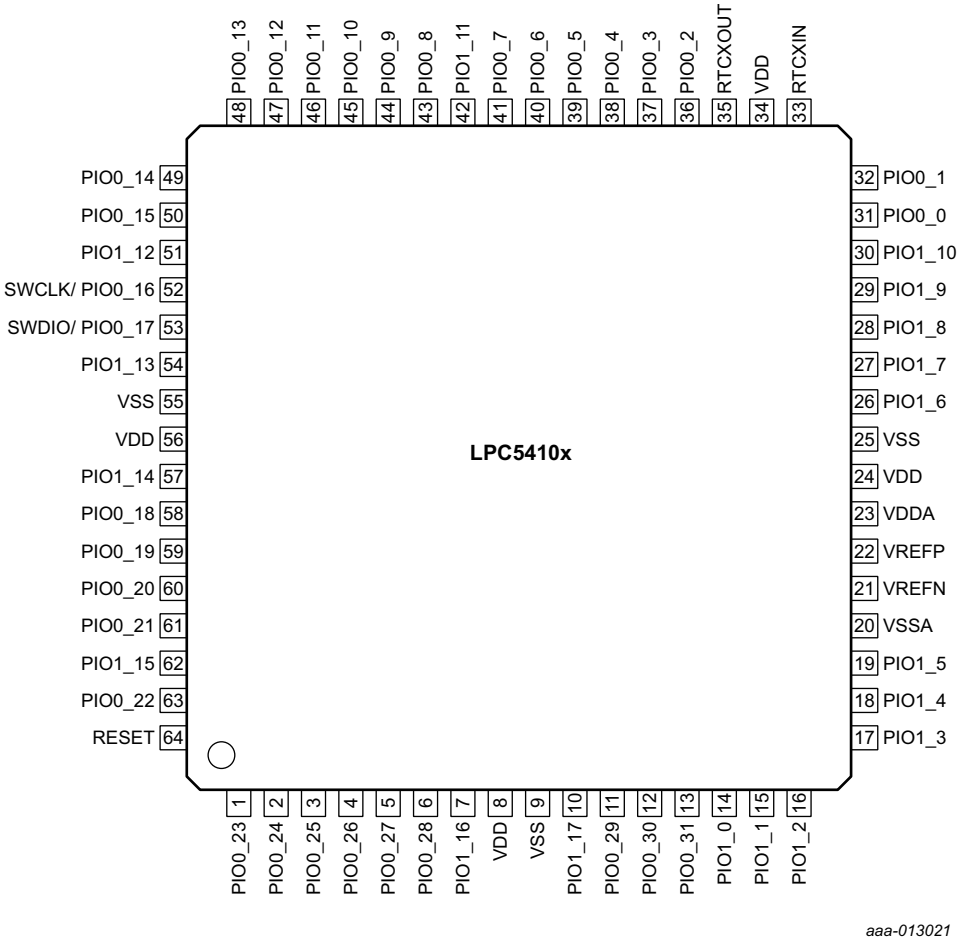



**Fig 5. LQFP64 Pin configuration**

## 6.2 Pin description

On the LPC5410x, digital pins are grouped into two ports. Each digital pin may support up to four different digital functions and one analog function, including General Purpose I/O (GPIO).

**Table 4. Pin description**

| Symbol | WLCSP49 | LQFP64 | | Reset state [1] | Type [6] | Description |
|---|---|---|---|---|---|---|
| PIO0_0 | A6 | 31 | [2] | PU | I/O | **PIO0_0 —** General-purpose digital input/output pin.<br>**Remark:** In ISP mode, this pin is the UART0 RXD function. |
| | | | | | I | **U0_RXD —** Receiver input for USART0. |
| | | | | | I/O | **SPI0_SSEL0 —** Slave Select 0 for SPI0. |
| | | | | | I | **CT32B0_CAP0 —** 32-bit CT32B0 capture input 0. |
| | | | | | I | **R —** Reserved. |
| | | | | | O | **SCT0_OUT3 —** SCT0 output 3. PWM output 3. |
| PIO0_1 | B6 | 32 | [2] | PU | I/O | **PIO0_1 —** General-purpose digital input/output pin.<br>**Remark:** In ISP mode, this pin is the UART0 TXD function. |
| | | | | | O | **U0_TXD —** Transmitter output for USART0. |
| | | | | | I/O | **SPI0_SSEL1 —** Slave Select 1 for SPI0. |
| | | | | | I | **CT32B0_CAP1 —** 32-bit CT32B0 capture input 1. |
| | | | | | I | **R —** Reserved. |
| | | | | | O | **SCT0_OUT1 —** SCT0 output 1. PWM output 1. |
| PIO0_2 | - | 36 | [2] | PU | I/O | **PIO0_2 —** General-purpose digital input/output pin. |
| | | | | | I | **$\overline{\text{U0\_CTS}}$ —** Clear To Send input for USART0. |
| | | | | | I | **R —** Reserved. |
| | | | | | I | **CT32B2_CAP1 —** 32-bit CT32B2 capture input 1. |
| | | | | | I | **R —** Reserved. |
| PIO0_3 | - | 37 | [2] | PU | I/O | **PIO0_3 —** General-purpose digital input/output pin. |
| | | | | | O | **$\overline{\text{U0\_RTS}}$ —** Request To Send output for USART0. |
| | | | | | I | **R —** Reserved. |
| | | | | | O | **CT32B1_MAT3 —** 32-bit CT32B1 match output 3. |
| | | | | | I | **R —** Reserved. |
| PIO0_4 | C7 | 38 | [2] | PU | I/O | **PIO0_4 —** General-purpose digital input/output pin. |
| | | | | | I/O | **U0_SCLK —** USART0 clock in synchronous USART mode. |
| | | | | | I/O | **SPI0_SSEL2 —** Slave Select 2 for SPI0. |
| | | | | | I | **CT32B0_CAP2 —** 32-bit CT32B0 capture input 2. |
| | | | | | I | **R —** Reserved. |

- Pattern match engine:
  - Up to eight pins can be selected from all digital pins on ports 0 and 1 to contribute to a boolean expression. The boolean expression consists of specified levels and/or transitions on various combinations of these pins.
  - Each bit slice minterm (product term) comprising of the specified boolean expression can generate its own, dedicated interrupt request.
  - Any occurrence of a pattern match can also be programmed to generate an RXEV notification to the CPU. The RXEV signal can be connected to a pin.
  - Pattern match can be used in conjunction with software to create complex state machines based on pin inputs.
  - Pattern match engine facilities wake-up only from active and sleep modes.

## 7.15 AHB peripherals

### 7.15.1 DMA controller

The DMA controller allows peripheral-to memory, memory-to-peripheral, and memory-to-memory transactions. Each DMA stream provides unidirectional DMA transfers for a single source and destination.

#### 7.15.1.1 Features

- 22 channels, 21 of which are connected to peripheral DMA requests. These come from the USART, SPI, and $I^2C$ peripherals. One spare channels has no DMA request connected, and can be used for functions such as memory-to-memory moves.
- DMA operations can be triggered by on- or off-chip events. Each DMA channel can select one trigger input from 20 sources. Trigger sources include ADC interrupts, Timer interrupts, pin interrupts, and the SCT DMA request lines.
- Priority is user selectable for each channel.
- Continuous priority arbitration.
- Address cache.
- Efficient use of data bus.
- Supports single transfers up to 1,024 words.
- Address increment options allow packing and/or unpacking data.

## 7.16 Digital serial peripherals

### 7.16.1 USART

#### 7.16.1.1 Features

- Synchronous mode with master or slave operation. Includes data phase selection and continuous clock option.
- Maximum bit rates of 6.25 Mbit/s in asynchronous mode.
- Maximum supported bit rate of 24 Mbit/s for USART master and slave synchronous modes.
- 7, 8, or 9 data bits and 1 or 2 stop bits.

### 7.20.3 Clock Generation

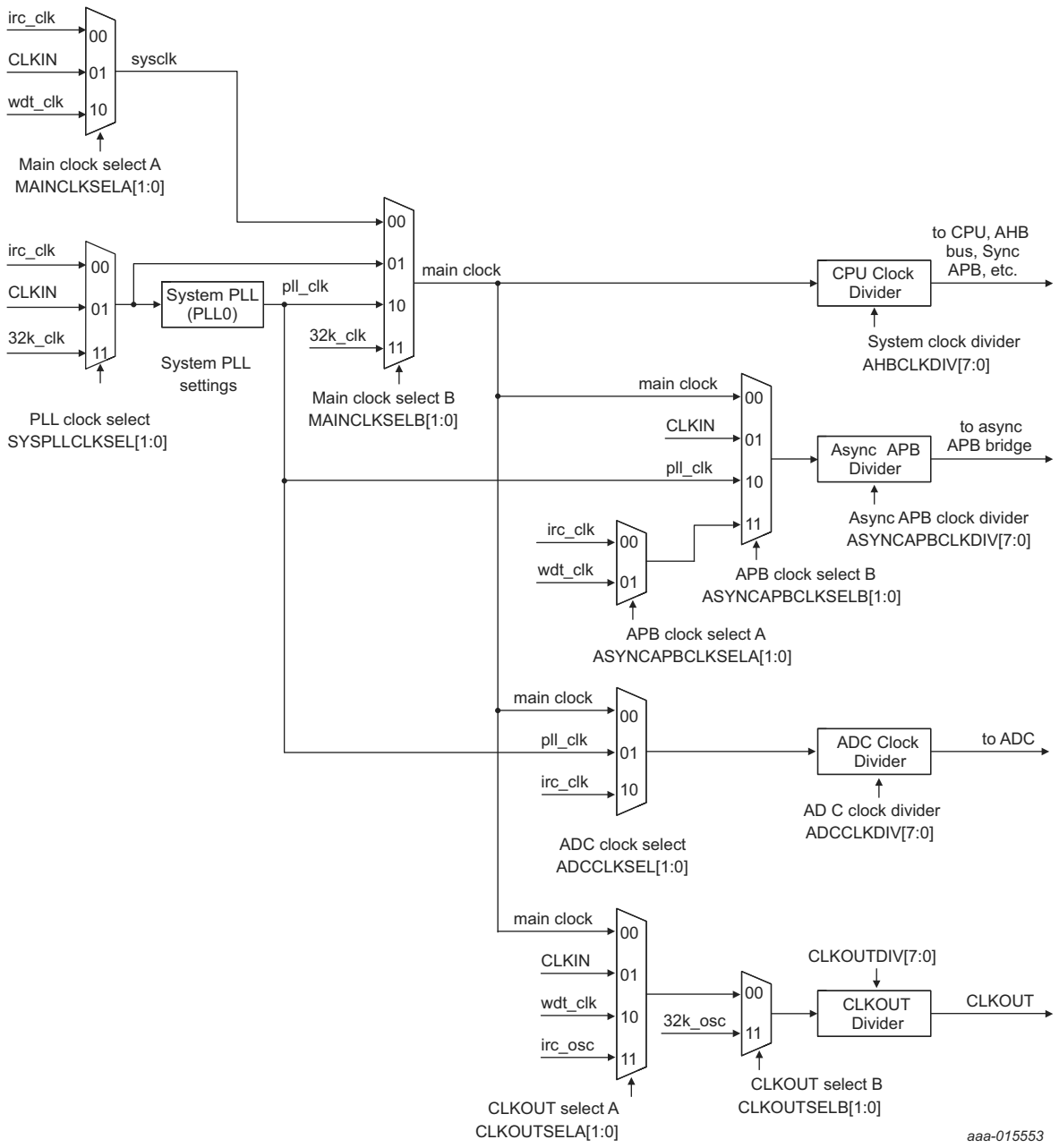



**Fig 7. LPC5410x clock generation**

### 7.20.4 Power control

The LPC5410x support a variety of power control features. In Active mode, when the chip is running, power and clocks to selected peripherals can be optimized for power consumption. In addition, there are four special modes of processor power reduction with different peripherals running: Sleep mode, deep sleep mode, power down mode, and deep power-down mode, activated by the power mode configure API.

**Table 12. Static characteristics: Power consumption in deep sleep, power down, and deep power-down modes**
*$T_{amb}$ = −40 °C to +105 °C, 1.62 V ≤ $V_{DD}$ ≤ 2.0 V; unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ[1][2] | Max[3] | Unit |
|---|---|---|---|---|---|---|---|
| $I_{DD}$ | supply current | Deep sleep mode; all SRAM on: | [2] | | | | |
| | | $T_{amb}$ = 25 °C | | - | 235 | 380 | µA |
| | | $T_{amb}$ = 105 °C | | - | - | 1.9 | mA |
| | | Power down mode; | [2] | | | | |
| | | first 8 kB in SRAM0 powered: | | | | | |
| | | $T_{amb}$ = 25 °C | | - | 4 | 8 | µA |
| | | $T_{amb}$ = 105 °C | | | - | 110 | µA |
| | | SRAM0 (64 kB) powered | | - | 6.7 | - | µA |
| | | SRAM0 (64 kB), SRAM1 (32 kB) powered | | - | 7.8 | - | µA |
| | | SRAM0 (64 kB), SRAM1 (32 kB), SRAM2 (8 kB) powered | | - | 8.2 | - | µA |
| | | Deep power-down mode; | [2] | - | | | |
| | | RTC oscillator input grounded (RTC oscillator disabled) | | | | | |
| | | $T_{amb}$ = 25 °C | | | 160 | 340 | nA |
| | | $T_{amb}$ = 105 °C | | | - | 14 | µA |
| | | RTC oscillator running with external crystal | | - | 240 | - | nA |

[1] Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C).

[2] Characterized through bench measurements using typical samples. $V_{DD}$ = 1.62 V

[3] Guaranteed by characterization, not tested in production. $V_{DD}$ = 2.0 V

**Table 15. Typical AHB/APB peripheral power consumption[3][4][5]**

*$V_{DD}$ = 3.3 V; T = 25 °C*

| Peripheral | | $I_{DD}$ in μA | $I_{DD}$ in μA/MHz | $I_{DD}$ in μA/MHz |
|---|---|---|---|---|
| FIFO | | - | 3.17 | 4.49 |
| **Sync APB peripheral** | | | **CPU: 12 MHz, sync APB bus: 12 MHz** | **CPU: 96MHz, sync APB bus: 96 MHz** |
| INPUTMUX | [1] | - | 0.83 | 0.96 |
| IOCON | [1] | - | 1.25 | 1.55 |
| PINT | | - | 0.83 | 1.05 |
| GINT | | - | 0.50 | 0.61 |
| WWDT | | - | 0.17 | 0.28 |
| MRT | | - | 0.50 | 0.65 |
| RTC | | - | 0.08 | 0.09 |
| RIT | | - | 0.50 | 0.71 |
| UTICK | | - | 0.17 | 0.11 |
| Timer2 | | - | 0.58 | 0.67 |
| Timer3 | | - | 0.42 | 0.42 |
| Timer4 | | - | 0.50 | 0.57 |
| **Async APB peripheral** | | | **CPU: 12 MHz, Async APB bus: 12 MHz** | **CPU: 96MHz, Async APB bus: 12 MHz[2]** |
| USART0 | | - | 0.67 | 0.11 |
| USART1 | | - | 0.75 | 0.07 |
| USART2 | | - | 0.67 | 0.11 |
| USART3 | | - | 0.75 | 0.07 |
| I2C0 | | - | 0.92 | 0.10 |
| I2C1 | | - | 0.83 | 0.26 |
| I2C2 | | - | 0.83 | 0.25 |
| SPIO0 | | - | 0.92 | 0.21 |
| SPIO1 | | - | 0.83 | 0.25 |
| CTimer0 | | - | 0.58 | 0.18 |
| CTimer1 | | - | 0.42 | 0.14 |
| Fractional Rate Generator | | - | 4.17 | 0.73 |

[1] Turn off the peripheral when the configuration is done.

[2] For optimal system power consumption, use fixed low frequency Async APB bus when the CPU is at a higher frequency.

[3] The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled using ASYNCAPBCLKCTRL, AHBCLKCTRL0/1, and PDRUNCFG register. All other blocks are disabled and no code accessing the peripheral is executed.

[4] The supply currents are shown for system clock frequencies of 12 MHz and 96 MHz.

[5] Typical ratings are not guaranteed. Characterized through bench measurements using typical samples.

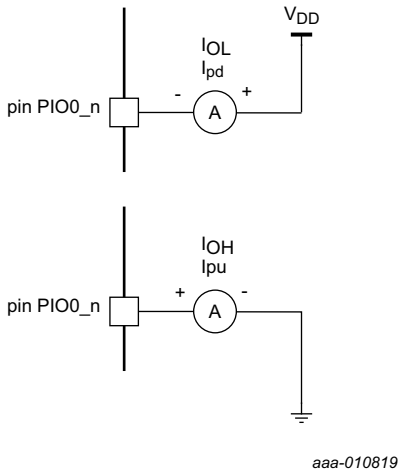
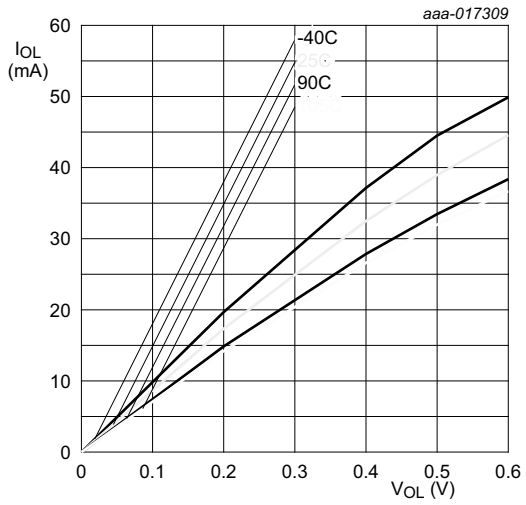
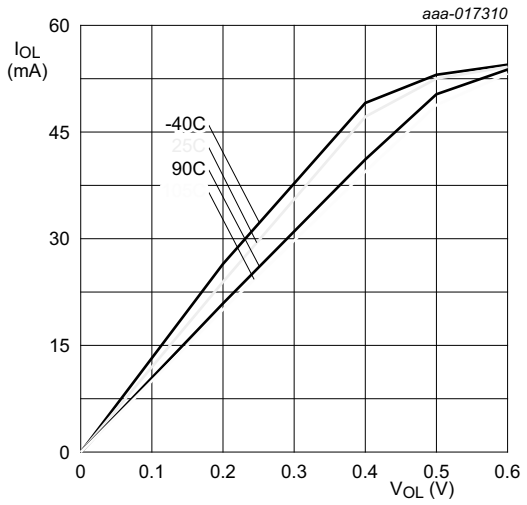



**Fig 13. Pin input/output current measurement**

### 10.4.1 Electrical pin characteristics

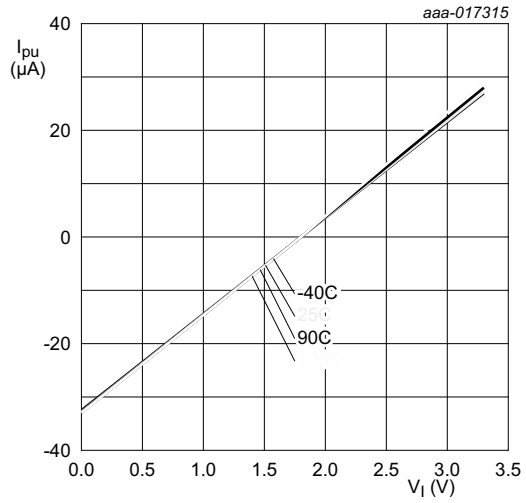



Conditions: $V_{DD}$ = 1.8 V; on pins PIO0_23 to PIO0_28.

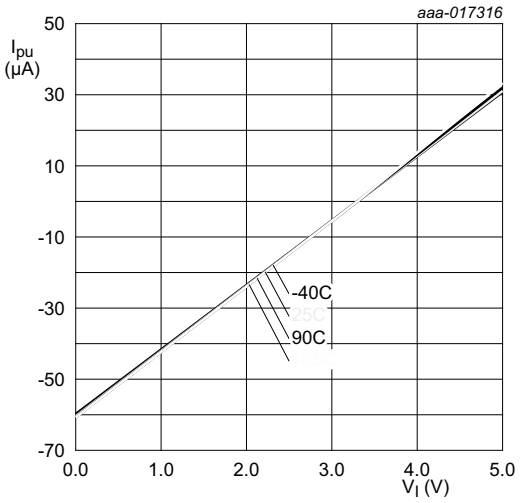



Conditions: $V_{DD}$ = 3.3 V; on pins PIO0_23 to PIO0_28.

**Fig 14. $I^2C$-bus pins (high current sink): Typical LOW-level output current $I_{OL}$ versus LOW-level output voltage $V_{OL}$**

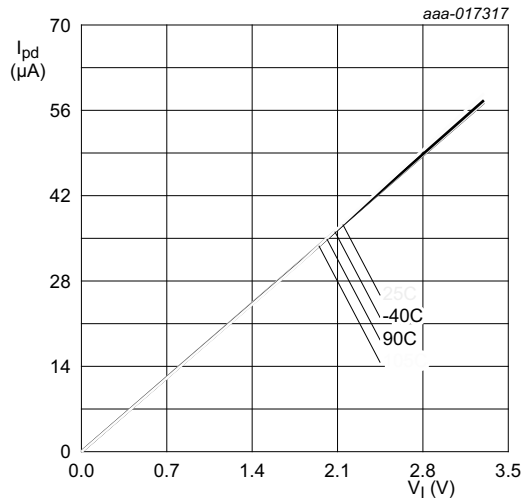



Conditions: $V_{DD}$ = 1.8 V; on standard port pins.

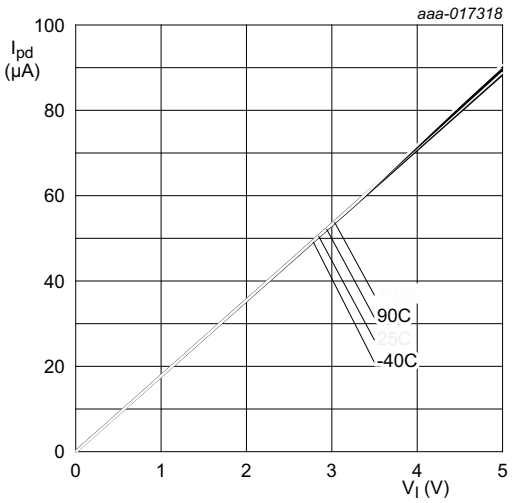



Conditions: $V_{DD}$ = 3.3 V; on standard port pins.

**Fig 17. Typical pull-up current $I_{PU}$ versus input voltage $V_I$**




Conditions: $V_{DD}$ = 1.8V; on standard port pins.




Conditions: $V_{DD}$ = 3.3 V; on standard port pins.

**Fig 18. Typical pull-down current $I_{PD}$ versus input voltage $V_I$**

[1] Number of erase/program cycles.

[2] Programming times are given for writing 256 bytes from RAM to the flash.

## 11.3 I/O pins

**Table 19. Dynamic characteristic: I/O pins[1]**
*$T_{amb}$ = −40 °C to +85 °C; 1.62 V ≤ $V_{DD}$ ≤ 3.6 V*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Standard I/O pins - normal drive strength** | | | | | | | |
| $t_r$ | rise time | pin configured as output; SLEW = 1 (fast mode); | [2][3] | | | | |
| | | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 1.0 | - | 2.5 | ns |
| | | 1.62 V ≤ $V_{DD}$ ≤ 1.98 V | | 1.6 | - | 3.8 | ns |
| $t_f$ | fall time | pin configured as output; SLEW = 1 (fast mode); | [2][3] | | | | |
| | | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 0.9 | - | 2.5 | ns |
| | | 1.62 V ≤$V_{DD}$ ≤ 1.98 V | | 1.7 | - | 4.1 | ns |
| $t_r$ | rise time | pin configured as output; SLEW = 0 (standard mode); | [2][3] | | | | |
| | | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 1.9 | - | 4.3 | ns |
| | | 1.62 V ≤ $V_{DD}$ ≤ 1.98 V | | 2.9 | - | 7.8 | ns |
| $t_f$ | fall time | pin configured as output; SLEW = 0 (standard mode); | [2][3] | | | | |
| | | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 1.9 | - | 4.0 | ns |
| | | 1.62 V ≤ $V_{DD}$ ≤ 1.98 V | | 2.7 | - | 6.7 | ns |
| $t_r$ | rise time | pin configured as input | [4] | 0.3 | - | 1.3 | ns |
| $t_f$ | fall time | pin configured as input | [4] | 0.2 | - | 1.2 | ns |

[1] Simulated data.

[2] Simulated using 10 cm of 50 Ω PCB trace with 5 pF receiver input. Rise and fall times measured between 80 % and 20 % of the full output signal level.

[3] The slew rate is configured in the IOCON block the SLEW bit. See the LPC5410x user manual.

[4] $C_L$ = 20 pF. Rise and fall times measured between 90 % and 10 % of the full input signal level.

## 11.4 Wake-up process

**Table 20. Dynamic characteristic: Typical wake-up times from low power modes**
*$V_{DD}$ = 3.3 V;$T_{amb}$ = 25 °C; using IRC as the system clock.*

| Symbol | Parameter | Conditions | | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|---|
| $t_{wake}$ | wake-up time | from sleep mode | [2][3] | - | 1.6 | - | µs |
| | | from deep sleep mode with full SRAM retention: to code executing in flash or SRAM | [2] | - | 18 | - | µs |
| | | from power down mode | [2] | | 180 | - | µs |
| | | from deep power-down mode; RTC disabled; using $\overline{\text{RESET}}$ pin. | [4] | - | 200 | - | µs |

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] The wake-up time measured is the time between when a GPIO input pin is triggered to wake the device up from the low power modes and from when a GPIO output pin is set in the interrupt service routine (ISR) wake-up handler. Measurements are based on using the power library provided in the LPC5410x LPCOpen software platform version v.3.04.

[3] IRC enabled, all peripherals off.

[4] RTC disabled. Wake-up from deep power-down causes the part to go through entire reset process. The wake-up time measured is the time between when the $\overline{\text{RESET}}$ pin is triggered to wake the device up and when a GPIO output pin is set in the reset handler.

## 11.10 SPI interfaces

The actual SPI bit rate depends on the delays introduced by the external trace, the external device, system clock (CCLK), and capacitive loading. Excluding delays introduced by external device and PCB, the maximum supported bit rate for SPI master mode is 48 Mbit/s, and the maximum supported bit rate for SPI slave mode is 21 Mbit/s.

**Table 27. SPI dynamic characteristics[1]**

*$T_{amb}$ = −40 °C to 105 °C; $C_L$ = 30 pF balanced loading on all pins; SLEW = standard mode. Parameters sampled at the 50 % level of the rising or falling edge.*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| **SPI master 1.62V ≤ VDD ≤ 2.0 V** | | | | | | |
| $t_{DS}$ | data set-up time | CCLK = 1 MHz to 12 MHz | | 0 | - | ns |
| | | CCLK = 48 MHz to 60 MHz | | 0 | - | ns |
| | | CCLK = 96 MHz | | 0 | - | ns |
| $t_{DH}$ | data hold time | CCLK = 1 MHz to 12 MHz | | 14 | - | ns |
| | | CCLK = 48 MHz to 60 MHz | | 12 | - | ns |
| | | CCLK = 96 MHz | | 9 | - | ns |
| $t_{v(Q)}$ | data output valid time | CCLK = 1 MHz to 12 MHz | | 0 | 7 | ns |
| | | CCLK = 48 MHz to 60 MHz | | 0 | 2 | ns |
| | | CCLK = 96 MHz | | 0 | 2 | ns |
| **SPI slave 1.62V ≤ VDD ≤ 2.0 V** | | | | | | |
| $t_{DS}$ | data set-up time | CCLK = 1 MHz to 12 MHz | | 22 | - | ns |
| | | CCLK = 48 MHz to 60 MHz | | 4 | - | ns |
| | | CCLK = 96 MHz | | 4 | - | ns |
| $t_{DH}$ | data hold time | CCLK = 1 MHz to 12 MHz | | 0 | - | ns |
| | | CCLK = 48 MHz to 60 MHz | | 0 | - | ns |
| | | CCLK = 96 MHz | | 0 | - | ns |
| $t_{v(Q)}$ | data output valid time | CCLK = 1 MHz to 12 MHz | | 46 | 70 | ns |
| | | CCLK = 48 MHz to 60 MHz | | 30 | 37 | ns |
| | | CCLK = 96 MHz | | 30 | 36 | ns |
| **SPI master 2.7 V ≤ VDD ≤ 3.6 V** | | | | | | |
| $t_{DS}$ | data set-up time | CCLK = 1 MHz to 12 MHz | | 0 | - | ns |
| | | CCLK = 48 MHz to 60 MHz | | 0 | - | ns |
| | | CCLK = 96 MHz | | 0 | - | ns |
| $t_{DH}$ | data hold time | CCLK = 1 MHz to 12 MHz | | 10 | - | ns |
| | | CCLK = 48 MHz to 60 MHz | | 8 | - | ns |
| | | CCLK = 96 MHz | | 7 | - | ns |
| $t_{v(Q)}$ | data output valid time | CCLK = 1 MHz to 12 MHz | | 0 | 6 | ns |
| | | CCLK = 48 MHz to 60 MHz | | 0 | 1 | ns |
| | | CCLK = 96 MHz | | 0 | 1 | ns |
| **SPI slave 2.7V ≤ VDD ≤ 3.6 V** | | | | | | |
| $t_{DS}$ | data set-up time | CCLK = 1 MHz to 12 MHz | | 21 | - | ns |
| | | CCLK = 48 MHz to 60 MHz | | 4 | - | ns |
| | | CCLK = 96 MHz | | 3 | - | ns |

## 11.11 USART interface

The actual USART bit rate depends on the delays introduced by the external trace, the external device, system clock (CCLK), and capacitive loading. Excluding delays introduced by external device and PCB, the maximum supported bit rate for USART master and slave synchronous modes is 24 Mbit/s.

**Table 28. USART dynamic characteristics[1]**

*$T_{amb}$ = −40 °C to 105 °C; 1.62 V ≤ $V_{DD}$ ≤ 3.6 V; $C_L$ = 30 pF balanced loading on all pins; SLEW = standard mode. Parameters sampled at the 50% level of the falling or rising edge.*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| **USART master (in synchronous mode) 1.62V ≤ VDD ≤ 2.0 V** | | | | | |
| $t_{su(D)}$ | data input set-up time | CCLK = 1 MHz to 12 MHz | 65 | - | ns |
| | | CCLK = 48 MHz to 60 MHz | 35 | - | ns |
| | | CCLK = 96 MHz | 34 | - | ns |
| $t_{h(D)}$ | data input hold time | CCLK = 1 MHz to 12 MHz | 0 | - | ns |
| | | CCLK = 48 MHz to 60 MHz | 0 | - | ns |
| | | CCLK = 96 MHz | 0 | - | ns |
| $t_{v(Q)}$ | data output valid time | CCLK = 1 MHz to 12 MHz | 0 | 8 | ns |
| | | CCLK = 48 MHz to 60 MHz | 0 | 2 | ns |
| | | CCLK = 96 MHz | 0 | 2 | ns |
| **USART slave (in synchronous mode) 1.62V ≤ VDD ≤ 2.0 V** | | | | | |
| $t_{su(D)}$ | data input set-up time | CCLK = 1 MHz to 12 MHz | 18 | - | ns |
| | | CCLK = 48 MHz to 60 MHz | 5 | - | ns |
| | | CCLK = 96 MHz | 4 | - | ns |
| $t_{h(D)}$ | data input hold time | CCLK = 1 MHz to 12 MHz | 0 | - | ns |
| | | CCLK = 48 MHz to 60 MHz | 0 | - | ns |
| | | CCLK = 96 MHz | 0 | - | ns |
| $t_{v(Q)}$ | data output valid time | CCLK = 1 MHz to 12 MHz | 50 | 65 | ns |
| | | CCLK = 48 MHz to 60 MHz | 35 | 40 | ns |
| | | CCLK = 96 MHz | 30 | 36 | ns |
| **USART master (in synchronous mode) 2.7V ≤ VDD ≤ 3.6V** | | | | | |
| $t_{su(D)}$ | data input set-up time | CCLK = 1 MHz to 12 MHz | 61 | - | ns |
| | | CCLK = 48 MHz to 60 MHz | 22 | - | ns |
| | | CCLK = 96 MHz | 21 | - | ns |
| $t_{h(D)}$ | data input hold time | CCLK = 1 MHz to 12 MHz | 0 | - | ns |
| | | CCLK = 48 MHz to 60 MHz | 0 | - | ns |
| | | CCLK = 96 MHz | 0 | - | ns |
| $t_{v(Q)}$ | data output valid time | CCLK = 1 MHz to 12 MHz | 0 | 7 | ns |
| | | CCLK = 48 MHz to 60 MHz | 1 | 2 | ns |
| | | CCLK = 96 MHz | 1 | 2 | ns |

# 12. Analog characteristics

## 12.1 BOD

**Table 30. BOD static characteristics**

*$T_{amb}$ = 25 °C; based on characterization; not tested in production.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{th}$ | threshold voltage | interrupt level 0 | | | | | |
| | | assertion | | - | 2.05 | - | V |
| | | de-assertion | | - | 2.20 | - | V |
| $V_{th}$ | threshold voltage | interrupt level 1 | | | | | |
| | | assertion | | - | 2.45 | - | V |
| | | de-assertion | | - | 2.60 | - | V |
| | | reset level 1 | | | | | |
| | | assertion | | - | 1.85 | - | V |
| | | de-assertion | | - | 2.00 | - | V |
| $V_{th}$ | threshold voltage | interrupt level 2 | | | | | |
| | | assertion | | - | 2.75 | - | V |
| | | de-assertion | | - | 2.90 | - | V |
| | | reset level 2 | | | | | |
| | | assertion | | - | 2.00 | - | V |
| | | de-assertion | | - | 2.15 | - | V |
| $V_{th}$ | threshold voltage | interrupt level 3 | | | | | |
| | | assertion | | - | 3.05 | - | V |
| | | de-assertion | | - | 3.20 | - | V |
| | | reset level 3 | | | | | |
| | | assertion | | - | 2.30 | - | V |
| | | de-assertion | | - | 2.45 | - | V |

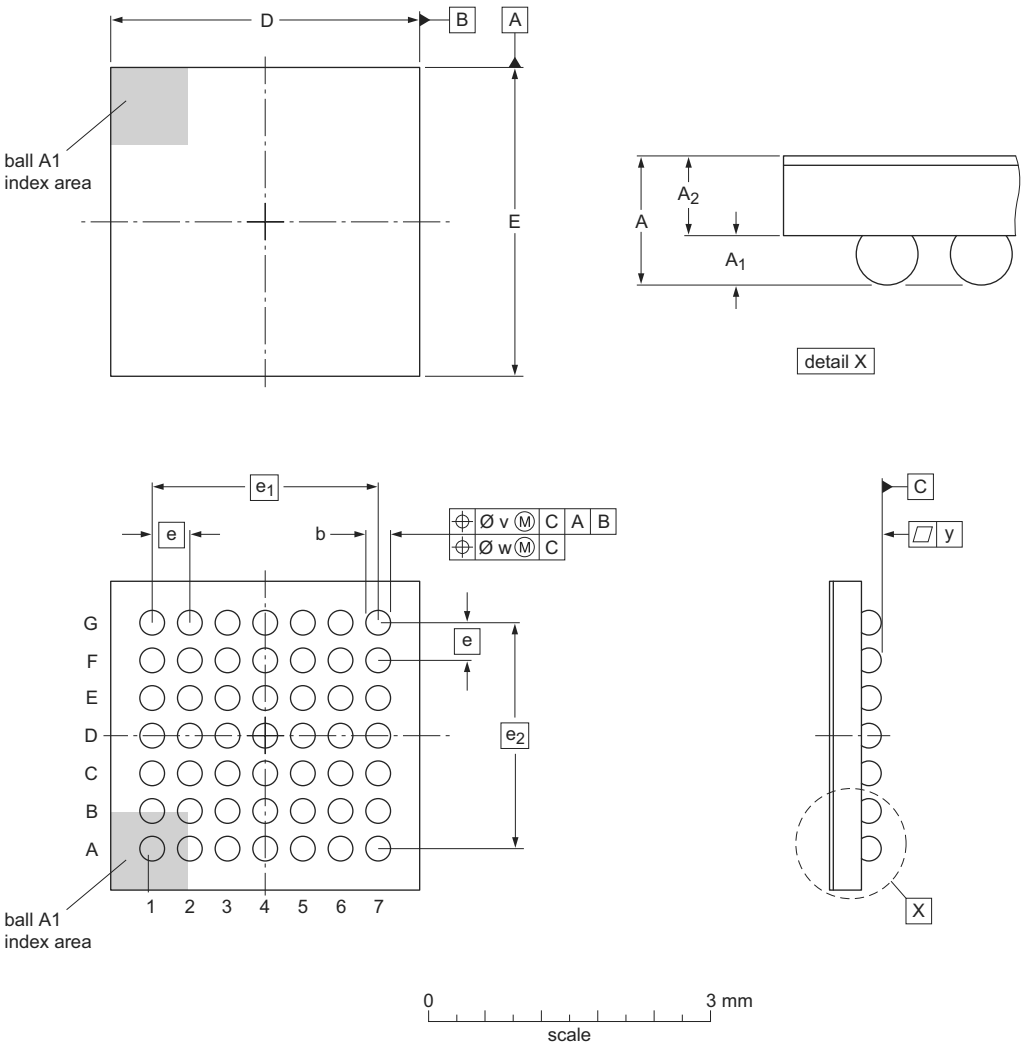
**Table 32. ADC sampling times[1]**

*-40 °C ≤ $T_{amb}$ ≤ 85 °C; 1.62 V ≤ $V_{DDA}$ ≤ 3.6 V; 1.62 V ≤ $V_{DD}$ ≤ 3.6 V*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **ADC inputs ADC_5 to ADC_0 (fast channels); ADC resolution = 12 bit** | | | | | | | |
| $t_s$ | sampling time | $Z_o$ < 0.05 kΩ | [3] | 20 | - | - | ns |
| | | 0.05 kΩ ≤ $Z_o$ < 0.1 kΩ | | 23 | - | - | ns |
| | | 0.1 kΩ ≤ $Z_o$ < 0.2 kΩ | | 26 | - | - | ns |
| | | 0.2 kΩ ≤ $Z_o$ < 0.5 kΩ | | 31 | - | - | ns |
| | | 0.5 kΩ ≤ $Z_o$ < 1 kΩ | | 47 | - | - | ns |
| | | 1 kΩ ≤ $Z_o$ < 5 kΩ | | 75 | - | - | ns |
| **ADC inputs ADC_5 to ADC_0 (fast channels); ADC resolution = 10 bit** | | | | | | | |
| $t_s$ | sampling time | $Z_o$ < 0.05 kΩ | [3] | 15 | - | - | ns |
| | | 0.05 kΩ ≤ $Z_o$ < 0.1 kΩ | | 18 | - | - | ns |
| | | 0.1 kΩ ≤ $Z_o$ < 0.2 kΩ | | 20 | - | - | ns |
| | | 0.2 kΩ ≤ $Z_o$ < 0.5 kΩ | | 24 | - | - | ns |
| | | 0.5 kΩ ≤ $Z_o$ < 1 kΩ | | 38 | - | - | ns |
| | | 1 kΩ ≤ $Z_o$ < 5 kΩ | | 62 | - | - | ns |
| **ADC inputs ADC_5 to ADC_0 (fast channels); ADC resolution = 8 bit** | | | | | | | |
| $t_s$ | sampling time | $Z_o$ < 0.05 kΩ | [3] | 12 | - | - | ns |
| | | 0.05 kΩ ≤ $Z_o$ < 0.1 kΩ | | 13 | - | - | ns |
| | | 0.1 kΩ ≤ $Z_o$ < 0.2 kΩ | | 15 | - | - | ns |
| | | 0.2 kΩ ≤ $Z_o$ < 0.5 kΩ | | 19 | - | - | ns |
| | | 0.5 kΩ ≤ $Z_o$ < 1 kΩ | | 30 | - | - | ns |
| | | 1 kΩ ≤ $Z_o$ < 5 kΩ | | 48 | - | - | ns |
| **ADC inputs ADC_5 to ADC_0 (fast channels); ADC resolution = 6 bit** | | | | | | | |
| $t_s$ | sampling time | $Z_o$ < 0.05 kΩ | [3] | 9 | - | - | ns |
| | | 0.05 kΩ ≤ $Z_o$ < 0.1 kΩ | | 10 | - | - | ns |
| | | 0.1 kΩ ≤ $Z_o$ < 0.2 kΩ | | 11 | - | - | ns |
| | | 0.2 kΩ ≤ $Z_o$ < 0.5 kΩ | | 13 | - | - | ns |
| | | 0.5 kΩ ≤ $Z_o$ < 1 kΩ | | 22 | - | - | ns |
| | | 1 kΩ ≤ $Z_o$ < 5 kΩ | | 36 | - | - | ns |
| **ADC inputs ADC_11 to ADC_6 (slow channels); ADC resolution = 12 bit** | | | | | | | |
| $t_s$ | sampling time | $Z_o$ < 0.05 kΩ | [3] | 43 | - | - | ns |
| | | 0.05 kΩ ≤ $Z_o$ < 0.1 kΩ | | 46 | - | - | ns |
| | | 0.1 kΩ ≤ $Z_o$ < 0.2 kΩ | | 50 | - | - | ns |
| | | 0.2 kΩ ≤ $Z_o$ < 0.5 kΩ | | 56 | - | - | ns |
| | | 0.5 kΩ ≤ $Z_o$ < 1 kΩ | | 74 | - | - | ns |
| | | 1 kΩ ≤ $Z_o$ < 5 kΩ | | 105 | - | - | ns |

# 14. Package outline

**WLCSP49: wafer level chip-scale package; 49 bumps; 3.29 x 3.29 x 0.54 mm (backside coating included)** **LPC5410**




Dimensions (mm are the original dimensions)

| Unit | | A | $A_1$ | $A_2$ | b | D | E | e | $e_1$ | $e_2$ | v | w | y |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | max | 0.58 | 0.23 | 0.37 | 0.29 | 3.318 | 3.318 | 0.4 | 2.4 | 2.4 | 0.05 | 0.015 | 0.03 |
| | nom | 0.54 | 0.20 | 0.34 | 0.26 | 3.288 | 3.288 | | | | | | |
| | min | 0.50 | 0.17 | 0.31 | 0.23 | 3.258 | 3.258 | | | | | | |

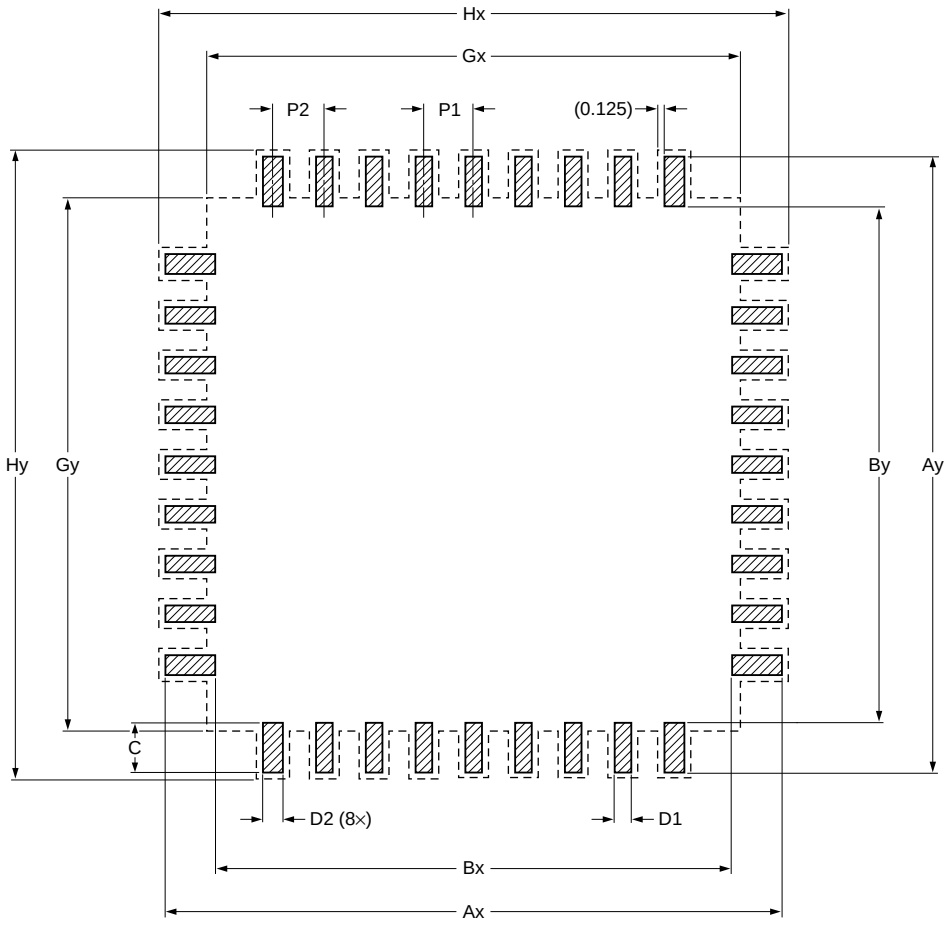
Note
Backside coating 40 µm

*wlcsp49_lpc5410_po*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| LPC5410 | | - - - | | | | ~~13-09-16~~ 14-11-03 |

**Fig 30. WLCSP49 Package outline**

**Footprint information for reflow soldering of LQFP64 package** **SOT314-2**




Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

| P1 | P2 | Ax | Ay | Bx | By | C | D1 | D2 | Gx | Gy | Hx | Hy |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0.500 | 0.560 | 13.300 | 13.300 | 10.300 | 10.300 | 1.500 | 0.280 | 0.400 | 10.500 | 10.500 | 13.550 | 13.550 |

*sot314-2_fr*

**Fig 33. LQFP64 Soldering footprint**

# 16. Abbreviations

**Table 35. Abbreviations**

| Acronym | Description |
|---|---|
| AHB | Advanced High-performance Bus |
| APB | Advanced Peripheral Bus |
| API | Application Programming Interface |
| DMA | Direct Memory Access |
| GPIO | General Purpose Input/Output |
| IRC | Internal RC |
| LSB | Least Significant Bit |
| MCU | MicroController Unit |
| PLL | Phase-Locked Loop |
| SPI | Serial Peripheral Interface |
| TTL | Transistor-Transistor Logic |
| USART | Universal Asynchronous Receiver/Transmitter |

# 17. References

[1] LPC5410x User manual UM10850:
http://www.nxp.com/documents/user_manual/UM10850.pdf

[2] LPC5410x Errata sheet:
http://www.nxp.com/documents/errata_sheet/ES_LPC5410X.pdf

[3] Technical note ADC design guidelines:
http://www.nxp.com/documents/technical_note/TN00009.pdf

**Table 36. Revision history** *…continued*

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| Modification: | • Updated Table 18 “Flash characteristics”: For $N_{endu}$ conditions, removed the row with page erase/program; page in small sector 10000 and removed the word large so that it is "page erase/program;page in a sector".<br>• Updated Section 7.16.1 “USART” features: changed maximum bit rates to 6.25 Mbit/s in asynchronous mode. | | | |
| LPC5410x v2.2 | 20151222 | Product data sheet | 201512007I | LPC5410x v2.1 |
| Modification: | • Updated Section 11.6 “IRC”, Table 23 “Dynamic characteristic: IRC oscillator” for IRC frequency tolerance improvement over temperature.<br>• Added boot code version and device revision. See Section 4 “Marking”.<br>• Added the abbreviation ISP to the Remark: This pin is also used to force In-System Programming mode (ISP) after device reset. See the LPC5410x User Manual (Boot Process chapter) for details to PIO0_31. See Table 4 “Pin description”.<br>• Removed 164 uA PLL spec in peripheral power consumption table, Table 15 “Typical AHB/APB peripheral power consumption[3][4][5]”.<br>• Added Table 21 “PLL lock times and current”.<br>• Updated Figure 10 “Deep sleep mode: Typical supply current IDD versus temperature for different supply voltages VDD”, Figure 11 “Power down mode: Typical supply current IDD versus temperature for different supply voltages VDD”, and Figure 12 “Deep power-down mode: Typical supply current IDD versus temperature for different supply voltages VDD”.<br>• Updated Table 12 “Static characteristics: Power consumption in deep sleep, power down, and deep power-down modes”: added max values to Deep sleep mode at 25 °C and 105 °C, Power down mode at 25 °C and 105 °C. Changed typ and max values for Deep power-down mode RTC oscillator input grounded (RTC oscillator disabled) at 25 °C; was: typ = 84 nA, max = 240 nA; now: typ = 160 nA, max = 340 nA.<br>• Updated Table 13 “Static characteristics: Power consumption in deep sleep, power down, and deep power-down modes”: added max values to Deep sleep mode at 25 °C and 105 °C, Power down mode at 25 °C and 105 °C. Changed typ and max values for Deep power-down mode RTC oscillator input grounded (RTC oscillator disabled) at 25 °C; was: typ = 135 nA, max = 470 nA; now: typ = 200 nA, max = 570 nA.<br>• Updated Table 7 “Limiting values”; VESD, electrostatic discharge voltage, human body model; all pins value to 4000 V; was 5000 V.<br>• Updated Table 31 “12-bit ADC static characteristics”: ED differential linearity error, VDDA = VREFP = 1.62 V and 3.6 V, typ value ±3 and ±2; $EL_{(adj)}$ integral non-linearity, VDDA = VREFP = 1.62 V, typ value ±5; $V_{err(FS)}$ full-scale error voltage VDDA = VREFP = 1.62 V and 3.6 V, typ value to ±3 | | | |
| LPC5410x v2.1 | 20150701 | Product data sheet | - | LPC5410x v2.0 |
| Modification: | • Updated Figure 3 “LPC5410x Block diagram”. Corrected Sync APB bridge to Async APB bridge.<br>• Updated external clock input for clock frequencies of up to 24 MHz to 25 MHz in Section 2 “Features and benefits”.<br>• Updated Table 12 “Static characteristics: Power consumption in deep sleep, power down, and deep power-down modes”. Fixed the unit of the max value from nA to μA for IDD in deep power-down mode; RTC oscillator input grounded (RTC oscillator disabled), $T_{amb}$ = 105 °C. | | | |