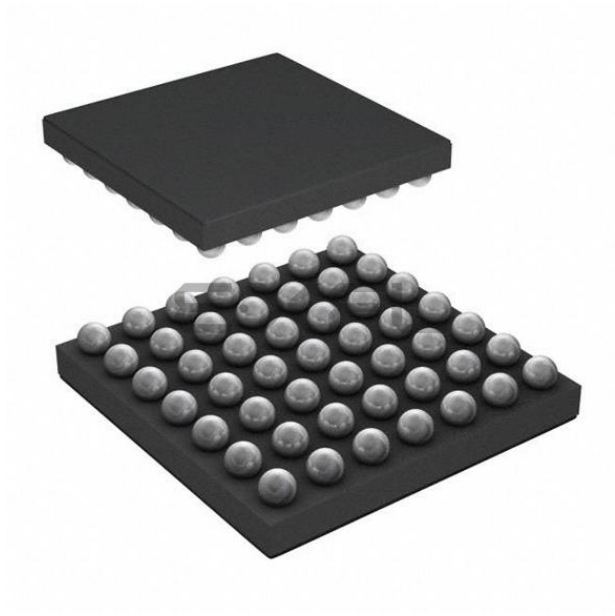

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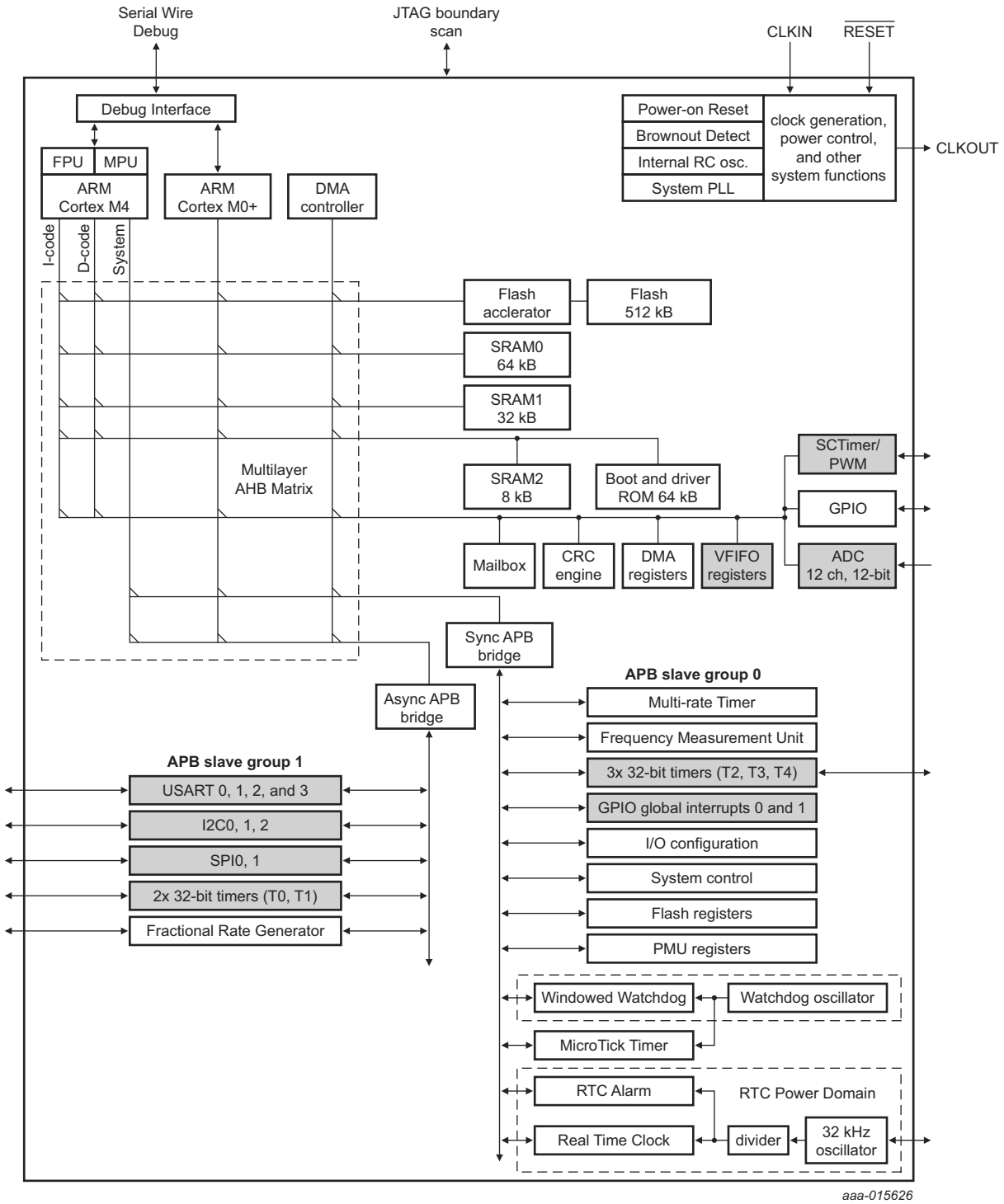
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4/M0+
Core Size	32-Bit Dual-Core
Speed	100MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	39
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	104K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	49-UFBGA, WLCSP
Supplier Device Package	49-WLCSP (3.29x3.29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc54102j256uk49z

- ARM Cortex-M0+ core (version r0p1):
  - ARM Cortex-M0+ processor, running at a frequency of up to 100 MHz.
  - ARM Cortex-M0+ built-in Nested Vectored Interrupt Controller (NVIC).
  - Non-maskable Interrupt (NMI) input with a selection of sources.
  - Serial Wire Debug with four breakpoints and two watch points.
  - System tick timer.
- On-chip memory:
  - Up to 512 kB on-chip flash program memory with flash accelerator and 256 byte page erase and write.
  - 104 kB total SRAM composed of:
  - Up to 96 kB contiguous main SRAM.
  - An additional 8 kB SRAM.
- ROM API support:
  - Flash In-Application Programming (IAP) and In-System Programming (ISP).
  - Power control API.
- Serial interfaces:
  - Four USART interfaces with synchronous mode and 32 kHz mode for wake-up from deep sleep and power down modes. The USARTs have FIFO support from the System FIFO and share a fractional baud-rate generator.
  - Two SPI interfaces, each with four slave selects and flexible data configuration. The SPIs have FIFO support from the System FIFO. The slave function is able to wake up the device from deep sleep and power down modes.
  - Three I^2C-bus interfaces supporting fast mode and Fast-mode Plus with data rates of up to 1Mbit/s and with multiple address recognition and monitor mode. Each I^2C-bus interface also supports High Speed Mode (3.4 Mbit/s) as a slave. The slave function is able to wake up the device from deep sleep and power down modes.
- Digital peripherals:
  - DMA controller with 22 channels and 20 programmable triggers, able to access all memories and DMA-capable peripherals.
  - Up to 50 General-Purpose Input/Output (GPIO) pins. Most GPIOs have configurable pull-up/pull-down resistors, programmable open-drain mode, and input inverter.
  - GPIO registers are located on the AHB for fast access. The DMA supports GPIO ports.
  - Up to eight GPIOs (pin interrupts) can be selected as edge-sensitive (rising or falling edges or both) interrupt requests or level-sensitive (active low or active high) interrupt requests. In addition, up to eight GPIOs can be selected to contribute a boolean expression and interrupt generation using the pattern match engine block.
  - Two GPIO grouped interrupts (GINT) enable an interrupt based on a logical (AND/OR) combination of input states.
  - CRC engine.
- Timers:
  - Five 32-bit standard general purpose timers/counters, four of which support up to 4 capture inputs and 4 compare outputs, PWM mode, and external count input. Specific timer events can be selected to generate DMA requests. The fifth timer does not have external pin connections and may be used for internal timing operations.

5. Block diagram



Gray-shaded peripheral blocks provide dedicated request lines or triggers for DMA transfers.

Fig 3. LPC5410x Block diagram

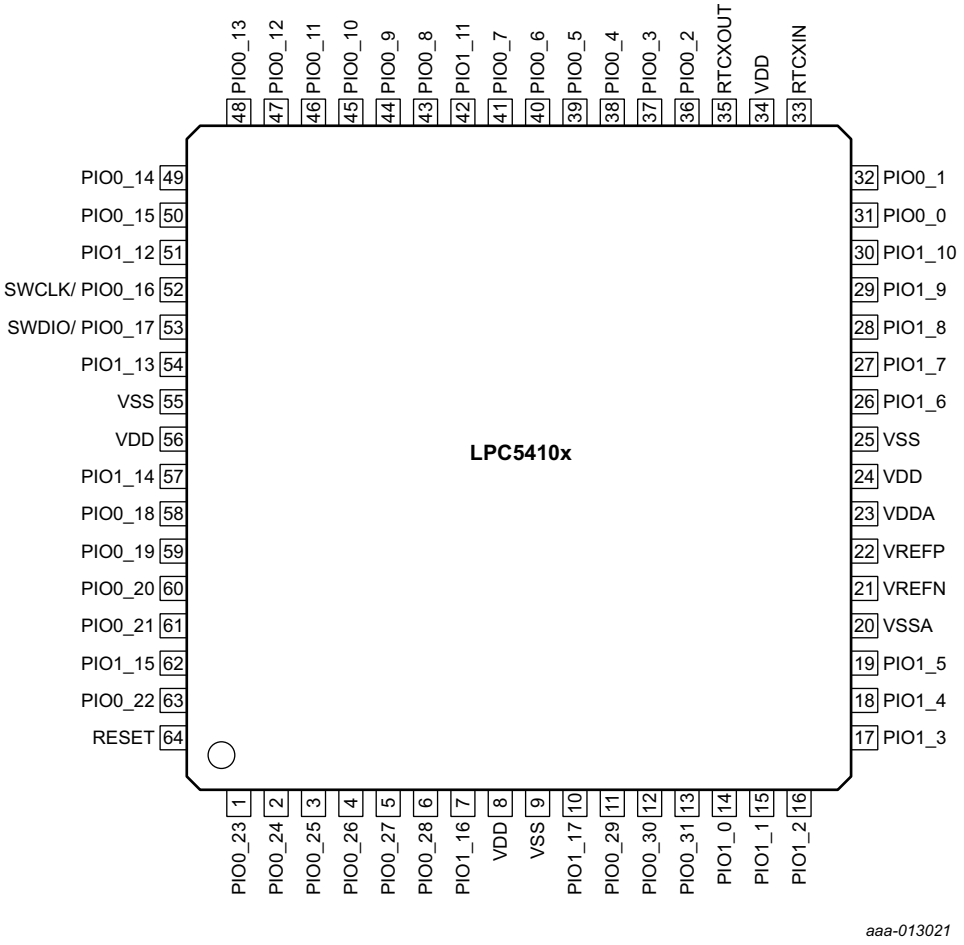


Fig 5. LQFP64 Pin configuration

Table 4. Pin description *…continued*

Symbol	WLCSP49	LQFP64		Reset state [1]	Type [6]	Description
PIO0_12	F7	47	[2]	PU	I/O	**PIO0_12 —** General-purpose digital input/output pin.
					I/O	**SPI0_MOSI —** Master Out Slave in for SPI0.
					O	**U1_TXD —** Transmitter output for USART1.
					O	**CT32B2_MAT3 —** 32-bit CT32B2 match output 3.
					I	**R —** Reserved.
PIO0_13	G7	48	[2]	PU	I/O	**PIO0_13 —** General-purpose digital input/output pin.
					I/O	**SPI0_MISO —** Master In Slave Out for SPI0.
					O	**SCT0_OUT4 —** SCT0 output 4. PWM output 4.
					O	**CT32B2_MAT0 —** 32-bit CT32B2 match output 0.
					I	**R —** Reserved.
PIO0_14/TCK	F6	49	[2]	PU	I/O	**PIO0_14 —** General-purpose digital input/output pin. In boundary scan mode: TCK (Test Clock).
					I/O	**SPI0_SSEL0 —** Slave Select 0 for SPI0.
					O	**SCT0_OUT5 —** SCT0 output 5. PWM output 5.
					O	**CT32B2_MAT1 —** 32-bit CT32B2 match output 1.
					I	**R —** Reserved.
PIO0_15/TDO	G6	50	[2]	PU	I/O	**PIO0_15 —** General-purpose digital input/output pin. In boundary scan mode: TDO (Test Data Out).
					I/O	**SPI0_SSEL1 —** Slave Select 1 for SPI0.
					I/O	**SWO —** Serial wire trace output.
					O	**CT32B2_MAT2 —** 32-bit CT32B2 match output 2.
					I	**R —** Reserved.
SWCLK/ PIO0_16	F5	52	[2]	PU	I/O	**PIO0_16 —** General-purpose digital input/output pin. After booting, this pin is connected to the SWCLK.
					I/O	**SPI0_SSEL2 —** Slave Select 2 for SPI0.
					I	**$\overline{\text{U1\_CTS}}$ —** Clear To Send input for USART1.
					O	**CT32B3_MAT1 —** 32-bit CT32B3 match output 1.
					I	**R —** Reserved.
					I/O	**SWCLK —** Serial Wire Clock. This is the default function after booting.
SWDIO/ PIO0_17	G5	53	[2]	PU	I/O	**PIO0_17 —** General-purpose digital input/output pin. After booting, this pin is connected to SWDIO.
					I/O	**SPI0_SSEL3 —** Slave Select 3 for SPI0.
					O	**$\overline{\text{U1\_RTS}}$ —** Request To Send output for USART1.
					O	**CT32B3_MAT2 —** 32-bit CT32B3 match output 2.
					I	**R —** Reserved.
					I/O	**SWDIO —** Serial Wire Debug I/O. This is the default function after booting.

Table 4. Pin description *…continued*

Symbol	WLCSP49	LQFP64		Reset state [1]	Type [6]	Description
PIO0_24	F1	2	[3]	Z	I/O	**PIO0_24 —** General-purpose digital input/output pin.
					I/O	**I2C0_SDA —** I^2C0 data input/output.
					I	**R —** Reserved.
					I	**CT32B0_CAP1 —** 32-bit CT32B0 capture input 1.
					I	**R —** Reserved.
					O	**CT32B0_MAT0 —** 32-bit CT32B0 match output 0.
PIO0_25	E2	3	[3]	Z	I/O	**PIO0_25 —** General-purpose digital input/output pin.
					I/O	**I2C1_SCL —** I^2C1 clock input/output.
					I	**$\overline{\text{U1\_CTS}}$ —** Clear To Send input for USART1.
					I	**CT32B0_CAP2 —** 32-bit CT32B0 capture input 2.
					I	**R —** Reserved.
					I	**CT32B1_CAP1 —** 32-bit CT32B1 capture input 1.
PIO0_26	E1	4	[3]	Z	I/O	**PIO0_26 —** General-purpose digital input/output pin.
					I/O	**I2C1_SDA —** I^2C1 data input/output.
					I	**R —** Reserved.
					I	**CT32B0_CAP3 —** 32-bit CT32B0 capture input 3.
					I	**R —** Reserved.
PIO0_27	D2	5	[3]	Z	I/O	**PIO0_27 —** General-purpose digital input/output pin.
					I/O	**I2C2_SCL —** I^2C2 clock input/output.
					I	**R —** Reserved.
					I	**CT32B2_CAP0 —** 32-bit CT32B2 capture input 0.
					I	**R —** Reserved.
PIO0_28	D1	6	[3]	Z	I/O	**PIO0_28 —** General-purpose digital input/output pin.
					I/O	**I2C2_SDA —** I^2C2 data input/output.
					I	**R —** Reserved.
					O	**CT32B2_MAT0 —** 32-bit CT32B2 match output 0.
					I	**R —** Reserved.
PIO0_29/ ADC0_0	D3	11	[4]	PU	I/O; AI	**PIO0_29/ADC0_0 —** General-purpose digital input/output pin (default). ADC input channel 0 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					O	**SCT0_OUT2 —** SCT0 output 2.
					O	**CT32B0_MAT3 —** 32-bit CT32B0 match output 3.
					I	**R —** Reserved.
					I	**CT32B0_CAP1 —** 32-bit CT32B0 capture input 1.
					O	**CT32B0_MAT1 —** 32-bit CT32B0 match output 1.

Table 4. Pin description *…continued*

Symbol	WLCSP49	LQFP64		Reset state [1]	Type [6]	Description
PIO0_30/ ADC0_1	C1	12	[4]	PU	I/O; AI	**PIO0_30/ADC0_1 —** General-purpose digital input/output pin (default). ADC input channel 1 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					O	**SCT0_OUT3 —** SCT0 output 3.
					O	**CT32B0_MAT2 —** 32-bit CT32B0 match output 2.
					I	**R —** Reserved.
					I	**CT32B0_CAP2 —** 32-bit CT32B0 capture input 2.
PIO0_31/ ADC0_2	C2	13	[4]	PU	I/O; AI	**PIO0_31/ADC0_2 —** General-purpose digital input/output pin (default). ADC input channel 2 if the DIGIMODE bit is set to 0 in the IOCON register for this pin. **Remark:** This pin is also used to force In-System Programming mode (ISP) after device reset. See the LPC5410x User Manual (Boot Process chapter) for details.
					-	**R —** Reserved.
					I	**$\overline{\text{U2\_CTS}}$ —** Clear To Send input for USART2.
					I	**CT32B2_CAP2 —** 32-bit CT32B2 capture input 2.
					I	**R —** Reserved.
					I	**CT32B0_CAP3 —** 32-bit CT32B0 capture input 3.
					O	**CT32B0_MAT3 —** 32-bit CT32B0 match output 3.
PIO1_0/ ADC0_3	C3	14	[4]	PU	I/O; AI	**PIO1_0/ADC0_3 —** General-purpose digital input/output pin (default). ADC input channel 3 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					O	**$\overline{\text{U2\_RTS}}$ —** Request To Send output for USART2.
					O	**CT32B3_MAT1 —** 32-bit CT32B3 match output 1.
					I	**R —** Reserved.
					I	**CT32B0_CAP0 —** 32-bit CT32B0 capture input 0.
PIO1_1/ ADC0_4	B1	15	[4]	PU	I/O; AI	**PIO1_1/ADC0_4 —** General-purpose digital input/output pin (default). ADC input channel 4 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					I/O	**SWO —** Serial wire trace output.
					O	**SCT0_OUT4 —** SCT0 output 4.
PIO1_2/ ADC0_5	A1	16	[4]	PU	I/O; AI	**PIO1_2/ADC0_5 —** General-purpose digital input/output pin (default). ADC input channel 5 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					I/O	**SPI1_SSEL3 —** Slave Select 3 for SPI1.
					O	**SCT0_OUT5 —** SCT0 output 5.

[4] 5 V tolerant pin providing standard digital I/O functions with configurable modes, configurable hysteresis, and analog input. When configured as an analog input, the digital section of the pin is disabled, and the pin is not 5 V tolerant.

[5] Reset pad.5 V tolerant pad with glitch filter with hysteresis. Pulse width of spikes or glitches suppressed by input filter is from 3 ns to 20 ns (simulated value)

[6] I = Input; AI = Analog input; O = Output

- Burst conversion mode for single or multiple inputs.
- Synchronous or asynchronous operation. Asynchronous operation maximizes flexibility in choosing the ADC clock frequency, Synchronous mode minimizes trigger latency and can eliminate uncertainty and jitter in response to a trigger.

7.20 System control

7.20.1 Clock sources

The LPC5410x supports two external and three internal clock sources:

- The Internal RC (IRC).
- Watchdog oscillator (WDOSC).
- External clock source from the digital I/O pin CLKIN.
- External RTC 32 KHz clock.
- Output of the system PLL.

7.20.1.1 Internal RC oscillator (IRC)

The IRC can be used as the clock that drives the system PLL and subsequently the CPU. The nominal IRC frequency is 12 MHz.

Upon power-up or any chip reset, the LPC5410x uses the IRC as the clock source. Software may later switch to one of the other available clock sources.

7.20.1.2 Watchdog oscillator (WDOSC)

The watchdog oscillator is a low-power internal oscillator. The WDOSC can be used to provide a clock to the WWDT and to the entire chip. The nominal output frequency is 500 kHz.

7.20.1.3 Clock input pin (CLKIN)

An external square-wave clock source (up to 25 MHz) can be supplied on the digital I/O pin CLKIN.

7.20.2 System PLL

The system PLL accepts an input clock frequency in the range of 32 kHz to 12 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO).

The PLL can be enabled or disabled by software.

7.20.4.1 Sleep mode

When sleep mode is entered, the clock to the core is stopped along with any unused peripherals. Waking up from the sleep mode does not need any special sequence other than re-enabling the clock to the ARM core.

In sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, internal buses, and unused peripherals. The processor state and registers, peripheral registers, and internal SRAM values are maintained, and the logic levels of the pins remain static.

7.20.4.2 Deep sleep mode

In deep sleep mode, all peripheral clocks and all clock sources are off with the option of keeping the 32 kHz clock and the WDOSC running. In addition, all analog blocks are shut down and the flash is put in stand-by mode. In deep sleep mode, the application can keep some of the internal clocks and the BOD circuit running for self-timed wake-up and BOD protection.

The LPC5410x can wake up from deep sleep mode via a reset, digital pins selected as inputs to the pin interrupt block, RTC alarm, Micro-tick, a watchdog timer reset interrupt, BOD interrupt/reset, or an interrupt from the USART (in 32 kHz mode or synchronous slave mode), the SPI, or any of the I2C peripherals. For wake-up from deep sleep mode, the SPI, USART, and I2C peripherals must be configured in slave mode.

Any interrupt used for waking up from deep sleep mode must be enabled in one of the SYSCON wake-up enable registers and the NVIC.

In deep sleep mode, the processor state and registers, peripheral registers, and internal SRAM values are maintained, and the logic levels of the pins remain static. deep sleep mode allows for very low quiescent power and fast wake-up options.

7.20.4.3 Power down mode

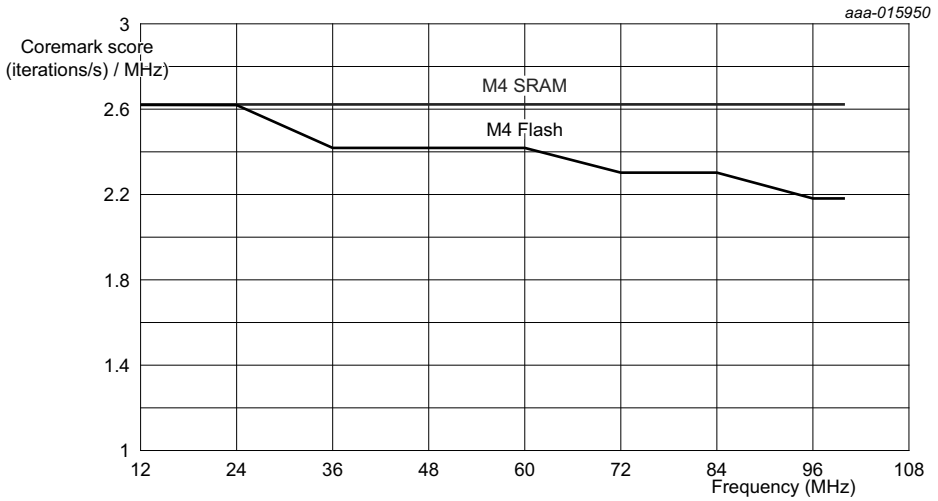
In power down mode, all peripheral clocks and all clock sources are off with the option of keeping the 32 kHz clock, and the WDOSC running. In addition, all analog blocks and the flash are shut down. In power down mode, the application can keep the BOD circuit running for BOD protection.

The LPC5410x can wake up from power down mode via a reset, digital pins selected as inputs to the pin interrupt block, RTC alarm, Micro-tick, a watchdog timer reset interrupt, BOD interrupt/reset, or an interrupt from the USART (in 32 kHz mode or synchronous slave mode), the SPI, or any of the I2C peripherals. For wake-up from power down mode, the SPI, USART, and I2C peripherals must be configured in slave mode.

In power down mode, the processor state and registers, peripheral registers, and internal SRAM values are maintained, and the logic levels of the pins remain static. Power down mode reduces power consumption compared to deep sleep mode at the expense of longer wake-up times.

[5] SRAM0 and SRAM1 powered, SRAM2 powered down.

[6] See the FLASHCFG register in the LPC5410x User Manual for system clock flash access time settings.



Conditions: V_{DD} = 3.3 V; T_{amb} = 25 °C; active mode; all peripherals except one UART; BOD disabled; SRAM0 and SRAM1 powered, SRAM2 powered down. See the FLASHCFG register in the LPC5410x User Manual for system clock flash access time settings. Measured with Keil uVision 5.12. Optimization level 3, optimized for time on.

12 MHz: IRC enabled; PLL disabled. 24 MHz - 100 MHz: IRC enabled; PLL enabled.

Fig 8. Typical CoreMark score

Table 11. Static characteristics: Power consumption in active and sleep modes

T_{amb} = −40 °C to +105 °C, unless otherwise specified.1.62 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
ARM Cortex-M4 in sleep mode; ARM Cortex-M0+ in sleep mode							
I_{DD}	supply current	CCLK = 12 MHz	[2][4][7]	-	990	-	μA
		CCLK = 100 MHz	[3][4][7]	-	4.0	-	mA

[1] Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C), 3.3V.

[2] Clock source 12 MHz IRC. PLL disabled.

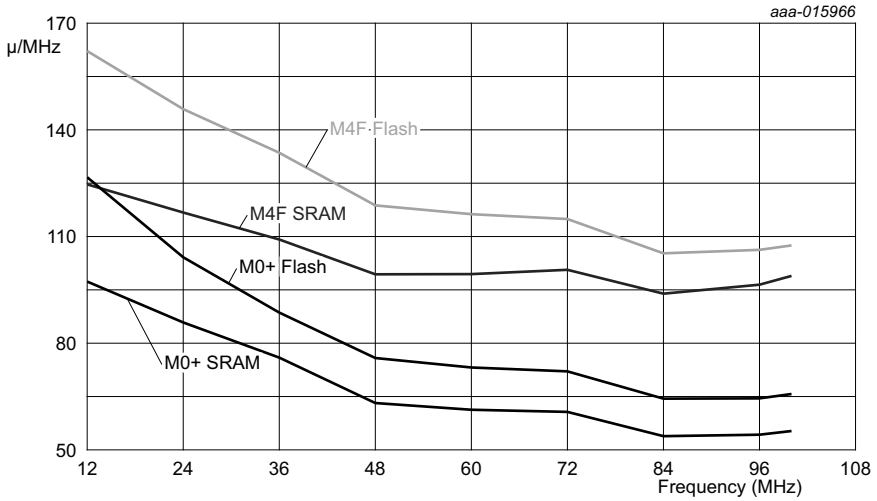
[3] Clock source 12 MHz IRC. PLL enabled.

[4] Characterized through bench measurements using typical samples.

[5] Compiler settings: Keil µVision v.5.10, optimization level 0, optimized for time off.

[6] Prefetch disabled in FLASHCFG register. System clock flash access time set by power API. SRAM0 powered, SRAM1 and SRAM2 powered down.Compiler settings: Keil µVision v.5.12, optimization level 0, optimized for time off.

[7] First 8 kB in SRAM0 powered; Flash, SRAM1, and SRAM2 are powered down; all peripheral clocks disabled. Compiler settings: Keil µVision v.5.12, optimization level 0, optimized for time off.



Conditions: V_{DD} = 3.3 V; T_{amb} = 25 °C; active mode; all peripherals disabled; BOD disabled; Prefetch disabled in FLASHCFG register. System clock flash access time set by power API. SRAM0 powered, SRAM1 and SRAM2 powered down. Measured with Keil uVision 5.12. Optimization level 0, optimized for time off.

12 MHz: IRC enabled; PLL disabled. 24 MHz - 100 MHz: IRC enabled; PLL enabled.

Fig 9. CoreMark power consumption: typical µA/MHz for M4 and M0+ cores

[1] Number of erase/program cycles.

[2] Programming times are given for writing 256 bytes from RAM to the flash.

11.3 I/O pins

Table 19. Dynamic characteristic: I/O pins[1]
T_{amb} = −40 °C to +85 °C; 1.62 V ≤ V_{DD} ≤ 3.6 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Standard I/O pins - normal drive strength							
t_r	rise time	pin configured as output; SLEW = 1 (fast mode);	[2][3]				
		2.7 V ≤ V_{DD} ≤ 3.6 V		1.0	-	2.5	ns
		1.62 V ≤ V_{DD} ≤ 1.98 V		1.6	-	3.8	ns
t_f	fall time	pin configured as output; SLEW = 1 (fast mode);	[2][3]				
		2.7 V ≤ V_{DD} ≤ 3.6 V		0.9	-	2.5	ns
		1.62 V ≤V_{DD} ≤ 1.98 V		1.7	-	4.1	ns
t_r	rise time	pin configured as output; SLEW = 0 (standard mode);	[2][3]				
		2.7 V ≤ V_{DD} ≤ 3.6 V		1.9	-	4.3	ns
		1.62 V ≤ V_{DD} ≤ 1.98 V		2.9	-	7.8	ns
t_f	fall time	pin configured as output; SLEW = 0 (standard mode);	[2][3]				
		2.7 V ≤ V_{DD} ≤ 3.6 V		1.9	-	4.0	ns
		1.62 V ≤ V_{DD} ≤ 1.98 V		2.7	-	6.7	ns
t_r	rise time	pin configured as input	[4]	0.3	-	1.3	ns
t_f	fall time	pin configured as input	[4]	0.2	-	1.2	ns

[1] Simulated data.

[2] Simulated using 10 cm of 50 Ω PCB trace with 5 pF receiver input. Rise and fall times measured between 80 % and 20 % of the full output signal level.

[3] The slew rate is configured in the IOCON block the SLEW bit. See the LPC5410x user manual.

[4] C_L = 20 pF. Rise and fall times measured between 90 % and 10 % of the full input signal level.

11.4 Wake-up process

Table 20. Dynamic characteristic: Typical wake-up times from low power modes
V_{DD} = 3.3 V;T_{amb} = 25 °C; using IRC as the system clock.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
t_{wake}	wake-up time	from sleep mode	[2][3]	-	1.6	-	µs
		from deep sleep mode with full SRAM retention: to code executing in flash or SRAM	[2]	-	18	-	µs
		from power down mode	[2]		180	-	µs
		from deep power-down mode; RTC disabled; using $\overline{\text{RESET}}$ pin.	[4]	-	200	-	µs

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

11.8 Watchdog oscillator

Table 25. Dynamic characteristics: Watchdog oscillator

Symbol	Parameter		Min	Typ[1]	Max	Unit
$f_{osc(int)}$	internal watchdog oscillator frequency	[2]	-	500	-	kHz
D_{clkout}	clkout duty cycle		48	-	52	%
J_{PP-CC}	peak-peak period jitter	[3][4]	-	1	20	ns
t_{start}	start-up time	[4]	-	4	-	µs

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] The typical frequency spread over processing and temperature (T_{amb} = −40 °C to +105 °C) is ±40 %.

[3] Actual jitter dependent on amplitude and spectrum of substrate noise.

[4] Guaranteed by design. Not tested in production samples.

11.9 I²C-bus

Table 26. Dynamic characteristic: I²C-bus pins[1]

T_{amb} = −40 °C to +105 °C; 1.62 V ≤ V_{DD} ≤ 3.6 V.[2]

Symbol	Parameter		Conditions	Min	Max	Unit
f_{SCL}	SCL clock frequency		Standard-mode	0	100	kHz
			Fast-mode	0	400	kHz
			Fast-mode Plus	0	1	MHz
t_f	fall time	[4][5][6][7]	of both SDA and SCL signals Standard-mode	-	300	ns
			Fast-mode	20 + 0.1 × C_b	300	ns
			Fast-mode Plus	-	120	ns
t_{LOW}	LOW period of the SCL clock		Standard-mode	4.7	-	µs
			Fast-mode	1.3	-	µs
			Fast-mode Plus	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock		Standard-mode	4.0	-	µs
			Fast-mode	0.6	-	µs
			Fast-mode Plus	0.26	-	µs
$t_{HD;DAT}$	data hold time	[3][4][8]	Standard-mode	0	-	µs
			Fast-mode	0	-	µs
			Fast-mode Plus	0	-	µs
$t_{SU;DAT}$	data set-up time	[9][10]	Standard-mode	250	-	ns
			Fast-mode	100	-	ns
			Fast-mode Plus	50	-	ns

[1] Guaranteed by design. Not tested in production.

[2] Parameters are valid over operating temperature range unless otherwise specified. See the I²C-bus specification *UM10204* for details.

[3] tHD;DAT is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[4] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[5] C_b = total capacitance of one bus line in pF. If mixed with Hs-mode devices, faster fall times are allowed.

11.10 SPI interfaces

The actual SPI bit rate depends on the delays introduced by the external trace, the external device, system clock (CCLK), and capacitive loading. Excluding delays introduced by external device and PCB, the maximum supported bit rate for SPI master mode is 48 Mbit/s, and the maximum supported bit rate for SPI slave mode is 21 Mbit/s.

Table 27. SPI dynamic characteristics[1]

T_{amb} = −40 °C to 105 °C; C_L = 30 pF balanced loading on all pins; SLEW = standard mode. Parameters sampled at the 50 % level of the rising or falling edge.

Symbol	Parameter	Conditions		Min	Max	Unit
SPI master 1.62V ≤ VDD ≤ 2.0 V						
t_{DS}	data set-up time	CCLK = 1 MHz to 12 MHz		0	-	ns
		CCLK = 48 MHz to 60 MHz		0	-	ns
		CCLK = 96 MHz		0	-	ns
t_{DH}	data hold time	CCLK = 1 MHz to 12 MHz		14	-	ns
		CCLK = 48 MHz to 60 MHz		12	-	ns
		CCLK = 96 MHz		9	-	ns
$t_{v(Q)}$	data output valid time	CCLK = 1 MHz to 12 MHz		0	7	ns
		CCLK = 48 MHz to 60 MHz		0	2	ns
		CCLK = 96 MHz		0	2	ns
SPI slave 1.62V ≤ VDD ≤ 2.0 V						
t_{DS}	data set-up time	CCLK = 1 MHz to 12 MHz		22	-	ns
		CCLK = 48 MHz to 60 MHz		4	-	ns
		CCLK = 96 MHz		4	-	ns
t_{DH}	data hold time	CCLK = 1 MHz to 12 MHz		0	-	ns
		CCLK = 48 MHz to 60 MHz		0	-	ns
		CCLK = 96 MHz		0	-	ns
$t_{v(Q)}$	data output valid time	CCLK = 1 MHz to 12 MHz		46	70	ns
		CCLK = 48 MHz to 60 MHz		30	37	ns
		CCLK = 96 MHz		30	36	ns
SPI master 2.7 V ≤ VDD ≤ 3.6 V						
t_{DS}	data set-up time	CCLK = 1 MHz to 12 MHz		0	-	ns
		CCLK = 48 MHz to 60 MHz		0	-	ns
		CCLK = 96 MHz		0	-	ns
t_{DH}	data hold time	CCLK = 1 MHz to 12 MHz		10	-	ns
		CCLK = 48 MHz to 60 MHz		8	-	ns
		CCLK = 96 MHz		7	-	ns
$t_{v(Q)}$	data output valid time	CCLK = 1 MHz to 12 MHz		0	6	ns
		CCLK = 48 MHz to 60 MHz		0	1	ns
		CCLK = 96 MHz		0	1	ns
SPI slave 2.7V ≤ VDD ≤ 3.6 V						
t_{DS}	data set-up time	CCLK = 1 MHz to 12 MHz		21	-	ns
		CCLK = 48 MHz to 60 MHz		4	-	ns
		CCLK = 96 MHz		3	-	ns

Table 27. SPI dynamic characteristics[1]

T_{amb} = −40 °C to 105 °C; C_L = 30 pF balanced loading on all pins; SLEW = standard mode. Parameters sampled at the 50 % level of the rising or falling edge.

Symbol	Parameter	Conditions		Min	Max	Unit
t_{DH}	data hold time	CCLK = 1 MHz to 12 MHz		0	-	ns
		CCLK = 48 MHz to 60 MHz		0	-	ns
		CCLK = 96 MHz		0	-	ns
$t_{v(Q)}$	data output valid time	CCLK = 1 MHz to 12 MHz		36	61	ns
		CCLK = 48 MHz to 60 MHz		21	22	ns
		CCLK = 96 MHz		20	21	ns

[1] *Based on characterization; not tested in production.*

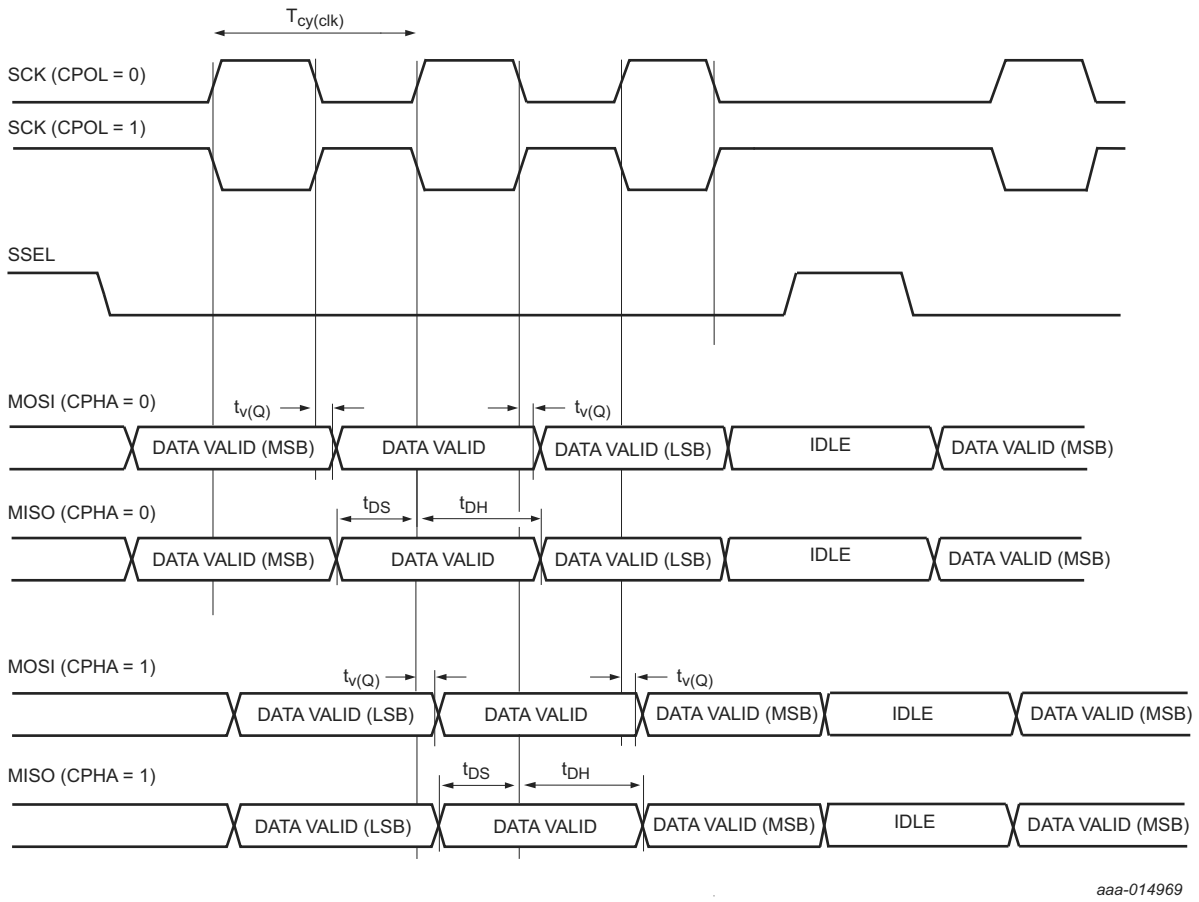


Fig 21. SPI master timing

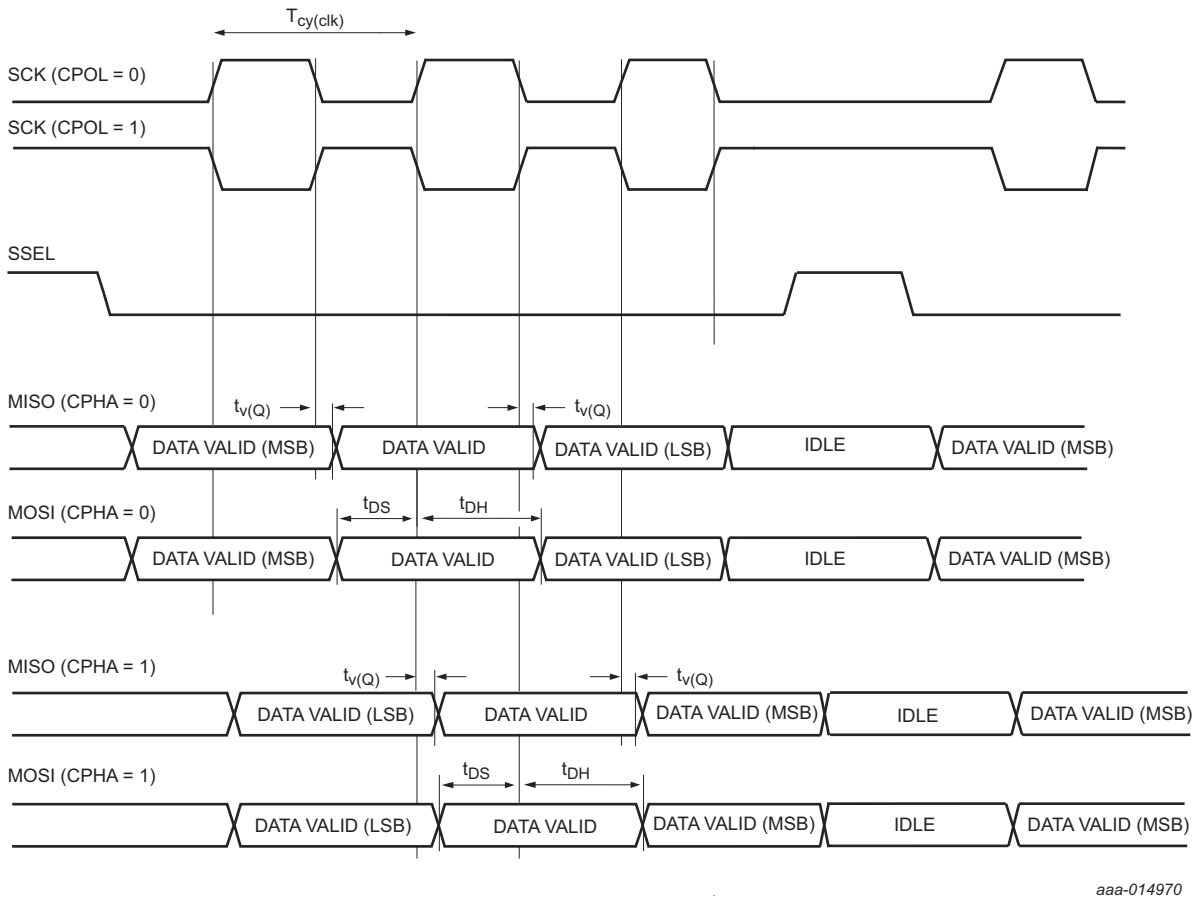


Fig 22. SPI slave timing

Table 28. USART dynamic characteristics[1]

T_{amb} = −40 °C to 105 °C; 1.62 V ≤ V_{DD} ≤ 3.6 V; C_L = 30 pF balanced loading on all pins; SLEW = standard mode. Parameters sampled at the 50% level of the falling or rising edge.

Symbol	Parameter	Conditions	Min	Max	Unit
USART slave (in synchronous mode) 2.7V ≤ VDD ≤ 3.6 V					
$t_{su(D)}$	data input set-up time	CCLK = 1 MHz to 12 MHz	21	-	ns
		CCLK = 48 MHz to 60 MHz	5	-	ns
		CCLK = 96 MHz	4	-	ns
$t_{h(D)}$	data input hold time	CCLK = 1 MHz to 12 MHz	0	-	ns
		CCLK = 48 MHz to 60 MHz	0	-	ns
		CCLK = 96 MHz	0	-	ns
$t_{v(Q)}$	data output valid time	CCLK = 1 MHz to 12 MHz	37	62	ns
		CCLK = 48 MHz to 60 MHz	22	25	ns
		CCLK = 96 MHz	19	21	ns

[1] *Based on characterization; not tested in production.*

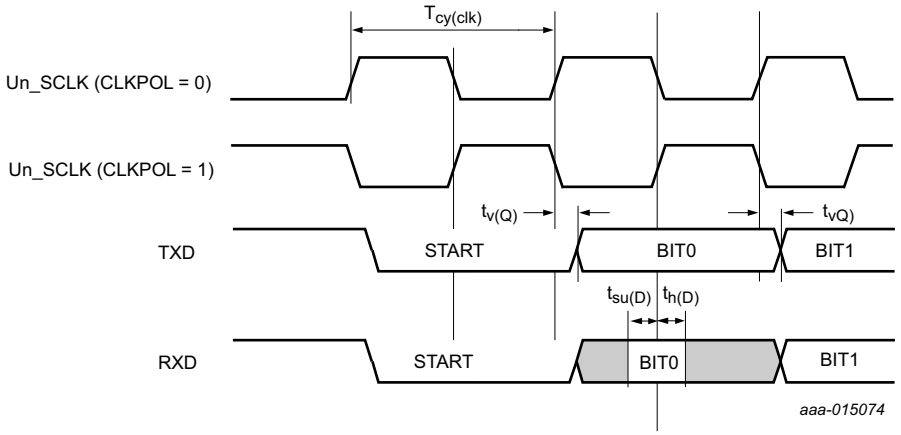


Fig 23. USART timing

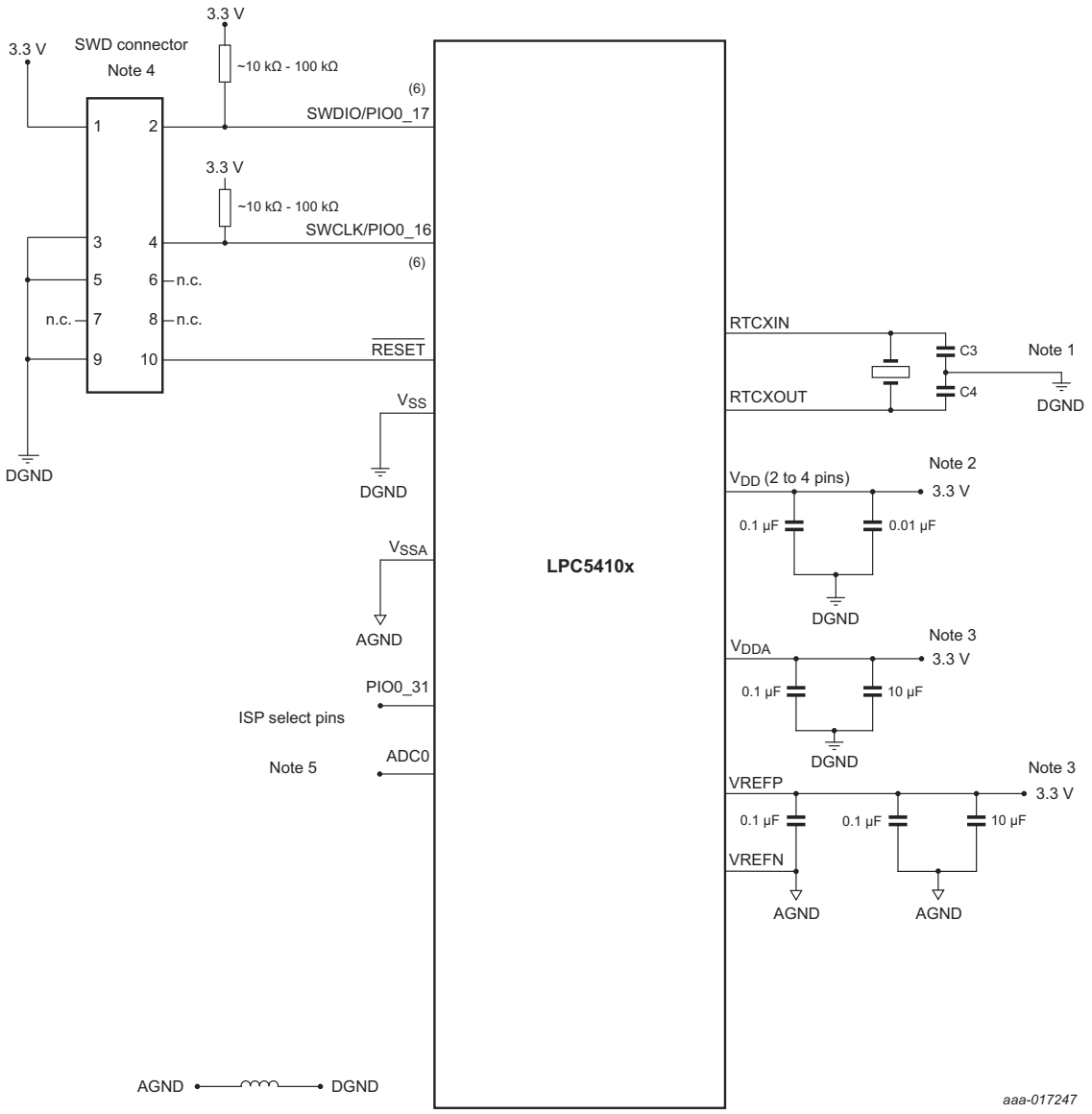
11.12 SCTimer/PWM output timing

Table 29. SCTimer/PWM output dynamic characteristics

T_{amb} = −40 °C to 105 °C; 1.62 V ≤ V_{DD} ≤ 3.6 V C_L = 30 pF. Simulated skew (over process, voltage, and temperature) of any two SCT fixed-pin output signals; sampled at 10 % and 90 % of the signal level; values guaranteed by design.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{sk(o)}$	output skew time	-	-	-	3.0	ns

13.3 Connecting power, clocks, and debug functions



(1) See Section 13.5 “RTC oscillator” for the values of C3 and C4.

(2) Position the decoupling capacitors of 0.1 µF and 0.01 µF as close as possible to the V_{DD} pin. Add one set of decoupling capacitors to each V_{DD} pin.

(3) Position the decoupling capacitors of 0.1 µF as close as possible to the VREFN and V_{DDA} pins. The 10 µF bypass capacitor filters the power line. Tie V_{DDA} and VREFP to V_{DD} if the ADC is not used. Tie VREFN to V_{SS} if ADC is not used.

(4) Uses the ARM 10-pin interface for SWD.

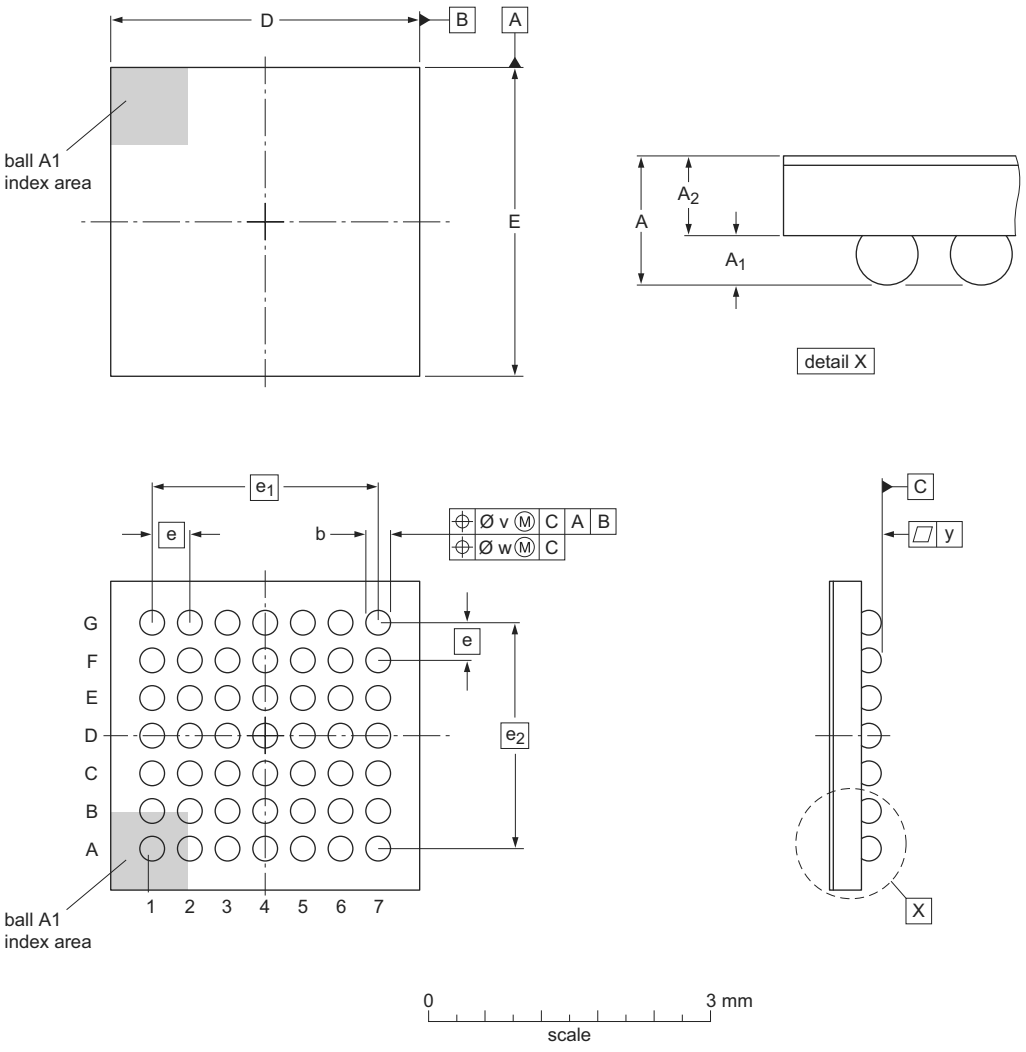
(5) When measuring signals of low frequency, use a low-pass filter to remove noise and to improve ADC performance. Also see Ref. 3.

(6) External pull-up resistors on SWDIO and SWCLK pins are optional because these pins have an internal pull-up enabled by default.

Fig 28. Power, clock, and debug connections

14. Package outline

WLCSP49: wafer level chip-scale package; 49 bumps; 3.29 x 3.29 x 0.54 mm (backside coating included) **LPC5410**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y
mm	max	0.58	0.23	0.37	0.29	3.318	3.318	0.4	2.4	2.4	0.05	0.015	0.03
	nom	0.54	0.20	0.34	0.26	3.288	3.288						
	min	0.50	0.17	0.31	0.23	3.258	3.258						

Note
Backside coating 40 µm

wlcsp49_lpc5410_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
LPC5410		- - -				~~13-09-16~~ 14-11-03

Fig 30. WLCSP49 Package outline

21. Contents

continued >>