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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4/M0+
Core Size	32-Bit Dual-Core
Speed	100MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	50
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	104K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc54102j512bd64ql

- One State Configurable Timer/PWM (SCT/PWM) with 8 inputs (6 external inputs and 2 internal inputs) and 8 output functions (including capture and match). Inputs and outputs can be routed to/from external pins and internally to/from selected peripherals. Internally, the SCT supports 13 captures/matches, 13 events and 13 states.
- 32-bit Real-time clock (RTC) with 1 s resolution running in the always-on power domain. A timer in the RTC can be used for wake-up from all low power modes including deep power-down, with 1 ms resolution.
- Multiple-channel multi-rate 24-bit timer (MRT) for repetitive interrupt generation at up to four programmable, fixed rates.
- Windowed Watchdog Timer (WWDT).
- Ultra-low power Micro-tick Timer, running from the Watchdog oscillator, that can be used to wake up the device from low power modes.
- Repetitive Interrupt Timer (RIT) for debug time-stamping and general-purpose use.

- Analog peripheral: 12-bit, 12-channel, Analog-to-Digital Converter (ADC) supporting 5.0 Msamples/s. The ADC supports two independent conversion sequences.
- Clock generation:
  - 12 MHz internal RC oscillator.
  - External clock input for clock frequencies of up to 25 MHz.
  - Internal low-power, watchdog oscillator (WDOSC) with a nominal frequency of 500 kHz.
  - 32 kHz low-power RTC oscillator.
  - System PLL allows CPU operation up to the maximum CPU rate. May be run from the internal RC oscillator, the external clock input CLKIN, or the RTC oscillator.
  - Clock output function for monitoring internal clocks.
  - Frequency measurement unit for measuring the frequency of any on-chip or off-chip clock signal.
- Power-saving modes and wake-up:
  - Integrated PMU (Power Management Unit) to minimize power consumption.
  - Reduced power modes: sleep, deep sleep, power down, and deep power-down.
  - Wake-up from deep sleep and power down modes via activity on the USART, SPI, and I^2C peripherals.
  - Wake-up from sleep, deep sleep, power down, and deep power-down modes using the RTC alarm.
- Single power supply 1.62 V to 3.6 V.
- Power-On Reset (POR).
- Brown-Out Detect (BOD) with separate thresholds for interrupt and forced reset.
- JTAG boundary scan supported.
- Unique device serial number (128 bit) for identification.
- Operating temperature range −40 °C to 105 °C.
- Available in a 3.288 x 3.288 mm WLCSP49 package and LQFP64 package.

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC54102J512UK49	WLCSP49	wafer level chip-size package; 49 (7 x 7) bumps; 3.288 x 3.288 x 0.54 mm	-
LPC54102J256UK49	WLCSP49	wafer level chip-size package; 49 (7 x 7) bumps; 3.288 x 3.288 x 0.54 mm	-
LPC54101J512UK49	WLCSP49	wafer level chip-size package; 49 (7 x 7) bumps; 3.288 x 3.288 x 0.54 mm	-
LPC54101J256UK49	WLCSP49	wafer level chip-size package; 49 (7 x 7) bumps; 3.288 x 3.288 x 0.54 mm	-
LPC54102J512BD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC54102J256BD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC54101J512BD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC54101J256BD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2

3.1 Ordering options

Table 2. Ordering options

Type number	Device order part number	Flash/kB	Total SRAM/kB	Core M4 w/ FPU	Core M0+	GPIO
LPC54102J512UK49	LPC54102J512UK49Z	512	104	1	1	39
LPC54102J256UK49	LPC54102J256UK49Z	256	104	1	1	39
LPC54101J512UK49	LPC54101J512UK49Z	512	104	1	0	39
LPC54101J256UK49	LPC54101J256UK49Z	256	104	1	0	39
LPC54102J512BD64	LPC54102J512BD64QL	512	104	1	1	50
LPC54102J256BD64	LPC54102J256BD64QL	256	104	1	1	50
LPC54101J512BD64	LPC54101J512BD64QL	512	104	1	0	50
LPC54101J256BD64	LPC54101J256BD64QL	256	104	1	0	50

[1] All of the parts include five 32-bit general-purpose timers, one State-Configurable Timer with PWM capabilities (SCTimer/PWM), one RTC/alarm timer, one 24-bit Multi-Rate Timer (MRT), a Windowed Watchdog Timer (WWDT), four USARTs, two SPIs, three Fast-mode plus I2C-bus interfaces with high-speed slave mode, and one 12-bit 5.0 Msamples/sec ADC.

4. Marking

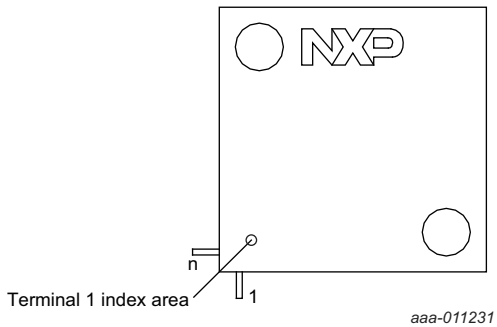


Fig 1. LQFP64 package marking

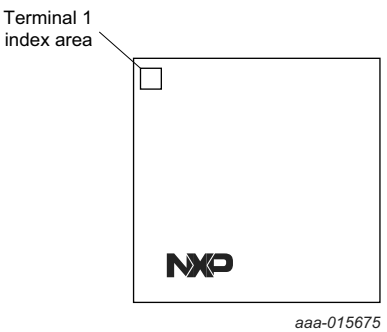


Fig 2. WLCSP49 package marking

6.2 Pin description

On the LPC5410x, digital pins are grouped into two ports. Each digital pin may support up to four different digital functions and one analog function, including General Purpose I/O (GPIO).

Table 4. Pin description

Symbol	WLCSP49	LQFP64		Reset state [1]	Type [6]	Description
PIO0_0	A6	31	[2]	PU	I/O	**PIO0_0 —** General-purpose digital input/output pin. **Remark:** In ISP mode, this pin is the UART0 RXD function.
					I	**U0_RXD —** Receiver input for USART0.
					I/O	**SPI0_SSEL0 —** Slave Select 0 for SPI0.
					I	**CT32B0_CAP0 —** 32-bit CT32B0 capture input 0.
					I	**R —** Reserved.
					O	**SCT0_OUT3 —** SCT0 output 3. PWM output 3.
PIO0_1	B6	32	[2]	PU	I/O	**PIO0_1 —** General-purpose digital input/output pin. **Remark:** In ISP mode, this pin is the UART0 TXD function.
					O	**U0_TXD —** Transmitter output for USART0.
					I/O	**SPI0_SSEL1 —** Slave Select 1 for SPI0.
					I	**CT32B0_CAP1 —** 32-bit CT32B0 capture input 1.
					I	**R —** Reserved.
					O	**SCT0_OUT1 —** SCT0 output 1. PWM output 1.
PIO0_2	-	36	[2]	PU	I/O	**PIO0_2 —** General-purpose digital input/output pin.
					I	**$\overline{\text{U0\_CTS}}$ —** Clear To Send input for USART0.
					I	**R —** Reserved.
					I	**CT32B2_CAP1 —** 32-bit CT32B2 capture input 1.
					I	**R —** Reserved.
PIO0_3	-	37	[2]	PU	I/O	**PIO0_3 —** General-purpose digital input/output pin.
					O	**$\overline{\text{U0\_RTS}}$ —** Request To Send output for USART0.
					I	**R —** Reserved.
					O	**CT32B1_MAT3 —** 32-bit CT32B1 match output 3.
					I	**R —** Reserved.
PIO0_4	C7	38	[2]	PU	I/O	**PIO0_4 —** General-purpose digital input/output pin.
					I/O	**U0_SCLK —** USART0 clock in synchronous USART mode.
					I/O	**SPI0_SSEL2 —** Slave Select 2 for SPI0.
					I	**CT32B0_CAP2 —** 32-bit CT32B0 capture input 2.
					I	**R —** Reserved.

Table 4. Pin description *…continued*

Symbol	WLCSP49	LQFP64		Reset state [1]	Type [6]	Description
PIO0_12	F7	47	[2]	PU	I/O	**PIO0_12 —** General-purpose digital input/output pin.
					I/O	**SPI0_MOSI —** Master Out Slave in for SPI0.
					O	**U1_TXD —** Transmitter output for USART1.
					O	**CT32B2_MAT3 —** 32-bit CT32B2 match output 3.
					I	**R —** Reserved.
PIO0_13	G7	48	[2]	PU	I/O	**PIO0_13 —** General-purpose digital input/output pin.
					I/O	**SPI0_MISO —** Master In Slave Out for SPI0.
					O	**SCT0_OUT4 —** SCT0 output 4. PWM output 4.
					O	**CT32B2_MAT0 —** 32-bit CT32B2 match output 0.
					I	**R —** Reserved.
PIO0_14/TCK	F6	49	[2]	PU	I/O	**PIO0_14 —** General-purpose digital input/output pin. In boundary scan mode: TCK (Test Clock).
					I/O	**SPI0_SSEL0 —** Slave Select 0 for SPI0.
					O	**SCT0_OUT5 —** SCT0 output 5. PWM output 5.
					O	**CT32B2_MAT1 —** 32-bit CT32B2 match output 1.
					I	**R —** Reserved.
PIO0_15/TDO	G6	50	[2]	PU	I/O	**PIO0_15 —** General-purpose digital input/output pin. In boundary scan mode: TDO (Test Data Out).
					I/O	**SPI0_SSEL1 —** Slave Select 1 for SPI0.
					I/O	**SWO —** Serial wire trace output.
					O	**CT32B2_MAT2 —** 32-bit CT32B2 match output 2.
					I	**R —** Reserved.
SWCLK/ PIO0_16	F5	52	[2]	PU	I/O	**PIO0_16 —** General-purpose digital input/output pin. After booting, this pin is connected to the SWCLK.
					I/O	**SPI0_SSEL2 —** Slave Select 2 for SPI0.
					I	**$\overline{\text{U1\_CTS}}$ —** Clear To Send input for USART1.
					O	**CT32B3_MAT1 —** 32-bit CT32B3 match output 1.
					I	**R —** Reserved.
					I/O	**SWCLK —** Serial Wire Clock. This is the default function after booting.
SWDIO/ PIO0_17	G5	53	[2]	PU	I/O	**PIO0_17 —** General-purpose digital input/output pin. After booting, this pin is connected to SWDIO.
					I/O	**SPI0_SSEL3 —** Slave Select 3 for SPI0.
					O	**$\overline{\text{U1\_RTS}}$ —** Request To Send output for USART1.
					O	**CT32B3_MAT2 —** 32-bit CT32B3 match output 2.
					I	**R —** Reserved.
					I/O	**SWDIO —** Serial Wire Debug I/O. This is the default function after booting.

Table 4. Pin description *…continued*

Symbol	WLCSP49	LQFP64		Reset state [1]	Type [6]	Description
PIO0_24	F1	2	[3]	Z	I/O	**PIO0_24 —** General-purpose digital input/output pin.
					I/O	**I2C0_SDA —** I^2C0 data input/output.
					I	**R —** Reserved.
					I	**CT32B0_CAP1 —** 32-bit CT32B0 capture input 1.
					I	**R —** Reserved.
					O	**CT32B0_MAT0 —** 32-bit CT32B0 match output 0.
PIO0_25	E2	3	[3]	Z	I/O	**PIO0_25 —** General-purpose digital input/output pin.
					I/O	**I2C1_SCL —** I^2C1 clock input/output.
					I	**$\overline{\text{U1\_CTS}}$ —** Clear To Send input for USART1.
					I	**CT32B0_CAP2 —** 32-bit CT32B0 capture input 2.
					I	**R —** Reserved.
					I	**CT32B1_CAP1 —** 32-bit CT32B1 capture input 1.
PIO0_26	E1	4	[3]	Z	I/O	**PIO0_26 —** General-purpose digital input/output pin.
					I/O	**I2C1_SDA —** I^2C1 data input/output.
					I	**R —** Reserved.
					I	**CT32B0_CAP3 —** 32-bit CT32B0 capture input 3.
					I	**R —** Reserved.
PIO0_27	D2	5	[3]	Z	I/O	**PIO0_27 —** General-purpose digital input/output pin.
					I/O	**I2C2_SCL —** I^2C2 clock input/output.
					I	**R —** Reserved.
					I	**CT32B2_CAP0 —** 32-bit CT32B2 capture input 0.
					I	**R —** Reserved.
PIO0_28	D1	6	[3]	Z	I/O	**PIO0_28 —** General-purpose digital input/output pin.
					I/O	**I2C2_SDA —** I^2C2 data input/output.
					I	**R —** Reserved.
					O	**CT32B2_MAT0 —** 32-bit CT32B2 match output 0.
					I	**R —** Reserved.
PIO0_29/ ADC0_0	D3	11	[4]	PU	I/O; AI	**PIO0_29/ADC0_0 —** General-purpose digital input/output pin (default). ADC input channel 0 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					O	**SCT0_OUT2 —** SCT0 output 2.
					O	**CT32B0_MAT3 —** 32-bit CT32B0 match output 3.
					I	**R —** Reserved.
					I	**CT32B0_CAP1 —** 32-bit CT32B0 capture input 1.
					O	**CT32B0_MAT1 —** 32-bit CT32B0 match output 1.

6.2.1 Termination of unused pins

Table 5 shows how to terminate pins that are **not** used in the application. In many cases, unused pins should be connected externally or configured correctly by software to minimize the overall power consumption of the part.

Unused pins with GPIO function should be configured as outputs set to LOW with their internal pull-up disabled. To configure a GPIO pin as output and drive it LOW, select the GPIO function in the IOCON register, select output in the GPIO DIR register, and write a 0 to the GPIO PORT register for that pin. Disable the pull-up in the pin's IOCON register.

In addition, it is recommended to configure all GPIO pins that are not bonded out on smaller packages as outputs driven LOW with their internal pull-up disabled.

Table 5. Termination of unused pins

Pin	Default state[1]	Recommended termination of unused pins
$\overline{\text{RESET}}$	I; PU	The $\overline{\text{RESET}}$ pin can be left unconnected if the application does not use it.
all PIOn_m (not open-drain)	I; PU	Can be left unconnected if driven LOW and configured as GPIO output with pull-up disabled by software.
PIOn_m (I2C open-drain)	IA	Can be left unconnected if driven LOW and configured as GPIO output by software.
RTCXIN	-	Connect to ground. When grounded, the RTC oscillator is disabled.
RTCXOUT	-	Can be left unconnected.
VREFP	-	Tie to VDD.
VREFN	-	Tie to VSS.
VDDA	-	Tie to VDD.
VSSA	-	Tie to VSS.

[1] I = Input, IA = Inactive (no pull-up/pull-down enabled), PU = Pull-Up.

6.2.2 Pin states in different power modes

Table 6. Pin states in different power modes

Pin	Active	Sleep	Deep sleep/Power down	Deep power-down
PIOn_m pins (not I2C)	As configured in the IOCON[1]. Default: internal pull-up enabled.			Floating.
PIO0_23 to PIO0_28 (open-drain I2C-bus pins)	As configured in the IOCON[1].			Floating.
$\overline{\text{RESET}}$	Reset function enabled. Default: input, internal pull-up enabled. Reset function disabled.			

[1] Default and programmed pin states are retained in sleep, deep sleep, and power down modes.

7.18.6.1 Features

- 48-bit counter running from the main clock. Counter can be free-running or be reset by a generated interrupt.
- 48-bit compare value.
- 48-bit compare mask. An interrupt is generated when the counter value equals the compare value, after masking. This allows for combinations not possible with a simple compare.

7.18.7 Micro-tick timer (UTICK)

The ultra-low power Micro-tick Timer, running from the Watchdog oscillator, can be used to wake up the device from low power modes.

7.18.7.1 Features

- Ultra simple timer.
- Write once to start.
- Interrupt or software polling.

7.19 12-bit Analog-to-Digital Converter (ADC)

The ADC supports a resolution of 12-bit and fast conversion rates of up to 5.0 Msamples/s. Sequences of analog-to-digital conversions can be triggered by multiple sources. Possible trigger sources are the SCT, external pins, and the ARM TXEV interrupt.

The ADC supports a variable clocking scheme with clocking synchronous to the system clock or independent, asynchronous clocking for high-speed conversions

The ADC includes a hardware threshold compare function with zero-crossing detection. The threshold crossing interrupt is connected internally to the SCT inputs for tight timing control between the ADC and the SCT.

7.19.1 Features

- 12-bit successive approximation analog to digital converter.
- Input multiplexing among up to 12 pins.
- Two configurable conversion sequences with independent triggers.
- Optional automatic high/low threshold comparison and “zero crossing” detection.
- Measurement range VREFN to VREFP (typically 3 V; not to exceed VDDA voltage level).
- 12-bit conversion rate of 5.0 MHz. Options for reduced resolution at higher conversion rates.

- Burst conversion mode for single or multiple inputs.
- Synchronous or asynchronous operation. Asynchronous operation maximizes flexibility in choosing the ADC clock frequency, Synchronous mode minimizes trigger latency and can eliminate uncertainty and jitter in response to a trigger.

7.20 System control

7.20.1 Clock sources

The LPC5410x supports two external and three internal clock sources:

- The Internal RC (IRC).
- Watchdog oscillator (WDOSC).
- External clock source from the digital I/O pin CLKIN.
- External RTC 32 KHz clock.
- Output of the system PLL.

7.20.1.1 Internal RC oscillator (IRC)

The IRC can be used as the clock that drives the system PLL and subsequently the CPU. The nominal IRC frequency is 12 MHz.

Upon power-up or any chip reset, the LPC5410x uses the IRC as the clock source. Software may later switch to one of the other available clock sources.

7.20.1.2 Watchdog oscillator (WDOSC)

The watchdog oscillator is a low-power internal oscillator. The WDOSC can be used to provide a clock to the WWDT and to the entire chip. The nominal output frequency is 500 kHz.

7.20.1.3 Clock input pin (CLKIN)

An external square-wave clock source (up to 25 MHz) can be supplied on the digital I/O pin CLKIN.

7.20.2 System PLL

The system PLL accepts an input clock frequency in the range of 32 kHz to 12 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO).

The PLL can be enabled or disabled by software.

7.22 Emulation and debugging

Debug and trace functions are integrated into the ARM Cortex-M4 and ARM Cortex-M0+. Serial wire debug and trace functions are supported. The ARM Cortex-M4 is configured to support up to eight breakpoints and four watch points. The ARM Cortex-M0+ is configured to support up to four breakpoints and two watch points. In addition, JTAG boundary scan mode is provided.

The ARM SYSREQ reset is supported and causes the processor to reset the peripherals, execute the boot code, restart from address 0x0000 0000, and break at the user entry point.

The SWD pins are multiplexed with other digital I/O pins. On reset, the pins assume the SWD functions by default.

10. Static characteristics

10.1 General operating conditions

Table 9. General operating conditions

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{clk}	clock frequency	internal CPU/system clock		-	-	100	MHz
V_{DD}	supply voltage (core and external rail)			1.62	-	3.6	V
V_{DDA}	analog supply voltage		[1]	1.62	-	3.6	V
V_{refp}	ADC positive reference voltage	$V_{DDA} \geq 2$ V	[2]	2.0	-	V_{DDA}	V
		$V_{DDA} < 2$ V		V_{DDA}	-	V_{DDA}	V
RTC oscillator pins							
$V_{i(rtcx)}$	32 kHz oscillator input voltage	on pin RTCXIN		−0.5	-	+3.6	V
$V_{o(rtcx)}$	32 kHz oscillator output voltage	on pin RTCXOUT		−0.5	-	+3.6	V

[1] The V_{DD} voltage must be equal or lower than the voltage level on V_{DDA}.

[2] The V_{refp} voltage must not exceed the voltage level on V_{DDA}.

10.2 CoreMark data

Table 10. CoreMark score

T_{amb} = 25 °C, V_{DD} = 3.3V

Parameter	Conditions		Typ	Unit
ARM Cortex-M4 in active mode; ARM Cortex-M0+ in sleep mode				
CoreMark score	CoreMark code executed from SRAM; CCLK = 12 MHz	[1][3][4][5]	2.6	(Iterations/s) / MHz
	CCLK = 48 MHz	[2][3][4][5]	2.6	(Iterations/s) / MHz
	CCLK = 84 MHz	[2][3][4][5]	2.6	(Iterations/s) / MHz
	CCLK = 100 MHz	[2][3][4][5]	2.6	(Iterations/s) / MHz
CoreMark score	CoreMark code executed from flash; CCLK = 12 MHz; 1 system clock flash access time.	[1][3][4][6]	2.6	(Iterations/s) / MHz
	CCLK = 48 MHz; 3 system clock flash access time.	[2][3][4][6]	2.4	(Iterations/s) / MHz
	CCLK = 84 MHz; 5 system clock flash access time.	[2][3][4][6]	2.3	(Iterations/s) / MHz
	CCLK = 100 MHz; 6 system clock flash access time.	[2][3][4][6]	2.2	(Iterations/s) / MHz

[1] Clock source 12 MHz IRC. PLL disabled.

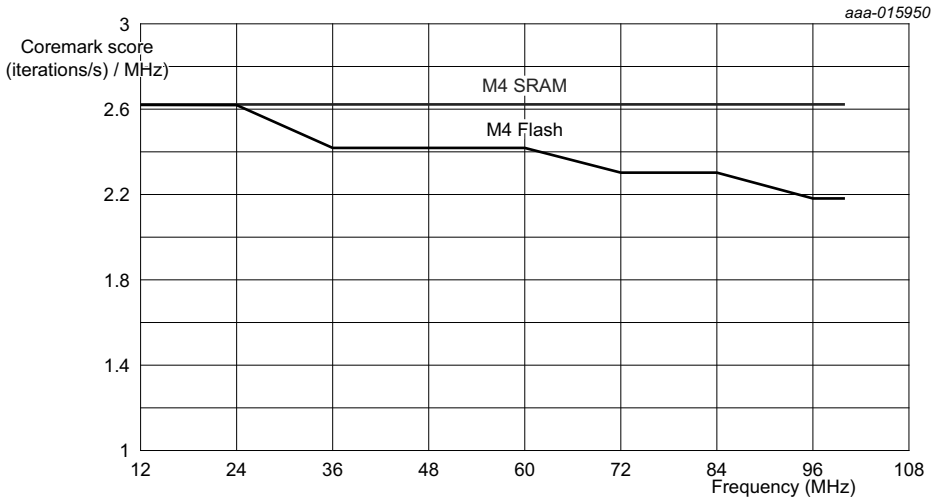
[2] Clock source 12 MHz IRC. PLL enabled.

[3] Characterized through bench measurements using typical samples.

[4] Compiler settings: Keil µVision v.5.12, optimization level 3, optimized for time on.

[5] SRAM0 and SRAM1 powered, SRAM2 powered down.

[6] See the FLASHCFG register in the LPC5410x User Manual for system clock flash access time settings.



Conditions: V_{DD} = 3.3 V; T_{amb} = 25 °C; active mode; all peripherals except one UART; BOD disabled; SRAM0 and SRAM1 powered, SRAM2 powered down. See the FLASHCFG register in the LPC5410x User Manual for system clock flash access time settings. Measured with Keil uVision 5.12. Optimization level 3, optimized for time on.

12 MHz: IRC enabled; PLL disabled. 24 MHz - 100 MHz: IRC enabled; PLL enabled.

Fig 8. Typical CoreMark score

10.3 Power consumption

Power measurements in Active, sleep, deep sleep, and power down modes were performed under the following conditions:

- Configure all pins as GPIO with pull-up resistor disabled in the IOCON block.
- Configure GPIO pins as outputs using the GPIO DIR register.
- Write 1 to the GPIO CLR register to drive the outputs LOW.
- All peripherals disabled.

Table 11. Static characteristics: Power consumption in active and sleep modes

T_{amb} = −40 °C to +105 °C, unless otherwise specified.1.62 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
ARM Cortex-M0+ in active mode; ARM Cortex-M4 in sleep mode							
I_{DD}	supply current	CoreMark code executed from SRAM; flash powered down CCLK = 12 MHz	[2][4][6]	-	1.2	-	mA
		CCLK = 48 MHz	[3][4][6]	-	3.0	-	mA
		CCLK = 84 MHz	[3][4][6]	-	4.5	-	mA
		CCLK = 100 MHz	[3][4][6]	-	5.5	-	mA
I_{DD}	supply current	CoreMark code executed from flash; CCLK = 12 MHz; 1 system clock flash access time.	[2][4][6]	-	1.5	-	mA
		CCLK = 48 MHz; 3 system clock flash access time.	[3][4][6]	-	3.6	-	mA
		CCLK = 84 MHz; 6 system clock flash access time.	[3][4][6]	-	5.4	-	mA
		CCLK = 100 MHz; 7 system clock flash access time.	[3][4][6]	-	6.6	-	mA
I_{DD}	supply current	Calculating Fibonacci numbers executed from flash; CCLK = 12 MHz	[2][4][5]	-	1.5	-	mA
		CCLK = 84 MHz	[3][4][5]	-	6.2	-	mA
		CCLK = 96 MHz	[3][4][5]	-	7.2	-	mA

Table 16. Static characteristics: pin characteristics *…continued*

T_{amb} = −40 °C to +105 °C, unless otherwise specified. 1.62 V ≤ V_{DD} ≤ 3.6 V unless otherwise specified. Values tested in production unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{OLS}	LOW-level short-circuit output current	1.62 V ≤ V_{DD} < 2.7 V	[2][4]	-	-	30	mA
	drive LOW; connected to V_{DD}	2.7 V ≤ V_{DD} ≤ 3.6 V		-	-	77	mA
Weak input pull-up/pull-down characteristics							
I_{pd}	pull-down current	V_I = V_{DD}		25		80	μA
		V_I = 5 V	[2]	80		100	μA
I_{pu}	pull-up current	V_I = 0 V		−25		−80	μA
		V_{DD} < V_I < 5 V	[2][7]	6		30	μA

Table 22. Dynamic characteristics of the PLL[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Reference clock input							
F_{in}	input frequency	-		32.768 kHz	-	25 MHz	-
Clock output							
f_o	output frequency	for PLL clkout output	[3]	1.2	-	150	MHz
d_o	output duty cycle	for PLL clkout output		46	-	54	%
f_{CCO}	CCO frequency			-	-	150	MHz
Lock detector output							
$\Delta_{lock(PFD)}$	PFD lock criterion		[4]	1	2	4	ns
Dynamic parameters at $f_{out} = f_{CCO} = 100$ MHz; standard bandwidth settings							
$J_{rms\text{-}interval}$	RMS interval jitter	f_{ref} = 10 MHz	[5][6]	-	15	30	ps
$J_{pp\text{-}period}$	peak-to-peak, period jitter	f_{ref} = 10 MHz	[5][6]	-	40	80	ps

[1] Data based on characterization results, not tested in production.

[2] Output jitter depends on the frequency of input jitter and is equal to or less than the input jitter.

[3] Excluding under- and overshoot which may occur when the PLL is not in lock.

[4] A phase difference between the inputs of the PFD (clkref and clkfb) smaller than the PFD lock criterion means lock output is HIGH.

[5] Actual jitter dependent on amplitude and spectrum of substrate noise.

[6] Input clock coming from a crystal oscillator with less than 250 ps peak-to-peak period jitter.

11.6 IRC

Table 23. Dynamic characteristic: IRC oscillator
1.62 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	T_{amb} = 25 °C	[2]	12 −1 %	12	12 +1 %	MHz
		−40 °C ≤ T_{amb} ≤ +105 °C	[3]	12 −3.5 %	12	12 +3 %	MHz
		0 °C ≤ T_{amb} ≤ +85 °C	[3]	12 −2 %	12	12 +2.5 %	MHz

[1] Typical ratings are not guaranteed. The value listed is at room temperature (25 °C).

[2] Tested in production.

[3] Guaranteed by characterization, not tested in production.

11.7 RTC oscillator

See Section 13.5 for connecting the RTC oscillator to a crystal or an external clock source.

Table 24. Dynamic characteristic: RTC oscillator
1.62 V ≤ V_{DD} ≤ 3.6 V[1]

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
f_i	input frequency	-		-	32.768	-	kHz

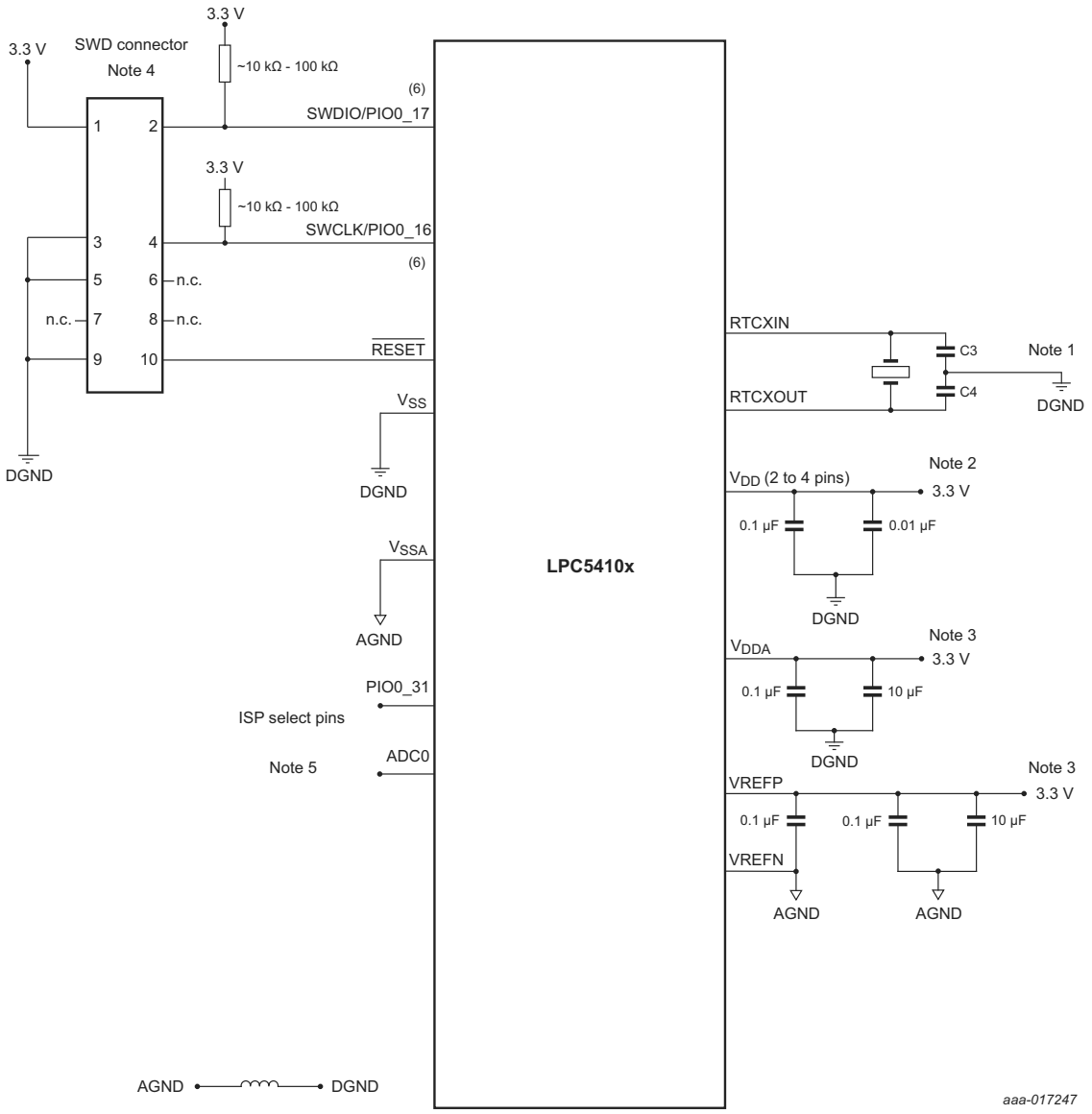
[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

Table 32. ADC sampling times[1]

-40 °C ≤ T_{amb} ≤ 85 °C; 1.62 V ≤ V_{DDA} ≤ 3.6 V; 1.62 V ≤ V_{DD} ≤ 3.6 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
ADC inputs ADC_5 to ADC_0 (fast channels); ADC resolution = 12 bit							
t_s	sampling time	Z_o < 0.05 kΩ	[3]	20	-	-	ns
		0.05 kΩ ≤ Z_o < 0.1 kΩ		23	-	-	ns
		0.1 kΩ ≤ Z_o < 0.2 kΩ		26	-	-	ns
		0.2 kΩ ≤ Z_o < 0.5 kΩ		31	-	-	ns
		0.5 kΩ ≤ Z_o < 1 kΩ		47	-	-	ns
		1 kΩ ≤ Z_o < 5 kΩ		75	-	-	ns
ADC inputs ADC_5 to ADC_0 (fast channels); ADC resolution = 10 bit							
t_s	sampling time	Z_o < 0.05 kΩ	[3]	15	-	-	ns
		0.05 kΩ ≤ Z_o < 0.1 kΩ		18	-	-	ns
		0.1 kΩ ≤ Z_o < 0.2 kΩ		20	-	-	ns
		0.2 kΩ ≤ Z_o < 0.5 kΩ		24	-	-	ns
		0.5 kΩ ≤ Z_o < 1 kΩ		38	-	-	ns
		1 kΩ ≤ Z_o < 5 kΩ		62	-	-	ns
ADC inputs ADC_5 to ADC_0 (fast channels); ADC resolution = 8 bit							
t_s	sampling time	Z_o < 0.05 kΩ	[3]	12	-	-	ns
		0.05 kΩ ≤ Z_o < 0.1 kΩ		13	-	-	ns
		0.1 kΩ ≤ Z_o < 0.2 kΩ		15	-	-	ns
		0.2 kΩ ≤ Z_o < 0.5 kΩ		19	-	-	ns
		0.5 kΩ ≤ Z_o < 1 kΩ		30	-	-	ns
		1 kΩ ≤ Z_o < 5 kΩ		48	-	-	ns
ADC inputs ADC_5 to ADC_0 (fast channels); ADC resolution = 6 bit							
t_s	sampling time	Z_o < 0.05 kΩ	[3]	9	-	-	ns
		0.05 kΩ ≤ Z_o < 0.1 kΩ		10	-	-	ns
		0.1 kΩ ≤ Z_o < 0.2 kΩ		11	-	-	ns
		0.2 kΩ ≤ Z_o < 0.5 kΩ		13	-	-	ns
		0.5 kΩ ≤ Z_o < 1 kΩ		22	-	-	ns
		1 kΩ ≤ Z_o < 5 kΩ		36	-	-	ns
ADC inputs ADC_11 to ADC_6 (slow channels); ADC resolution = 12 bit							
t_s	sampling time	Z_o < 0.05 kΩ	[3]	43	-	-	ns
		0.05 kΩ ≤ Z_o < 0.1 kΩ		46	-	-	ns
		0.1 kΩ ≤ Z_o < 0.2 kΩ		50	-	-	ns
		0.2 kΩ ≤ Z_o < 0.5 kΩ		56	-	-	ns
		0.5 kΩ ≤ Z_o < 1 kΩ		74	-	-	ns
		1 kΩ ≤ Z_o < 5 kΩ		105	-	-	ns

13.3 Connecting power, clocks, and debug functions



(1) See Section 13.5 “RTC oscillator” for the values of C3 and C4.

(2) Position the decoupling capacitors of 0.1 µF and 0.01 µF as close as possible to the V_{DD} pin. Add one set of decoupling capacitors to each V_{DD} pin.

(3) Position the decoupling capacitors of 0.1 µF as close as possible to the VREFN and V_{DDA} pins. The 10 µF bypass capacitor filters the power line. Tie V_{DDA} and VREFP to V_{DD} if the ADC is not used. Tie VREFN to V_{SS} if ADC is not used.

(4) Uses the ARM 10-pin interface for SWD.

(5) When measuring signals of low frequency, use a low-pass filter to remove noise and to improve ADC performance. Also see Ref. 3.

(6) External pull-up resistors on SWDIO and SWCLK pins are optional because these pins have an internal pull-up enabled by default.

Fig 28. Power, clock, and debug connections

13.4 I/O power consumption

I/O pins can contribute to the overall static and dynamic power consumption of the part.

If pins are configured as digital inputs with the pull-up resistor enabled, a static current can flow depending on the voltage level at the pin. This current can be calculated using the parameters I_{pu} and I_{pd} given in Table 16.

If pins are configured as digital outputs, the static current is derived from parameters IOH and IOL shown in Table 16, and any external load connected to the pin.

When an I/O pin switches in an application, it contributes to the dynamic power consumption because the VDD supply provides the current to charge and discharge all internal and external capacitive loads connected to the pin.

The contribution from the I/O switching current I_{sw} can be calculated as follows for any given switching frequency f_{sw} if the external capacitive load (C_{ext}) is known (see Table 16 for the internal I/O capacitance):

$$I_{sw} = V_{DD} \times f_{sw} \times (C_{io} + C_{ext})$$

13.5 RTC oscillator

In the RTC oscillator circuit, only the crystal (XTAL) and the capacitances C_{X1} and C_{X2} need to be connected externally on the RTCXIN and RTCXOUT pins. See Figure 29.

An external clock can be connected to RTCX1 if RTCX2 is left open. The recommended amplitude of the clock signal is $V_{i(RMS)}$ = 100 mV to 200 mV with a coupling capacitance of 5 pF to 10 pF.

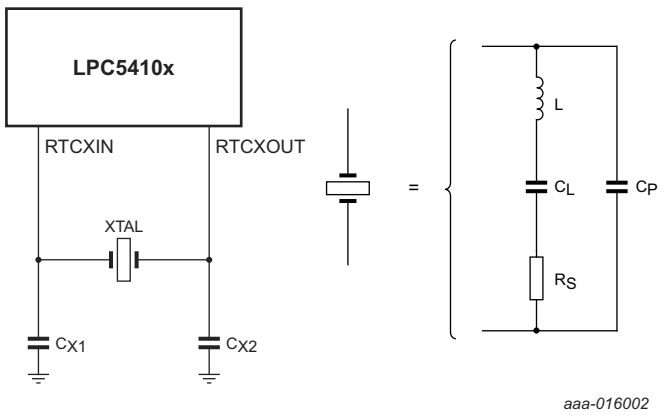


Fig 29. RTC oscillator components

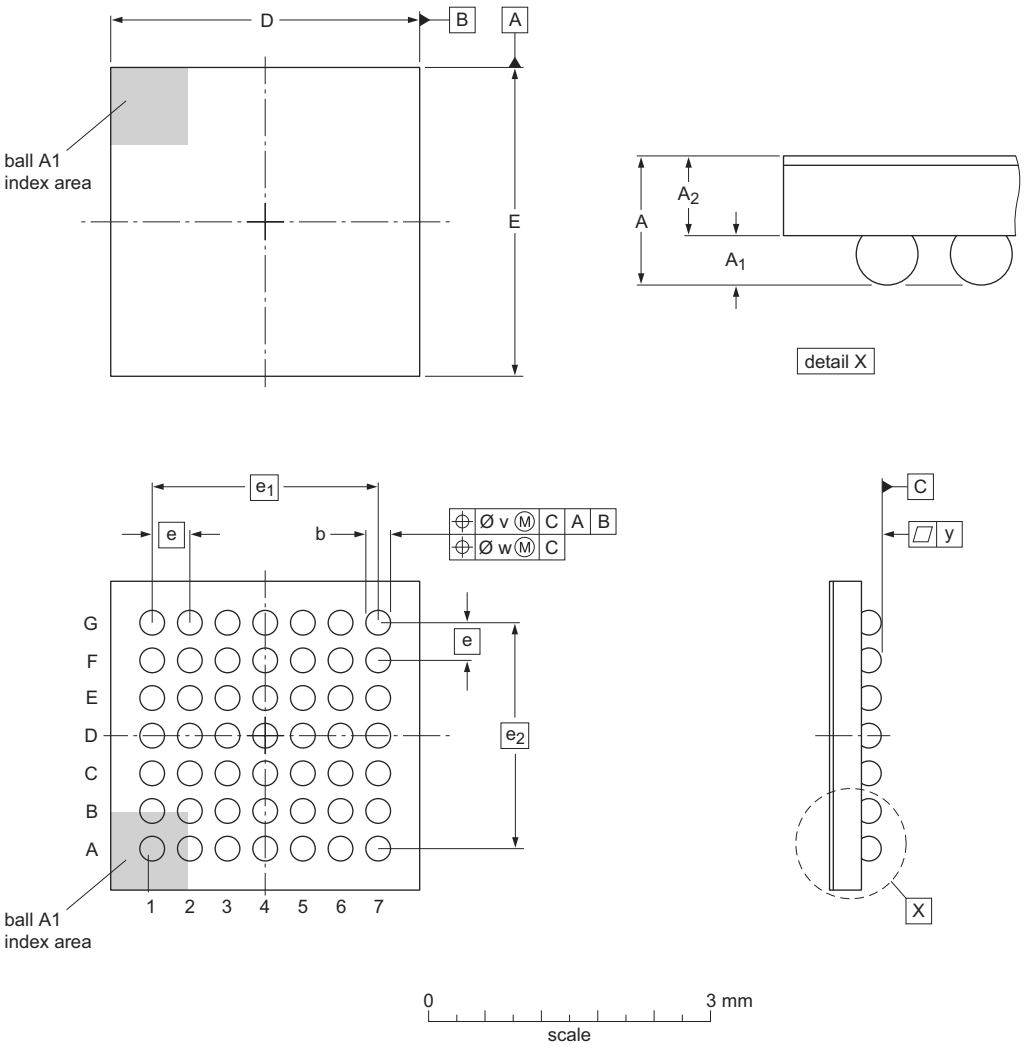
For best results, it is very critical to select a matching crystal for the on-chip oscillator. Load capacitance (C_L), series resistance (R_S), and drive level (D_L) are important parameters to consider while choosing the crystal. After selecting the proper crystal, the external load capacitor C_{X1} and C_{X2} values can also be generally determined by the following expression:

$$C_{X1} = C_{X2} = 2C_L - (C_{Pad} + C_{Parasitic})$$

Where:

14. Package outline

WLCSP49: wafer level chip-scale package; 49 bumps; 3.29 x 3.29 x 0.54 mm (backside coating included) **LPC5410**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y
mm	max	0.58	0.23	0.37	0.29	3.318	3.318	0.4	2.4	2.4	0.05	0.015	0.03
	nom	0.54	0.20	0.34	0.26	3.288	3.288						
	min	0.50	0.17	0.31	0.23	3.258	3.258						

Note
Backside coating 40 µm

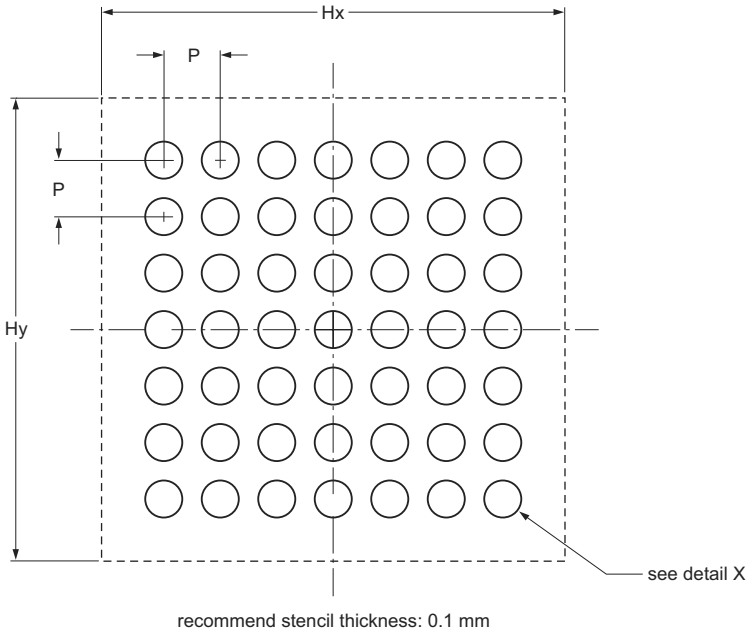
wlcsp49_lpc5410_po

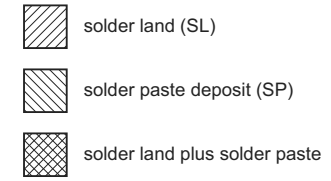
Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
LPC5410		- - -				~~13-09-16~~ 14-11-03

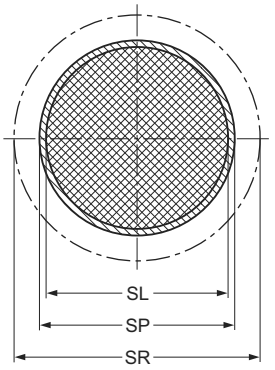
Fig 30. WLCSP49 Package outline

15. Soldering

Footprint information for reflow soldering of WLCSP49 package **LPC5410_NSMD**







detail X

Dimensions in mm

P	SL	SP	SR	Hx	Hy
0.4	0.24	0.27	0.31	3.5	3.5

wlcsp49_lpc5410_fr

Fig 32. WLCSP49 Soldering footprint

Table 36. Revision history *…continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC5410x v2.0	20150417	Product data sheet	-	LPC5410x v1.1
Modification:	• Updated the ADC conversion rate from 4.8 Msamples/s to 5.0 Msamples/s. • Added Section 7.14 “Pin interrupt/pattern engine”. • Added Section 7.18.6 “Repetitive Interrupt Timer (RIT)”. • Updated Table 12 “Static characteristics: Power consumption in deep sleep, power down, and deep power-down modes” on page 44. • Updated Table 15 “Static characteristics: pin characteristics” on page 49: – T_{amb} = −40 °C to +105 °C, unless otherwise specified. 1.62 V ≤ V_{DD} ≤ 3.6 V. – updated min and max values. • Added Section 11.1 “Power-up ramp conditions”. • Added Section 11.9 “SPI interfaces”, Section 11.10 “USART interface”, and Section 11.11 “SCTimer/PWM output timing”. • Updated Section 11.5 “IRC”: – added temperature conditions: T_{amb} = 25 °C, −40 °C ≤ T_{amb} ≤ +105 °C – updated min and max values. • Added Table 14 “Typical peripheral power consumption”. • Added Table 28 “12-bit ADC static characteristics”: – T_{amb} = −40 °C to +105 °C. – Values for E_D, $E_{L(adj)}$, E_O, and $V_{err(FS)}$. • Added Section 12.2.1 “ADC input impedance” • Updated Figure 26 “Standard I/O pin configuration” on page 71 • Minor updates to Section 13.3 “I/O power consumption”.			
LPC5410x v1.1	20141117	Product data sheet	-	LPC5410x v1.0
Modification:	• Minor editorial update in Section 1.			
LPC5410x v1.0	20141106	Product data sheet	-	-